ProxSense® IQS333 Datasheet

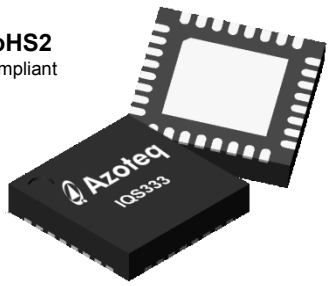
9 Channel Projected / 7 Channel Self- Capacitive Touch and Proximity Controller with 2 x 11-bit slider/scroll wheels

The **IQS333** ProxSense® IC is a 9-channel projected (or 7-channel self) capacitive proximity and touch controller with best in class sensitivity, signal to noise ratio and power consumption. Other features include automatic tuning of sense electrodes, internal reference capacitor and internal regulator to reduce total system cost.

Main Features

- 7 Self or 9 Mutual Channel Capacitive Controller
- 2 Configurable 11-bit sliders/scroll wheels
- Advanced on-chip digital signal processing
- Automatic adjustment for optimal performance (ATI)
- User selectable Proximity and Touch thresholds
- Long proximity range
- Automatic drift compensation
- Fast I^2C Interface
- Event mode or Streaming modes

RoHS2
Compliant



IQS333 QFN32
Representations only, not actual markings

- 8 PWM LED/ GPIOs drivers (5mA source/10mA sink)
  - Hardware PWM set through I^2C memory map – no overhead from host
  - Dimming modes available, up and down
  - Minimum, maximum & adjustable limit levels for dimming modes
- Low Power, suitable for battery applications
- Supply voltage: 1.8V to 3.6V
- <3µA Active sensing in LP mode

Applications

- White goods and appliances
- Office equipment, toys
- Medical and test equipment
- Blu-Ray, DVD players, TVs

Available options

T_A	QFN(5x5)-32
-40°C to 85°C	IQS333

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Functional Overview

1 Introduction

The **IQS333** is a 9 channel projected (7 self) capacitive proximity and touch sensor featuring an internal voltage regulator and reference capacitor (C_S).

The device has 7 possible pins for the connection of the sense electrodes, which consist of 7 Self electrodes, or 3 transmitters and 3 receivers. Three pins are used for serial data communication through the I^2C^{TM} compatible protocol, including an optional RDY pin. Up to 9 configurable outputs provide 8 PWM or general purpose I/O's. There is also a dedicated pin for driving a buzzer.

The device automatically tracks slow varying environmental changes via various filters, detects noise and is equipped with an Automatic Tuning Implementation (ATI) to adjust the device for optimal sensitivity.

1.1 Applicability

All specifications, except where specifically mentioned otherwise, provided by this datasheet are applicable to the following ranges:

- Temperature -40°C to +85°C
- Supply voltage (V_{DDHI}) 1.8V to 3.6V

2 Analogue Functionality

CRX and CTX electrodes are arranged in a suitable configuration that results in a mutual capacitance (Cm) between the two electrodes. CTX is charged up to a set positive potential during a charge cycle which results in a negative charge buildup at CRX.

The resulting charge displacement is then measured within the **IQS333** device through a charge transfer process that is periodically initiated by the digital circuitry. The capacitance measurement circuitry makes use of an internal reference capacitor C_S and voltage reference (V_{REF}).

The measuring process is referred to as a conversion and consists of the discharging of Cs and Cx capacitors, the charging of Cx and then a series of charge transfers from Cx to Cs until a trip voltage is reached. The number of charge transfers required to reach the trip voltage is referred to as the Counts (CS) value.

The analogue circuitry further provides functionality for:

- Power On Reset (POR) detection.
- Brown Out Detection (BOD).
- Internal regulation provides for accurate sampling.

3 Digital Functionality

The digital processing functionality is responsible for:

- Managing BOD and WDT events.
- Initiation of conversions at the selected rate.
- Processing of CS and execution of algorithms.
- Monitoring and execution of the ATI algorithm.
- Signal processing and digital filtering.
- Detection of PROX and TOUCH events.
- Managing outputs of the device.
- Managing serial communications.

4 Hardware Configuration

The IQS333 can be configured to charge in Self- or Projected-Capacitive mode through the memory map by the host controller. The IQS333 is default in Self-Capacitive mode, and can be set to Projected-Capacitive mode by setting the “Proj Mode” bit in Register 0x01, byte 0.

In **Self-Capacitive** mode, the IQS333 has 7 channels. It can be used as 7 discrete buttons OR 1 slider and 4 buttons, OR 2 sliders with 1 button.

In **Projected-Capacitive** mode, the IQS333 has 9 channels. It can be used as 9 discrete buttons OR 1 slider with 6 buttons, OR 2 sliders with 3 buttons.

4.1 IQS333 Pin Out

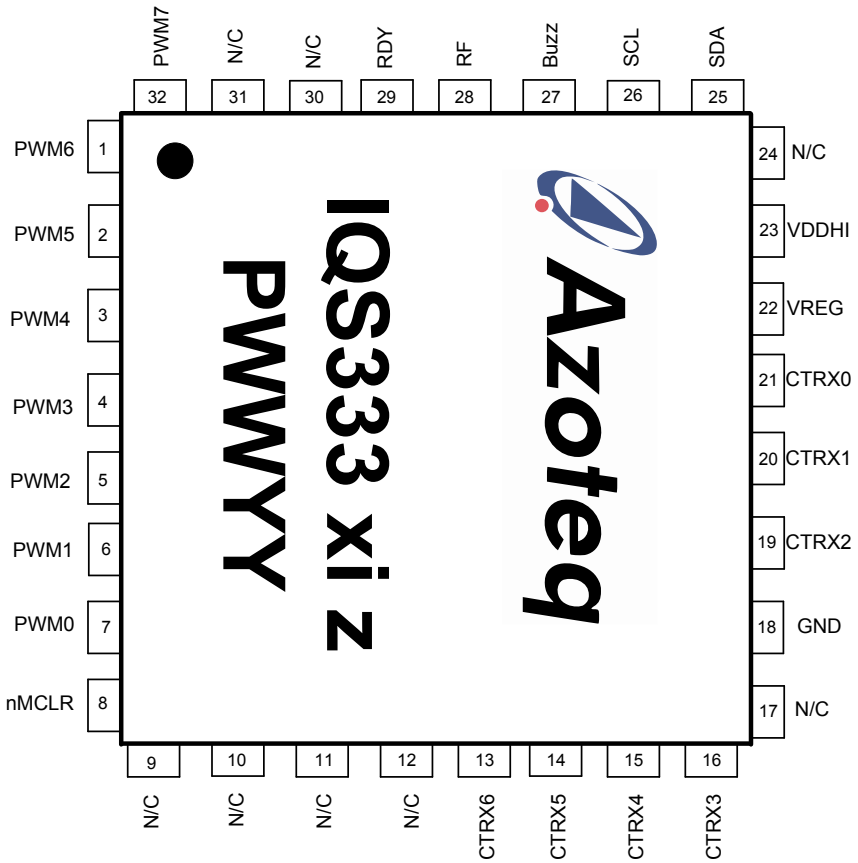


Figure 4.1 IQS333 Pin out in QFN-32.

Table 4.1 IQS333 QFN-32 Pin-outs.

Pin	Self-Capacitive	Projected-Capacitive	Function
1	PWM6	PWM6	Output
2	PWM5	PWM5	Output
3	PWM4	PWM4	Output
4	PWM3	PWM3	Output
5	PWM2	PWM2	Output
6	PWM1	PWM1	Output
7	PWM0	PWM0	Output
8	NMCLR	NMCLR	Master Clear
9	N/C	N/C	No Connect
10	N/C	N/C	No Connect
11	N/C	N/C	No Connect
12	N/C	N/C	No Connect
13	CX6		Sense Electrode
14	CX5	TX2	Sense Electrode
15	CX4	TX1	Sense Electrode
16	CX3	TX0	Sense Electrode
17	N/C	N/C	No Connect
18	GND	GND	Supply Ground
19	CX2	CRX2	Sense Electrode
20	CX1	CRX1	Sense Electrode
21	CX0	CRX0	Sense Electrode
22	VREG	VREG	Regulator Output
23	VDDHI	VDDHI	Supply Input
24	N/C	N/C	No Connect
25	SDA	SDA	I^2C Data
26	SCL	SCL	I^2C Clock
27	BUZ	BUZ	Buzzer
28	RF	RF	Noise Detect
29	RDY	RDY	Ready
30	N/C	N/C	No Connect
31	N/C	N/C	No Connect
32	PWM7	PWM7	Output

4.2 Reference Design

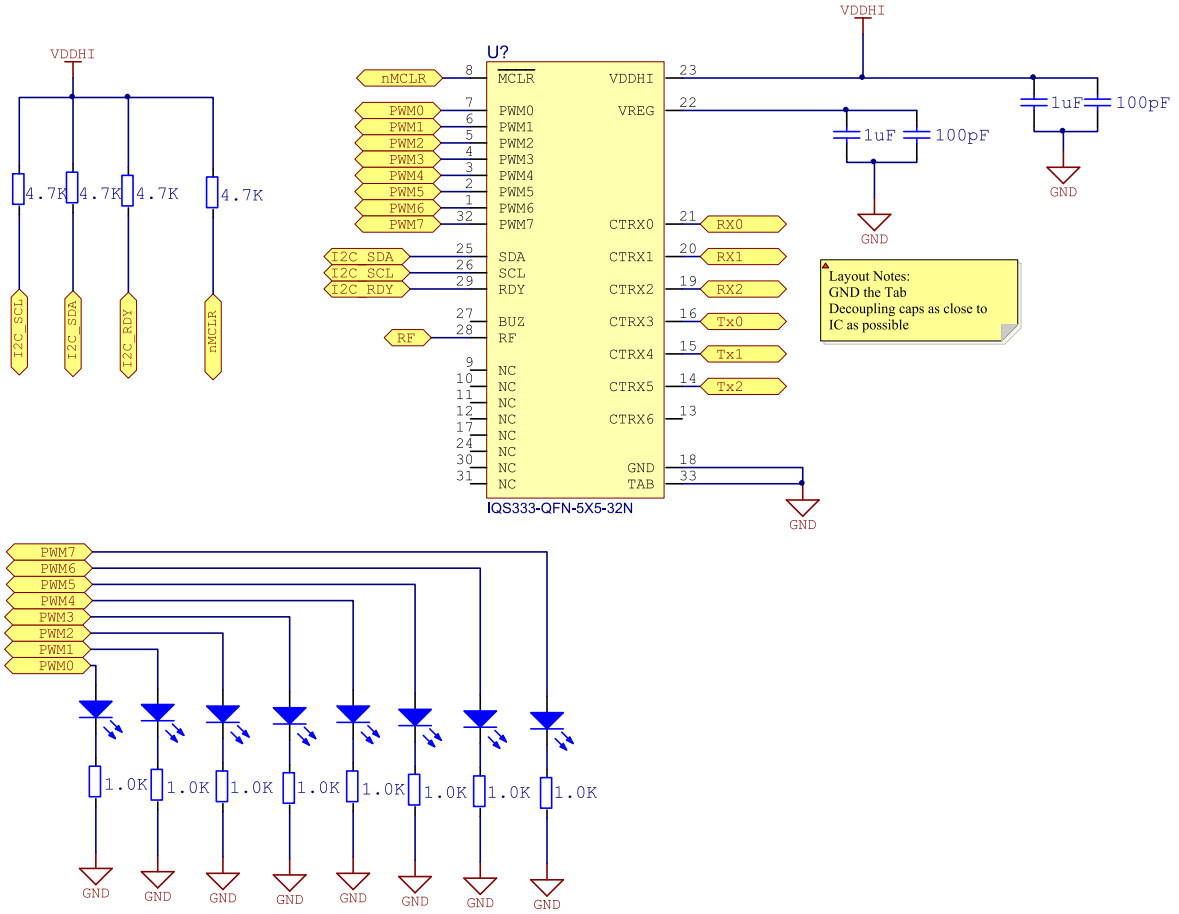


Figure 4.2 IQS333 Reference Design (Projected capacitive sensing).

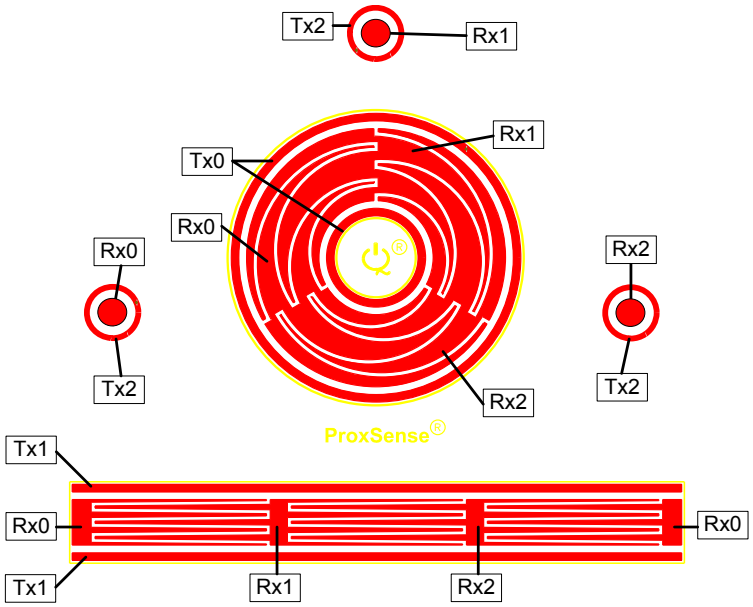


Figure 4.3 Projected-Capacitive Wheel, Slider and Button layout guidelines.
DXF files for wheels and sliders are available on request: info@azoteq.com.

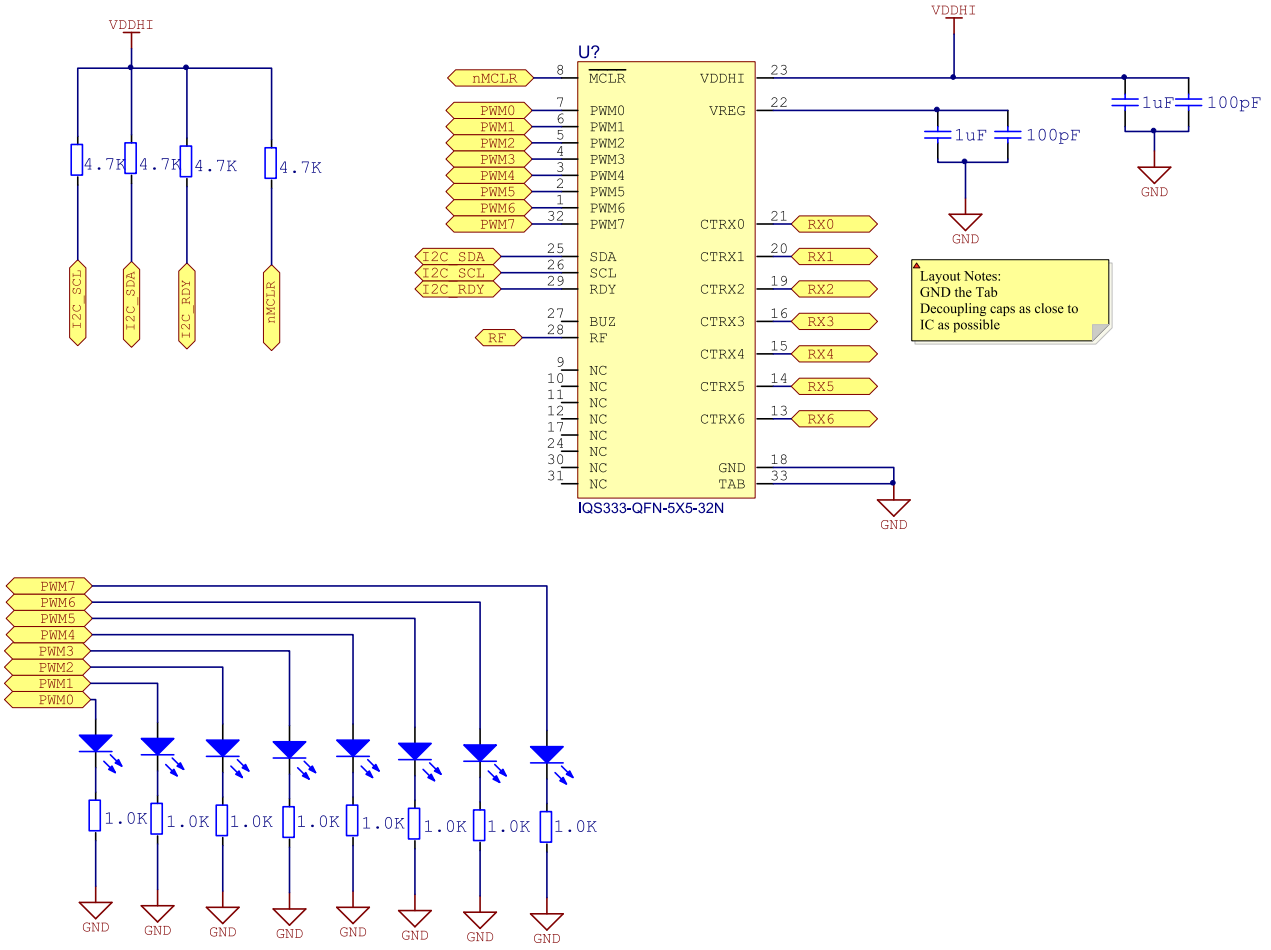


Figure 4.4 IQS333 Self Capacitive Reference Design.

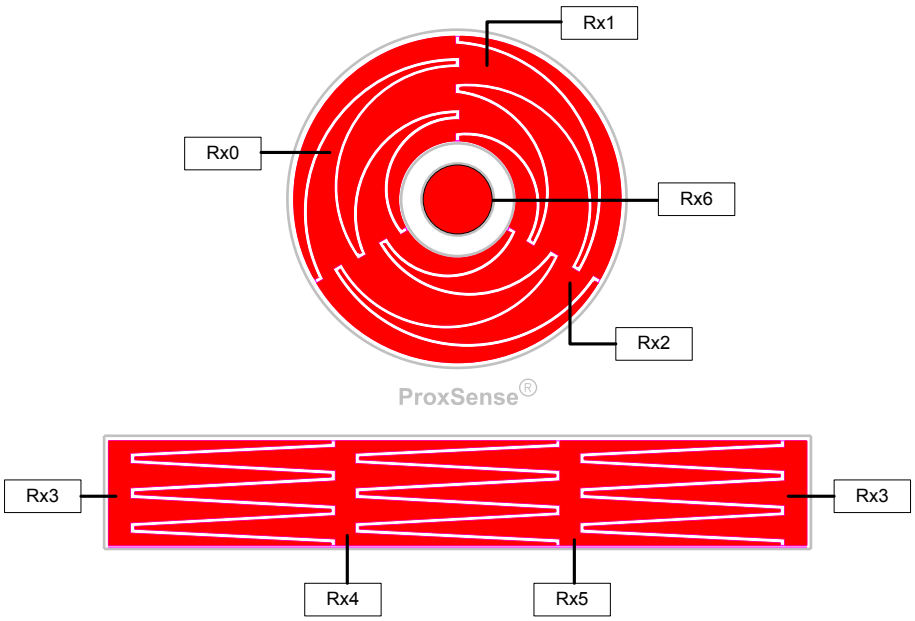
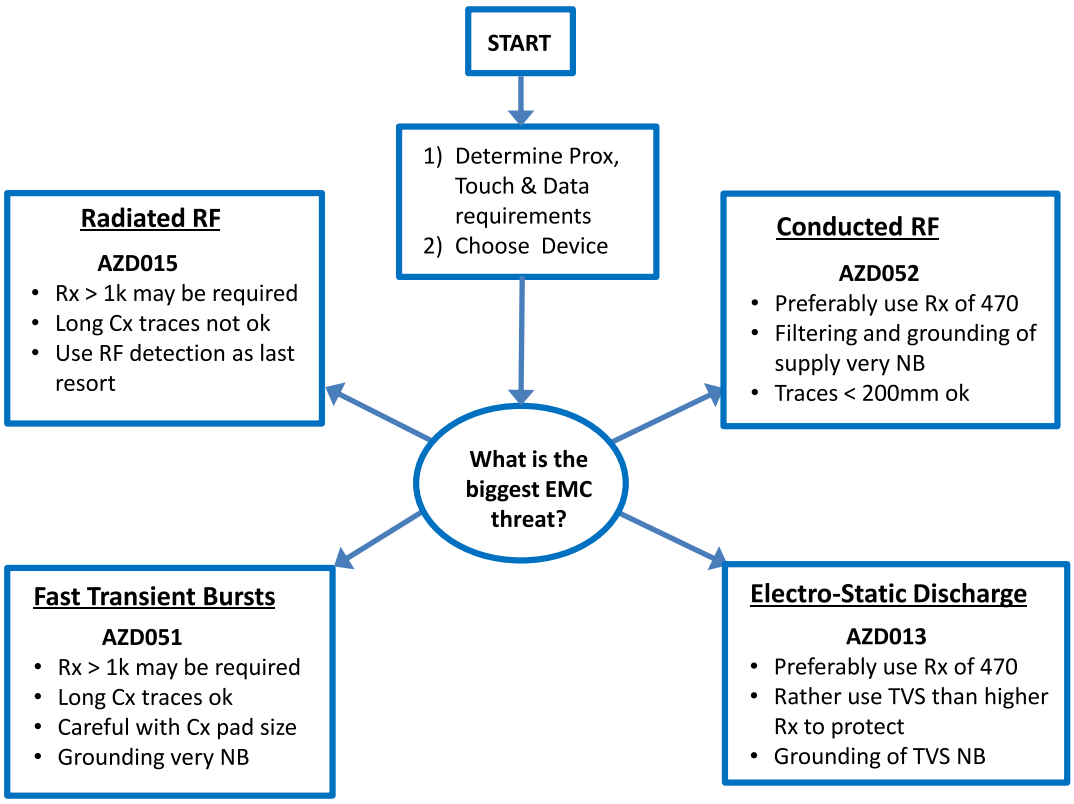


Figure 4.5 Self-Capacitive Wheel, Slider and Button layout guidelines.
DXF files for wheels and sliders are available on request:
info@azoteq.com.

4.3 Power Supply and PCB Layout

Azoteq IC's provide a high level of on-chip hardware and software noise filtering and ESD protection (refer to application note "***AZD013 – ESD Overview***"). Designing PCB's with better noise immunity against EMI, FTB and ESD in mind, it is always advisable to keep the critical noise suppression components like the de-coupling capacitors and series resistors in **Figure 4.2** as close as possible to the IC. Always maintain a good ground connection and ground pour underneath the IC. For more guidelines please refer to the relevant application notes as mentioned in **Section 4.4.**

4.4 Design Rules for Harsh EMC Environments



- ***Applicable application notes: AZD013, AZD015, AZD051, and AZD052.***

4.5 High Sensitivity

Through patented design and advanced signal processing, the device is able to provide extremely high sensitivity to detect proximity. This enables designs to detect proximity at distances that cannot be equaled by most other products. When the device is used in environments where high levels of noise or floating metal objects exist, a reduced proximity threshold is proposed to ensure reliable functioning of the sensor. The high sensitivity also allows the device to sense through overlay materials with low dielectric constants, such as wood or porous plastics.

For more guidelines on the layout of capacitive sense electrodes, please refer to application note ***AZD008***, available on the Azoteq web page: www.azoteq.com.

5 User Configurable Options

The IQS333 requires configuration by a master/host controller or MCU. The user needs to select the number of channels and corresponding touch and proximity thresholds.

5.1 Active Channels

The IQS333 can be configured to have up to 9 active touch channels (CH1-CH9) with one additional proximity channel (CH0) in projected charging mode. By default CH0 is a distributed proximity channel, comprised of charging all the channels together in one timeslot. There is an option to only charge Tx0 (transmitter) and CTRX0 – CTRX2 (receivers) together (see Figure 5.1). by setting the CH0_Settings bit in Register 0x08, byte 6.

The IQS333 can be configured to have up to 7 active touch channels (CH1-CH7) with one additional proximity channel (CH0) in self-capacitive charging mode. CH0 is a distributed proximity channel, comprised of charging all the channels together in one timeslot.

The desired number of channels can be selected in Register 0x0E.

Figure 5.1 illustrates the IQS333 channels mapped to the respective transmit (CTX) and receive (CRX) sense electrodes. Tx0 is used with all three Rx lines to form wheel 1, and Tx1 is used with all three lines to form wheel 2. All three Rx lines are charged together with Tx0 to for the distributed proximity channel (CH0).

Figure 5.2 illustrates the IQS333 channels mapped to the respective CTRX lines in Self capacitive charging mode. CX0 to CX2 forms wheel 1, while CX 3 to CX 5 forms wheel 2. All the channels are charged together to form 1 distributed proximity channel (CH0).

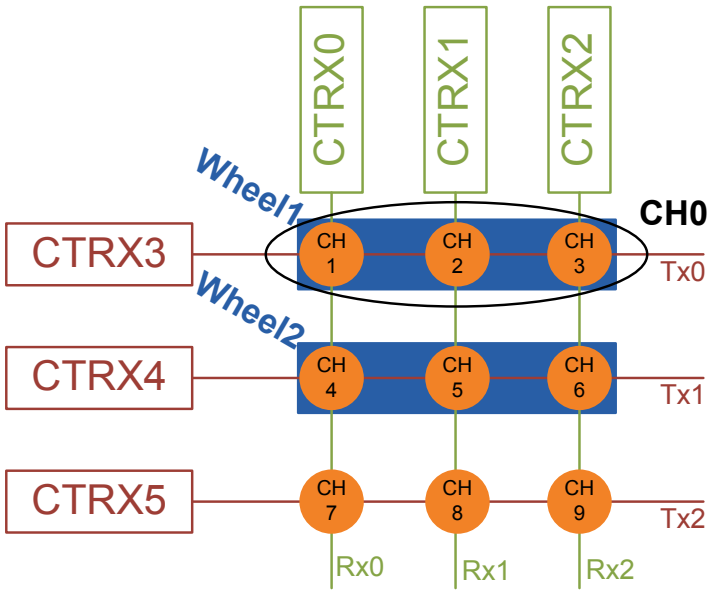


Figure 5.1 IQS333 Channel Mapping in Projected mode.

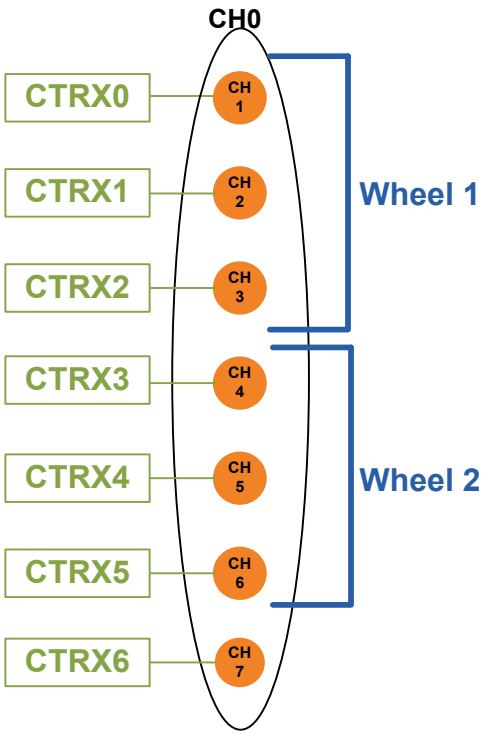


Figure 5.2 IQS333 Channel mapping in Self mode.

5.2 Proximity Threshold

A proximity threshold for channel 0 can be selected by the designer in **Register 0x09**, byte 0, to obtain the desired proximity trigger level. The proximity threshold is selectable between 1 (most sensitive) and 255 (least sensitive) counts. These threshold values (i.e. 1-255) are specified in Counts (CS). Note: The **IQS333** has a default proximity threshold of 4 counts, $P_{THR} = 4$.

5.3 Touch Thresholds

A touch threshold for each channel can be selected by the designer to obtain the desired touch sensitivity and is selectable between 1/256 (most sensitive) to 255/256 (least sensitive). The touch threshold is calculated as a fraction of the Long-Term Average (LTA) given by,

$$T_{THR} = {}^{x}/_{256} \times LTA$$

With lower target values (therefore lower LTA's) the touch threshold will be lower and vice versa.

Individual touch thresholds can be set for each channel (excl. CH0) in **Register 0x09**, byte 1 to 9.

Note: The **IQS333** has a default touch threshold of 16/256*LTA for all active channels.

5.4 Wheel Enable/Disable

The **IQS333** has the option to enable or disable wheel/slider coordinate calculations on 2 wheels. By default, both wheels will be enabled, but can disabled by setting the Wheel_Disable bits in **Register 0x08**, byte 3 (ProxSettings3).

5.5 Wheel Resolution

Both wheels/sliders have resolution up to 11-bit. The resolution can be adjusted between 4-bit and 11-bit, depending on the application requirements and wheel size. The resolution of the wheels cannot be adjusted individually. To adjust the

resolution, set the Resolution bits in Register 0x08, byte 3 (ProxSettings3).

5.6 Wheel Filter

A filter is implemented on both wheels/sliders to smooth the output. This filter can be disabled to increase the response rate by setting the Wheel Filter Disable bit in Register 0x08, byte 3 (ProxSettings3).

5.7 Halt times

The Halt Timer is started when a proximity or touch event occurs and is restarted when that event is removed or reoccurs. When a proximity or touch event condition occurs, the LTA values for all channels will be "halted", thus its values will be kept fixed, until the proximity event is cleared, or the halt timer reaches the halt time. The halt timer will count to the selected halt time (t_{HALT}), which can be configured in Register 0x0A, byte 0. There is also the option to change to never halt or always halt instead of t_{HALT} by setting the HALT bits in Register 0x08, byte 2 (ProxSettings2) When the timer expires, the output will be cleared, and a reseed or re-ATI event will occur (depending on whether the counts are within the ATI band).

It is possible that the CS (Count Value) could be outside the ATI boundary (ATI Target +- 12.5%) when the timer expires, which will cause the device to perform a re-ATI event on that channel and not just a reseed event.

The designer needs to select a halt timer value (t_{HALT}) to best accommodate the required application. The value of t_{HALT} is selectable between 1and 255 (times 250ms). The default value is 0x50H (80 decimal times 250ms = 20 seconds).

There is also the option to set t_{HALT} timer to never halt, or always halt in Register 0x08, byte 2 (Prox_Settings2).

5.8 AC Filter

The AC filter can be implemented to provide better stability of Counts (CS) in electrically noisy environments.

The AC filter also enforces a longer minimum sample time for detecting proximity events on CH0, which will result in a slower response rate when the device enters low power modes. The AC filter can be disabled in Register 0x08, byte 2 (Prox_Settings2).

The AC filter is implemented on all channels, to aid in the slider coordinate calculations, but touch events are determined on unfiltered count values.

5.9 Power Modes

5.9.1 LP Modes

The IQS333 IC has a wide range of configurable low power modes, specifically designed to reduce current consumption for low power and battery applications.

The power modes are implemented around the occurrence of a charge cycle every t_{LP} seconds. The value of t_{LP} is determined by the custom (LP_{value}) value between 1 and 255 in Register 0x0A, byte 2, multiplied by 16ms. Only CH0 is charged during LP, and is forced active (CH0 cannot be disabled). The other active channels will be periodically charged to keep their LTA filter values up to date.

Lower sampling frequencies typically yield significant lower power consumption (but also decreases the response time)

NOTE: While in any power mode the device will zoom to Boost Power (BP) mode whenever the condition (CS – LTA)[1] > PROX_TH or TOUCH_TH holds,

[1] CS-LTA in Projected mode. LTA-CS in Self capacitive sensing mode.

indicating a possible proximity or touch event. This improves the response time. The device will remain in BP for t_{ZOOM} and then return to the selected power mode. The Zoom function allows reliable detection of events with counts being produced at the BP rate. The LP charge cycle timing is illustrated in **Figure 5.3**. The bit0 in **Register 0x01**, byte 0 (Sys_Flags0), will indicate if low power is active, or the device is zoomed in.

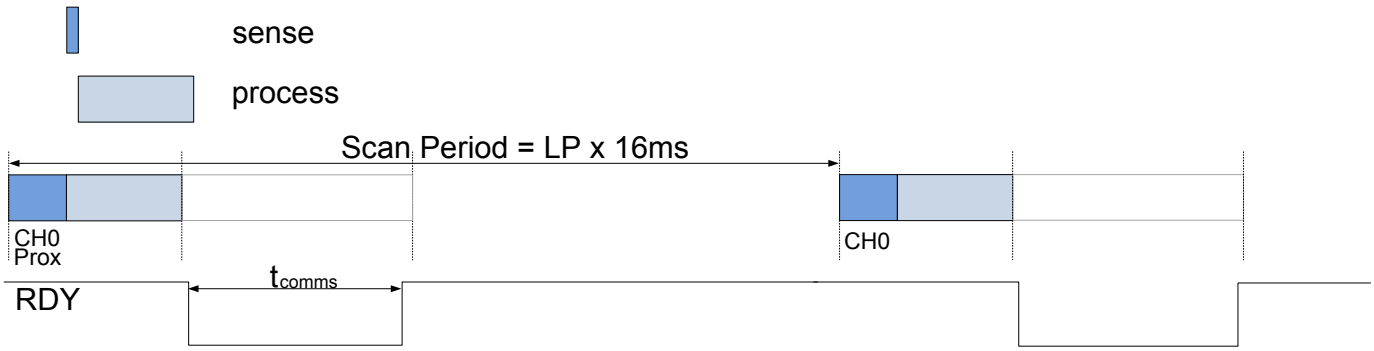


Figure 5.3 IQS333 Charge Cycle Timing in Low Power Mode.

Typical timings of the charge sequence shown above are listed in Table 5.1. These timings are only as reference, as they will differ with each application, depending on the setup of the **IQS333**. For example, the sense (or charge time) is affected by the target counts and charge transfer frequency, while process time is dependent on the turbo mode activation, ATI checking for counts within the pre-set band, filter settings and slider calculations. Communication time is affected by the MCU clock speed and the amount of data read (as well as the sequence thereof) and can be bypassed with using Event Mode. Communication time and the number of active channels will influence the Scan Period. Values shown below are for default settings.

Table 5.1 Typical Timings in LP mode

Typical timings of IQS333		
t_{sense}	900	µs
$t_{process}$	1.4	ms
t_{comms}	6	ms
Scan Period[1]	LP register setting x 16	ms

[1] All channels active, and all data read during communication window. Projected mode, all other settings default.

5.9.2 Turbo Mode

Setting the Turbo Mode bit in **Register 0x08**, byte 1 (Prox_settings1) will enable the **IQS333** device to perform conversions (charge transfers or sensing) as fast as processing and communication allows. Enabling Turbo Mode will maximizing detection speeds, but also increasing current consumption. Disabling Turbo Mode will yield in a fixed sampling period t_{Sample}.

5.10 ATI Method

The **IQS333** can be set up to perform sensor calibration in three ways: Full ATI, Partial ATI and Alternative ATI. The ATI method is selected or turned off in **Register 0x08**, byte 0 (Prox_Settings0).

In **Full ATI** mode, the device automatically selects the multipliers through the ATI algorithm to setup the **IQS333** as close as possible to its default sensitivity for the environment where it was placed.

The user can however, select **Partial ATI**, and set the multipliers to pre-configured values. This will cause the **IQS333** to only calculate the compensation (not the compensation and multipliers as in Full ATI), which allows the freedom to make the **IQS333** more or less sensitive for its intended environment of use. The Partial ATI also reduces start-up and re-ATI times.

In Alternative ATI, the **IQS333** will take the smallest multiplier values from Full ATI, and apply it to all the channels, and the algorithm will determine the compensation values. Special attention should be paid to layout when using Alternative ATI when using a wheel and/or slider, as multipliers for sliders and touch keys are not always in the same range.

5.11 Base Value

The **IQS333** has the option to individually change the base value of each channel during the Full ATI algorithm. Depending on the application, this provides the user with another option to select the sensitivity of the **IQS333** without changes in the hardware (CRX/CTX sizes and routing, etc).

The base values are set in **Register 0x06**, byte 0 to 9 (for channels 0 to 9). The base values can be selected to be **200**(default)**, 75, 100 or 150**.

The base value influences the overall sensitivity of the channel and establishes a base count from where the ATI algorithm starts executing. A lower base value will typically result in a higher sensitivity of the respective channel, as lower multipliers will be selected, and more compensation would be required.

5.12 Target Value

The default target value of the **IQS333** is 512 counts for the touch channels and 1024 counts for the proximity channel.

The target values are calculated by multiplying the value in **Register 0x0B**, byte 0 (for channel 0) & byte 1 (for channels 1 to 9) by 8.

Example: CH0 target = Register Value x 8
= 128(default) x 8 = 1024.

5.13 Charge Transfer Speed

The frequency at which charge cycles are performed can be adjusted by the Charge Xfer Speed bits in **Register 0x08**, byte 1 (Prox_Settings1).

Adjusting the charge transfer speed will change the charge cycle duration (t_{SENSE}) as shown in **Figure 5.3.**

The charge transfer frequency is a fraction of the main oscillator (FOSC = 8MHz) and

can be set at **1MHz** (default)**, 500kHz**, **250kHz** (not recommended for projected) or **2MHz**.

Higher charge transfer speeds are preferred for applications that require increased immunity against aqueous substances.

5.14 C_s Size

Another method to adjust the sensitivity of the **IQS333** is to change the size of the internal C_s capacitor. The size on default is 60pF, but can be changed to 30pF by setting the C_s_Size bit in **Register 0x08**, byte 0 (Prox_Settings0). Choosing the smaller C_s size will effectively reduce the number of counts before ATI, thus changing the multiplier and compensation values required to reach the ATI target.

5.15 Projected Bias

The **IQS333** has the option to change the bias current of the transmitter during projected sensing mode. A larger bias current is required to use larger electrodes, but will also increase the IC power consumption. The bias current is default on 10µA, and can be changed in **Register 0x08**, byte 0 (Prox_Settings0).

5.16 Additional Features

5.16.1 Noise Detect

The **IQS333** has advanced integrated immunity to RF noise sources such as GSM cellular telephones, DECT, Bluetooth and WIFI devices.

Noise detection can be enabled by setting the Noise Detect On bit in **Register 0x08**, byte 1 (Prox_Settings1) and adjusting the trim values.

Connecting a suitable RF antenna and enabling the RF noise detection functionality, will allow the device to identify RF interference and disregard any changes in CS values, blocking changes in touch or proximity status bits if RF noise is detected.

Design guidelines should however be followed to ensure the best noise immunity. Please refer to **Section 7.10.**

5.16.2 Halt Charge

Setting the Halt Charge bit in **Register 0x08**, byte 1 (Prox_Settings1), will stop all conversions.

This function is typically useful for ultra-low power requirements, where the **IQS333** can be controlled by a host MCU and does not require wake-up on proximity or touch events. This is a low power alternative to switching off, where no sensing is required, to avoid resetting the memory map.

5.16.3 Force Halt

The Force Halt bit in **Register 0x08**, byte 2 (Prox_Settings2) can be set to halt all current LTA values and prevent them from being adjusted towards the CS values.

Setting this bit overrides all filter halt settings and prevents the device from performing re-ATI events in cases where the CS values persist outside the ATI boundaries for extended periods of time. Reseed will also not be possible.

5.16.4 CTX / CRX Float

During the charge transfer process, the channels that are not being processed during the current cycle, are effectively grounded to decrease the effects of noise-coupling between the sense electrodes. Grounding these traces is useful in applications with long tracks between IC and sense electrode.

In **Register 0x08**, byte 5, there is the option to specify which channels' transmit and/or receive electrodes to float when they are not charged. This is particularly useful for applications with self-capacitive wheels/sliders with thick overlays, where more sensitivity is required. Sensitivity will be increased when floating the wheel

channels, as they charge in series, and not parallel.

6 ProxSense® Module

The **IQS333** contains a ProxSense® module that uses patented technology to provide detection of proximity and touch conditions on numerous sensing lines.

The ProxSense® module is a combination of hardware and software, based on the principles of charge transfer measurements.

6.1 Charge Transfer Concept

On ProxSense® devices like the **IQS333,** capacitance measurements are taken with a charge transfer process that is periodically initiated.

For projected capacitive sensing, the device measures the capacitance between 2 electrodes referred to as the transmitter (CTX) and receiver (CRX).

The measuring process is referred to as a charge transfer cycle and consists of the following:

- Discharging of an internal sampling capacitor (C_s) and the electrode capacitors (mutual: CTX & CRX) on a channel.
- charging of CTX's connected to the channel
- and then a series of charge transfers from the CRX's to the internal sampling capacitors (C_s), until the trip voltage is reached.

The number of charge transfers required to reach the trip voltage on a channel is referred to as the Current Sample (**CS**) or Count value (Counts).

The device continuously repeats charge transfers on the sense electrodes connected to the CRX pins. For each channel a Long Term Average (**LTA**) is calculated (12 bit unsigned integer values). The count (CS) values (12 bit unsigned integer values) are processed and compared to the LTA to detect Touch and Proximity events.

Please note: Attaching scope probes to the CTX/CRX pins will influence the capacitance of the sense electrodes and therefore the related CS values of those channels. This will have an instant effect on the CS measurements.

6.2 Rate of Charge Cycles

The **IQS333** samples all its active channels (up to 9 + channel 0 for proximity) in 10 timeslots. The charge sequence (as measured on the receive electrodes) is shown in Figure 6.1, where CH0, the Proximity channel, charges first, followed by all other active channels. There is only a communication window after all active channels have been charged.

The charging of CH0 comprises the simultaneous charging of the three receive electrodes (CRX0, CRX1 and CRX2) in conjunction with all transmit electrodes, thus realising a distributed load mutual capacitive sense electrode. Refer to **Figure 5.1** for **IQS333** channel numbering. The user has the option to only charge 1 Tx (Tx0/CTRX3) together with all 3 receivers, by setting the 1 Tx bit in **Register 0x08**, byte 1 (Prox_Settings1).

In self-capacitive mode, CH0 is also a distributed channel charging all 7 CX channels together.

6.2.1 Boost Power rate

With the **IQS333** zoomed to Boost Power (BP) mode, the active channels are charged at a fixed sampling period (t_{SAMPLE}) per channel (if Turbo Mode is not enabled). This is done to ensure regular samples for

processing of results, and fix timings for the halt times.

It is calculated as each channel having a time t_{SAMPLE} = charge/conversion time (t_{SENSE}) + computation time ($t_{PROCESS}$) of approximately t_{SAMPLE} = 1.6ms. Thus the time between consecutive samples on a specific channel (Scan Period) will depend on the number of enabled channels and the length of communication between the **IQS333** and the host MCU. Communication will always happen after processing of the last active channel. Due to processing and charging happening in parallel, CH0 will charge while the last active channel is processed. Therefore, communication windows will always be after CH0 has charged.

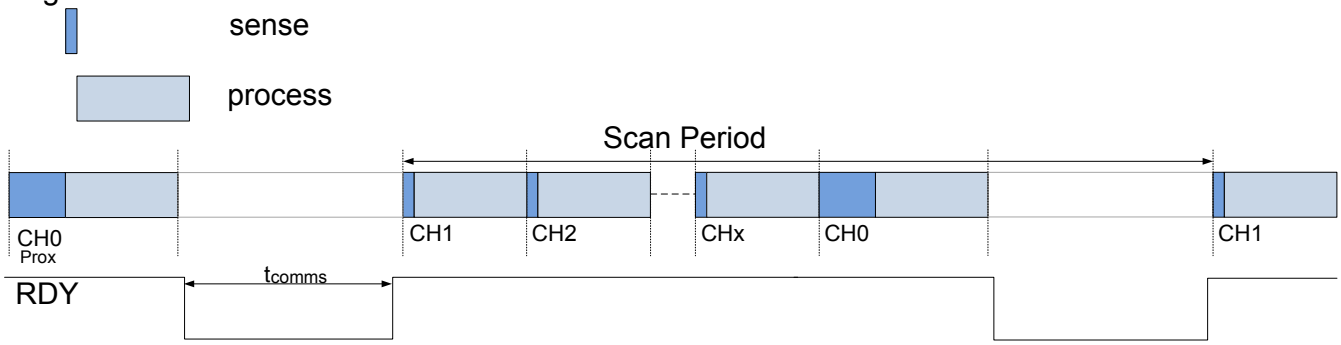


Figure 6.1 IQS333 Charge Sequence timing diagram in Boost Power mode.

Typical timings of the charge sequence shown above are listed in Table 6.1. These timings are only as reference, as they will differ with each application, depending on the setup of the **IQS333**. For example, the sense (or charge time) is affected by the target counts and charge transfer frequency, while process time is dependent on the turbo mode activation, ATI checking for counts within the pre-set band, filter settings and slider calculations. Communication time is affected by the MCU clock speed and the amount of data read (as well as the sequence thereof) and can be bypassed with using Event Mode. Communication time and the number of active channels will influence the Scan Period. Values shown below are for default settings.

Table 6.1 Typical Timings

Typical timings of IQS333		
t_{sense}	600	µs
$t_{process}$	1.4	ms
t_{comms}	6	ms
Scan Period[1]	26	ms

[1] All channels active, and all data read during communication window. Projected mode, all other settings default.

6.2.2 Low Power rate

A wide range of low current consumption charging modes is available on the **IQS333**.

In any Low Power (LP) mode, there will be an applicable low power time (t_{LP}). This is determined by **Register 0x0A**, byte 1. The value written into this register multiplied by 16ms will yield the LP time (t_{LP}).

With the detection of an undebounced proximity event the IC will zoom to BP mode, allowing a very fast reaction time for further possible touch events.

During any LP mode, only channel 0 is charged every t_{LP}. The LP charge timing is illustrated in **Figure 5.3.**

If a low power rate is selected and charging is not in the zoomed state (BP mode), the low power active bit (Register 0x01) will be set.

Please refer to **Section 5.9.**

6.3 Touch report Rate

During Boost Power (BP) mode, the touch report rate of the **IQS333** device depends on the charge transfer frequency, the number of channels enabled and the length of communications performed by the host MCU or master device.

Several factors may influence the touch report rate:

- **Enabled channels:** Disabling channels that are not used will not only increase the touch report rate, but will also reduce the device's current consumption.
- **Turbo Mode:** See **Section 5.9.2**
- **Target Values:** Lower target values requires shorter charge transfer times (t_{SENSE}), thus reducing the SCAN PERIOD and increasing the touch report rate.
- **Charge Transfer Speed:** Increasing the charge transfer frequency will reduce the conversion time (t_{SENSE}) and increase the touch report rate.
- **ACF:** Disabling the AC filter and wheel/slider position calculations will reduce the processing time ($t_{PROCESS}$) and yield a faster report rate.

6.4 Long Term Average

The Long-term Average (LTA) filter can be seen as the baseline or reference value. The LTA is calculated to continuously adapt to any environmental drift. The LTA filter is calculated from the CS value for each channel. The LTA filter allows the device to adapt to environmental (slow moving) changes/drift. Actuation (Touch or Prox) decisions are made by comparing the CS value with the LTA reference value.

The 12bit LTA values are contained in **Register 0x05**. Low bytes first, from CH0 up to CH9 (18 bytes in total).

Please refer to **Section 5.7** for LTA Halt Times.

6.5 Determine Touch or Prox

An event is determined by comparing the CS value with the LTA. Since the CS reacts differently when comparing the self- with the mutual capacitance technology, the user should consider only the conditions for the technology used.

An event is recorded if:

- Self: CS < LTA – **Threshold**
- Projected: CS > LTA + **Threshold**

Threshold can be either a Proximity or Touch threshold, depending on the current channel being processed.

Note that a proximity condition will be forced enabled if there is a touch condition on any channel.

Please refer to **Section 1.1** and **5.3** for proximity and touch threshold selections.

6.6 ATI

The **A**utomatic **T**uning **I**mplementation (**ATI**) is a sophisticated technology implemented on the new ProxSense® series devices. It allows for optimal performance of the devices for a wide range of sense electrode capacitances, without modification or addition of external components.

The ATI allows the tuning of two parameters, an ATI Multiplier and an ATI Compensation, to adjust the Count values for an attached sense electrode.

ATI allows the designer to optimize a specific design by adjusting the sensitivity and stability of each channel through the adjustment of the ATI parameters.

The **IQS333** has a full ATI function. The full-ATI function is default enabled, but can be disabled by setting the ATI_OFF bit, or changed to partial or alternative ATI by setting the ATI_Partial and ATI_ALT bits in **Register 0x08**, byte 0.

The ATI_Busy bit in **Register 0x01**, byte 0 (Sysflags0) will be set while an ATI event is busy.

For more information regarding the ATI algorithm, please contact Azoteq at: ProxSenseSupport@azoteq.com

6.6.1 ATI Sensitivity

On the **IQS333** device, the user can specify the BASE value (**Section 5.11**) for each channel individually and the TARGET values (**Section 5.12**) for the proximity (CH0) and touch (CH1-CH9) channels.

A rough estimation of sensitivity can be calculated as:

$$Sensitivity = \frac{TARGET}{BASE}$$

As can be seen from this equation, the sensitivity can be increased by either increasing the Target value or decreasing the Base value. It should, however, be noted that a higher sensitivity will yield a higher noise susceptibility.

6.6.2 ATI Target

The target value is reached by adjusting the COMPENSATION bits for each channel (ATI target limited to 4096 counts).

The target value is written into the respective channel's TARGET registers. The value written into these registers multiplied by 8 will yield the new target value. (Please refer to **Section 5.12**)

6.6.3 ATI Base (Multiplier)

The following parameters will influence the base value:

- C_s_SIZE[1]: Size of sampling capacitor.
- PROJ_BIAS bits: Adjusts the biasing of some analogue parameters in the mutual capacitive operated IC. (Only applicable in mutual capacitance mode.)
- Charge Transfer Frequency
- MULTIPLIER bits.

The base value used for the ATI function can be implemented in 2 ways:

1. ATI_PARTIAL = 0. ATI automatically adjusts MULTIPLIER bits to reach a selected base value[2]. Please refer to **Section 5.11** for available base values.

[1] Changing CS_SIZE if ATI_OFF = 0 will change CS

[2] ATI function will use user selected CS_SIZE and PROJ_BIAS (if applicable) and will only adjust the MULTIPLIER bits to reach the base values.

2. ATI_PARTIAL = 1. The designer can specify the multiplier settings. These settings will give a custom base value from where the compensation bits will be automatically implemented to reach the required target value. The base value is determined by two sets of multiplier bits. Sensitivity Multipliers which will also scale the compensation to normalise the sensitivity and Compensation Multipliers to adjust the gain.

6.6.4 Re-ATI

An automatic re-ATI event will occur if the counts are outside its re-ATI limits. The re-ATI limit or ATI boundary is calculated as the target value divided by 8. For example:

- Target = 512, Re-ATI will occur if CS is outside 512±64.

A re-ATI event can also be issued by the host MCU by setting the REDO_ATI bit in **Register 0x08**, byte0 (ProxSettings0). The REDO_ATI bit will clear automatically after the ATI event was started.

Note: Re-ATI will automatically clear all proximity, touch and halt status bits.

6.6.5 Reseed

Setting the Reseed bit in **Register 0x08**, byte 0), will shift all LTA filters to a value of LTA_{new} = CS + 8 (CS – 8 for Self). The LTA will then track the CS value until they are even.

Performing a reseed action on the LTA filters, will effectively clear any proximity and/or touch conditions that may have been established prior to the reseed call.

6.6.6 Alternative ATI

The Alternative ATI implementation ensures that all the multiplier values are identical for all the channels and adjusts only the compensation in order to achieve the desired count value. The multipliers are selected from the channel with the smallest multipliers according to the full ATI algorithm. Alternative ATI can be enabled in **Register 0x08**, byte 0.

6.6.7 ATI ERROR

The ATI error bit (read only) in **Register 0x08**, byte 1 (Prox_Settings1) indicates to the user that the ATI targets where not reached. Adjustments of the base values or ATI BANDs are required.

6.6.8 ATI Band

The user has the option to select the re-ATI band as 1/8 of the ATI target (default) or ¼ of the ATI target counts by setting the ATI BAND bit in **Register 0x08**, byte 1 (Prox_Settings1).

7 Communication

The **IQS333** device interfaces to a master controller via a 3-wire (SDA, SCL and RDY) serial interface bus that is I^2C^{TM} compatible, with a maximum communication speed of 400kbit/s.

7.1 Control Byte

The Control byte indicates the 7-bit device address (64H default) and the Read/Write indicator bit. The structure of the control byte is shown in Figure 7.1.

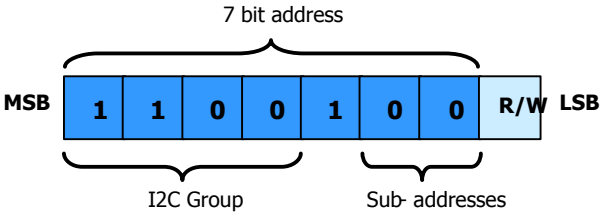


Figure 7.1 IQS333 Control Byte.

The I²C device has a 7 bit Slave Address (default 0x64H) in the control byte as shown in Figure 7.1. To confirm the address, the software compares the received address with the device address. Sub-address values can be set by OTP programming options.

7.2 I²C Read

To read from the device a *current address read* can be performed. This assumes that the address-command is already setup as desired.

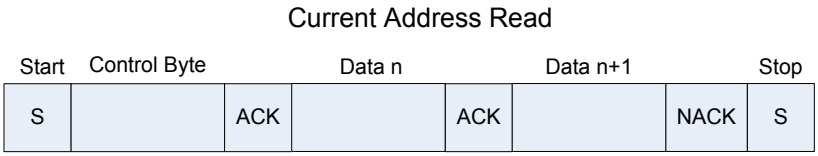


Figure 7.2 Current Address Read.

If the address-command must first be specified, then a *random read* must be performed. In this case a WRITE is initially performed to setup the address-command, and then a repeated start is used to initiate the READ section.

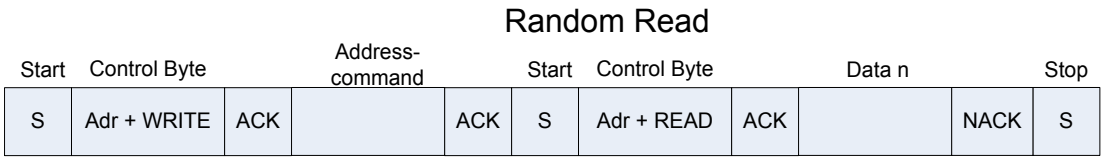


Figure 7.3 Random Read.

7.3 I²C Write

To write settings to the device a *Data Write* is performed. Here the Address-Command is always required, followed by the relevant data bytes to write to the device.

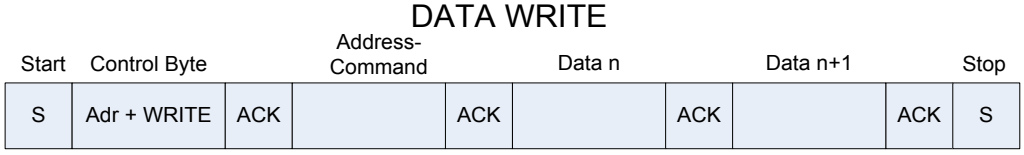


Figure 7.4 I²C Write.

7.4 End of Communication Session / Window

Similar to other Azoteq I²C devices, to end the I²C communication session, a STOP command is given. When sending numerous read and write commands in one communication cycle, a repeated start command must be used to stack them together (since a STOP will jump out of the communication window, which is not desired).

The STOP will then end the communication, and the **IQS333** will return to process a new set of data. Once this is obtained, the communication window will again become available (RDY set LOW).

7.5 I²C Sub-address

The **IQS333** has four available sub addresses, 64H (default) to 67H, which allows up to four devices on a single I²C bus.

7.5.1 Internal sub-address selection

Selecting the sub-address via OTP bits allows the user 4 different options:

Table 7.1 I²C sub-address selection

FG25	FG26	Device Address
0	0	0x64
0	1	0x65
1	0	0x66
1	1	0x67

7.6 Event Mode

By default the device operates in full streaming mode. There is an option for an event-driven I²C communication mode (also called “Event Mode”), with the RDY pin ONLY indicating a communication window after a prescribed event has occurred.

These events include:

- Proximity events
- Touch events
- ATI events
- Noise events (Noise detect enabled)

If the wheels/sliders are enabled, the device will stream data continuously when a touch is present on one of the wheel/slider channels, even if Event Mode is enabled.

Event Mode can be enabled by setting the Event_Mode bit in **Register 0x08**, byte 2 (Prox_Settings2).

Note: The device is also capable of functioning **without** a RDY line on a polling basis.

7.7 RDY Hand-Shake Routine

The master or host MCU has the capability to force a communication window at any time, by pulling the RDY line low. The communication window will open directly following the current conversion cycle.

7.8 I²C Specific Commands

7.8.1 Show Reset

The SHOW_RESET bit can be read in **Register 0x01**, byte 1 (Sysflags0), to determine whether a reset has occurred on the device. This bit will be set ’1’ after a reset. A reset can be forced by writing the Soft_Reset bit in **Register 0x08**, byte 2 (ProxSettings2).

The SHOW_RESET bit will be cleared (set to ’0’) by writing a ’1’ into the ACK_RESET bit in **Register 0x08**, byte 3 (ProxSettings3). A reset will typically take place if a timeout during communication occurs.

7.8.2 WDT disable

The WDT (watchdog timer) is used to reset the IC if a problem (for example a voltage spike) occurs during communication. The WDT will time-out (and thus reset the device) after t_{WDT} if no valid communication occurred during this time.

The WDT can be disabled by setting the WDT Off bit in **Register 0x08**, byte 2 (ProxSettings2).

7.8.3 Timeout Disable

If no communication is initiated from the master/host MCU within the first t_{COMMS} (t_{COMMS} = 20ms) of the RDY line indicating that data is available (i.e. RDY = low), the device will resume with the next cycle of charge transfers and the data from the previous conversions will be lost.

This time-out function can be disabled by setting the TIME_OUT DISABLE bit in **Register 0x08**, byte 2 (ProxSettings2).

7.8.4 Soft Reset

The user has the option to do a soft reset on the **IQS333.** The soft reset will clear all the registers (the device will restart as with POR) except the PWM register will keep their state.

A soft reset is initiated by setting the bit in **Register 0x08**, byte 2 (Prox_Settings2). The bit Soft Reset bit will automatically clear after the command is sent.

7.9 I²C I/O Characteristics

The **IQS333** requires the input voltages given in **Table 7.2**, for detecting high ("1") and low ("0") input conditions on the I²C communication lines (SDA, SCL and RDY).

Table 7.2 IQS333 I²C Input voltage

	Input Voltage (V)
Vin_{LOW}	0.3*VDDHI
Vin_{HIGH}	0.7*VDDHI

Table 7.3 provides the output voltage levels of the **IQS333** device during I²C communication.

Table 7.3 IQS333 I²C Output voltage

	Output Voltage (V)
$Vout_{LOW}$	VSS +0.2 (max.)
$Vout_{HIGH}$	VDDHI – 0.2 (min.)

7.10 PWM Controller

The **IQS333** incorporates a highly configurable PWM controller to implement user configurable LED lighting displays. The various PWM control modes can be easily configured with an I^2C interface by writing directly to the control bytes in the memory map. There are 8 identical PWM modules with 15.625kHz PWM carrier frequency which can be controlled independently to allow for a wide range of user configurable options

7.11 PWM Diming modes

The hardware PWM channels can be controlled through the memory map various diming modes. These include:

- Incrementing to 100%
- Incrementing to a set level
- Decrementing to 0%
- Decrementing to a set level

The speed of the dimming modes is also configurable.

7.12 PWM Duty Cycle Mapping

Although there are only 5 PWM bits in the MM, the resolution of the PWM engine is effectively 6 bits to ensure a more linear increase in LED brightness. A 6 bit internal timer is compared to a PWM value comprised of the Duty Cycle bits CMP4:0 in Register 0x0C, bytes 0 to 7.

Table 7.4 PWM Duty Cycle Mapping

CMP4:0	PWM Timer Count	PWM DUTY
0	0	0.00%
1	1	1.56%
2	2	3.13%
3	3	4.69%
4	4	6.25%
5	5	7.81%
6	6	9.38%
7	7	10.94%
8	8	12.50%
9	9	14.06%
10	10	15.63%
11	11	17.19%
12	12	18.75%
13	13	20.31%
14	14	21.88%
15	15	23.44%
16	16	25.00%
17	18	28.13%
18	20	31.25%
19	22	34.38%
20	24	37.50%
21	26	40.63%
22	28	43.75%
23	30	46.88%
24	32	50.00%
25	36	56.25%
26	40	62.50%
27	44	68.75%
28	48	75.00%
29	52	81.25%
30	56	87.50%
31	64	100.00%

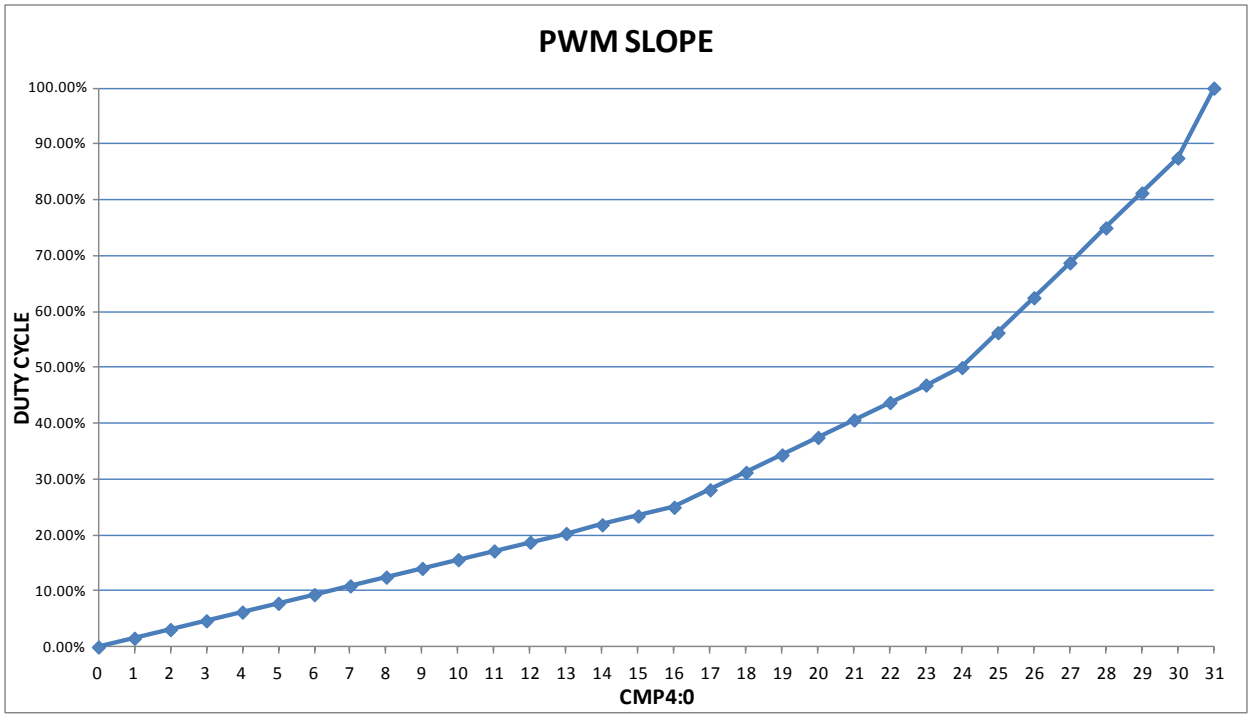


Figure 7.5 PWM Slope.

8 RF Noise

8.1 RF Noise Detection

In cases of extreme RF interference, enabling the **IQS333** on-chip RF detection is suggested.

The RF Noise Detection can be enabled by setting the Noise Detect On bit in **Register 0x08**, byte 1 (ProxSettings1).

By connecting a suitable antenna to the RF pin (pin 19), it allows the device to detect RF noise and notify the master of possible corrupt data. Noise affected samples are not allowed to influence the LTA filter, and also do not contribute proximity or touch detection. With the detection of RF noise, the RF NOISE bit in **Register 0x01**, byte 0 (Sysflags2) will be set.

8.1.1 RF Detector Sensitivity

The sensitivity of the RF detector can be selected by setting an appropriate RF detection voltage through the ND_TRIM bits in **Register 0x08**, byte 1 (ProxSettings1). Please see application note: "***AZD015: RF Immunity and detection in ProxSense devices***" for further details regarding this option.

8.2 RF Noise Immunity

The **IQS333** has advanced immunity to RF noise sources such as GSM cellular telephones, DECT, Bluetooth and WIFI devices. Design guidelines should however be followed to ensure the best noise immunity on a hardware level.

In general, the design of capacitive sensing applications may encompass a large range of configurations; however, following the guidelines in **Section 8.2.1** may improve a capacitive sensing design.

8.2.1 Notes for layout:

- A ground plane should be placed under the IC, except under the CRX lines.
- Place the sensor IC as close as possible to the sense electrodes.

- All the tracks on the PCB must be kept as short as possible.
- The capacitor between VDDHI and GND as well as between VREG and GND must be placed as close as possible to the IC.
- A 100 pF capacitor can be placed in parallel with the 1uF capacitor between VDDHI and GND. Another 100 pF capacitor can be placed in parallel with the 1uF capacitor between VREG and GND.
- When the device is too sensitive for a specific application a parasitic capacitor (max 5pF) can be added between the CX line and ground.
- Proper sense electrode and button design principles must be followed.
- Unintentional coupling of sense electrodes to ground and other circuitry must be limited by increasing the distance to these sources.
- In some instances a ground plane some distance from the device and sense electrode may provide significant shielding from undesirable interference.
    - However, if after proper layout, interference from an RF noise source persists, please refer to application note: "***AZD015: RF Immunity and detection in ProxSense devices***".

9 Communication Command/Address Structure

9.1 Registers

Table 9.1 IQS333 Registers

Address	Description	Access	Section
0x00H	**Device Information**	R	9.2.1
0x01H	**System Flags**	R	9.2.2
0x02H	**Wheel Coordinates**	R	9.2.3
0x03H	**Touch Bytes**	R	9.2.4
0x04H	**Counts**	R	9.2.5
0x05H	**LTA**	R	9.2.6
0x06H	**Multipliers**	R/W	9.2.7
0x07H	**Compensation**	R/W	9.2.8
0x08H	**ProxSettings**	R/W	9.2.9
0x09H	**Thresholds**	R/W	9.2.10
0x0AH	**Timings**	R/W	9.2.11
0x0BH	**Targets**	R/W	9.2.12
0x0CH	**PWM Duty**	R/W	9.2.13
0x0DH	**PWM LIM**	R/W	9.2.14
0x0EH	**Active Channels**	R/W	9.2.15
0x0FH	**Buzzer**	R/W	9.2.16

9.2 Registers Descriptions

9.2.1 Device Information 0x00H

Information regarding the device type and version is recorded here. Any other information specific to the device version can be stored here. Each Azoteq ROM has a unique Product- and Version number.

Access	Bit	Product Number (PROD_NUM)							
		7	6	5	4	3	2	1	0
R	Value	54 (Decimal)[1]							

Access	Bit	Version Number (VERSION_NUM)							
		7	6	5	4	3	2	1	0
R	Value	02 (Decimal)							

9.2.2 System Flags 0x01H

Access	Bit	System Flags (SYSFLAGS0)							
		7	6	5	4	3	2	1	0
R	Name	Show reset	Filter Halted	Proj Mode	Is Ch0	LP Active	ATI Busy	Noise detected	Zoom

9.2.3 Wheel Coordinates 0x02H

Access	Bit	Wheel 1 Low							
		7	6	5	4	3	2	1	0
R	Name	Wheel 1 Coordinate Low byte first							

Access	Bit	Wheel 1 High							
		7	6	5	4	3	2	1	0
R	Name	Wheel 1 Coordinate High byte							

Access	Bit	Wheel 2 Low							
		7	6	5	4	3	2	1	0
R	Name	Wheel 2 Coordinate Low byte first							

[1] Product and Version numbers are 32 14 for QFN20 devices – alpha customers only

		Wheel 2 High							
Access	Bit	7	6	5	4	3	2	1	0
R	Name	Wheel 2 Coordinate High byte							

9.2.4 Touch Bytes 0x03H

		Touch Byte 0							
Access	Bit	7	6	5	4	3	2	1	0
R	Name	CH7	CH6	CH5	CH6	CH3	CH2	CH1	

		Touch Byte 1							
Access	Bit	7	6	5	4	3	2	1	0
R	Name							CH9	CH8

9.2.5 Counts 0x04H

This register has 18 bytes to store the count values of CH0 up to CH9 the low byte will always read out first, followed by the high byte, before the moving to the next channel.

		CH0 Low							
Access	Bit	7	6	5	4	3	2	1	0
R	Name	Channel 0 CS (Counts) Low byte first							

		CH n High							
Access	Bit	7	6	5	4	3	2	1	0
R	Name	Last active channel, Count value (High byte last)							

9.2.6 LTA 0x05H

This register has 18 bytes to store the LTA values of CH0 up to CH9 the low byte will always read out first, followed by the high byte, before the moving to the next channel.

Access	Bit	CH0 LTA Low byte							
		7	6	5	4	3	2	1	0
R	Name								

Access	Bit	CH n LTA High byte							
		7	6	5	4	3	2	1	0
R	Name								

9.2.7 Multipliers 0x06H

Access	Bit	CH0 Multipliers							
		7	6	5	4	3	2	1	0
R	Name	Base Value		Comp Multipliers		Sensitivity Multipliers			

Access	Bit	CH n Multipliers							
		7	6	5	4	3	2	1	0
R	Name	Base Value		Comp Multipliers		Sensitivity Multipliers			

9.2.8 Compensation 0x07H

Access	Bit	CH0 Compensation value							
		7	6	5	4	3	2	1	0
R/W	Name	Channel 0 Compensation							
Byte 0									

Access	Bit	CH n Compensation Value							
		7	6	5	4	3	2	1	0
R/W	Name	Last active channel Compensation							
Byte n									

9.2.9 ProxSettings 0x08H

		ProxSettings0							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Name	ATI OFF	Partial ATI	ALT ATI	Redo ATI	Reseed	C_s Size	Proj Bias	
Byte 0	Default	0x06H							

Bit 1:0: 00 = 2.5µA
01 = 5µA
= 10µA (default)
= 20µA

		ProxSettings1							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Name	Charge Transfer Speed		Turbo Mode	Halt Charge	Noise Detect	CH0 on 1Tx	Error	Band
Byte 1	Default	0x00H							

Bit 7:6: 00 = 1MHz
01 = 500kHz
10 = 250kHz
11 = 2MHz

		ProxSettings2							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Name	Soft Reset	WDT Off	Force Halt	ACF Disable	Timeout Disable	Event Mode	Halt	
Byte 2	Default	0x00H							

Bit 1:0: 00 = Fhalt period
01 = Never
10 = Always

Access	Bit	ProxSettings3							
		7	6	5	4	3	2	1	0
R/W	Name		Wheel Resolution			Wheel Filter Disable	Wheel2 Disable	Wheel1 Disable	ACK Reset
Byte 3	Default	0x00H							

Access	Bit	ProxSettings4							
		7	6	5	4	3	2	1	0
R/W	Name		Up			Up Enable	Pass		
Byte 4	Default	0x07H							

Access	Bit	ProxSettings5							
		7	6	5	4	3	2	1	0
R/W	Name	CTRX_VSS							
Byte 5	Default	0x7FH							

9.2.10 Thresholds 0x09

Access	Bit	Proximity Threshold							
		7	6	5	4	3	2	1	0
R/W	Name	Value							
Byte 0	Default	0x04H							

Access	Bit	Touch Threshold CH1							
		7	6	5	4	3	2	1	0
R/W	Name	(Value/256)*LTA							
Byte 1	Default	0x10H							

Access	Bit	Touch Threshold CH9							
		7	6	5	4	3	2	1	0
R/W	Name	(Value/256)*LTA							
Byte 9	Default	0x10H							

9.2.11 Timings 0x0AH

Access	Bit	Filter Halt (t_HALT)							
		7	6	5	4	3	2	1	0
R/W	Name	Steps of 250ms							
Byte 0	Default	0x50H							

Access	Bit	Power Mode (LP)							
		7	6	5	4	3	2	1	0
R/W	Name	Steps of 16ms							
Byte 1	Default	0x00H							

Access	Bit	Timeout Period							
		7	6	5	4	3	2	1	0
R/W	Name	Steps of 1.28ms							
Byte 2	Default	0x10H							

Access	Bit	CH0 ACF Beta							
		7	6	5	4	3	2	1	0
R/W	Name	Value							
Byte 3	Default	0x02H							

		CH1 – CH9 ACF Beta							
Access	**Bit**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R/W	**Name**	Value							
Byte 4	**Default**	0x02H							

9.2.12 ATI Targets 0x0BH

		ATI Target CH0							
Access	**Bit**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R/W	**Name**	Steps of 8							
Byte 0	**Default**	128 (Decimal)							

		ATI Targets CH1 to CH 9							
Access	**Bit**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R/W	**Name**	Steps of 8							
Byte 1	**Default**	64 (Decimal)							

9.2.13 PWM 0x0CH

		PWM 0							
Access	**Bit**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R/W	**Name**	Mode			Duty Cycle				
Byte 0	**Default**	0x00H							

		PWM 7							
Access	**Bit**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R/W	**Name**	Mode			Duty Cycle				
Byte 3	**Default**	0x00H							

Bit 7-5: ***MODE2:MODE0:*** Selects PWM mode.

000 = PWM Off

001 / 010 / 011 = PWM Constant

100 = PWM CMP4:0 decremented and stops at 0%

101 = PWM CMP4:0 decremented and stops at value in PWM_LIM

110 = PWM CMP4:0 incremented and stops at 100%

111 = PWM CMP4:0 incremented and stops at value in PWM_LIM

Bit 4-0: **CMP4:CMP0:** LED Duty Cycle Value

9.2.14 PWM Limit 0x0DH

		PWM Lim							
Access	**Bit**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R/W	**Name**				PWM Limit				
Byte 0	**Default**	0x00H							

Bit 7-5: ***System Use***

Bit 4-0: ***LIM4:LIM0:*** CMP 4:0 is compared against this value if MODE 2:0 is configured 101 or 111

		PWM Speed							
Access	**Bit**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R/W	**Name**					PWM Speed			
Byte 1	**Default**	0x00H							

Bit 7-4: ***System Use***

Bit 3-0: ***SPD3:SPD0:*** PWM slope adjustment speed control

$$PWM\ Timing = SPD3{:}0 \times [CMP4{:}0 + 1] \times 8.192ms$$

Example:

SPD3:0 = 0100

CMP4:0 = 11111 (PWM Duty = 100%)

$$Ton = 4 \times [31 + 1] \times 8.192ms = 1.0486s$$

9.2.15 Active Channels 0x0EH

		Active Chan 0							
Access	**Bit**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R/W	**Name**	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
Byte 0	**Default**	0x0FH							

		Active Chan 1							
Access	**Bit**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R/W	**Name**							CH9	CH8
Byte 1	**Default**	0x00H							

9.2.16 Buzzer Output 0x0FH

		Buzzer 0							
Access	**Bit**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R/W	**Name**	Enable					DC	PERM	Burst
Byte 0	**Default**	0x00H							

This Byte sets up the Buzzer as shown below:

Bit 7: ***Enable:*** This bit enables or Disables the Buzzer output

0 = Disabled

1 = Enabled

Bit 6-3: ***Not Used***

Bit 2: ***DC*****:** Makes a DC output

0 = Low

1 = High

Bit 1: ***Perm*****:** Permanently sounding the buzzer

0 = Disabled

1 = Enabled

Bit 0: ***Burst*****:** Burst mode to make a “click” sound

0 = Disabled

1 = Enabled

10 IQS333 OTP Options

The **IQS333** only provide OTP (**O**ne-**T**ime **P**rogrammable) options for configuration of the device I²C sub-address and charge transfer methodology (Self/Projected sensing).

Configuration of the OTP settings can be done on packaged devices or in-circuit. In-circuit configuration may be limited by values of external components chosen.

Azoteq offers a Configuration Tool (CT210 or later) and associated software that can be used to program the OTP user options for prototyping purposes. For further information regarding this subject, please contact your local distributor or submit enquiries to Azoteq at: ProxSenseSupport@azoteq.com

10.1 User Selectable OTP options

Table 10.1 User Selectable OTP options : Bank3

bit7	Bank 3						bit0
System use	System use	System use	System use	Proj_Mode	I²C SubAddr1	I²C SubAddr0	System use

Bank3: bit7	**System Use**
Bank3: bit6	**System Use**
Bank3: bit5	**System Use**
Bank3: bit4	**System Use**
Bank3: bit 2:1	**Proj_Mode : Projected Selection**
	0 = Self (Default) 1 = Projected
Bank3: bit 2:1	**I²C SubAddr1: I²C SubAddr0 : I²C Sub-Address selection**
	00 = 0x64 (Default) 01 = 0x65 10 = 0x66 11 = 0x67
Bank3: bit 0	**System Use**

11 Specifications

11.1 Absolute Maximum Specifications

The following absolute maximum parameters are specified for the device:

Exceeding these maximum specifications may cause damage to the device.

- Operating temperature: -40°C to 85°C
- Supply Voltage (VDDHI – VSS): 3.6V
- Maximum pin voltage: VDDHI + 0.5V (may not exceed VDDHI max)
- Maximum continuous current (for specific Pins): 10mA
- Minimum pin voltage: VSS - 0.5V
- Minimum power-on slope: 100V/s
- ESD protection: ±8kV (Human body model)
- Package Moisture Sensitivity Level (MSL): 2

Table 11.1 IQS333 Self Capacitive General Operating Conditions[1]

DESCRIPTION	Conditions	PARAMETER	MIN	TYP	MAX	UNIT
Supply voltage		V_{DDHI}	1.8	3.3V	3.6	V
Internal regulator output	$1.8 \leq V_{DDHI} \leq 3.6$	V_{REG}	1.62	1.7	1.79	V
Default Operating Current	3.3V	$I_{IQS333NP}$	-	360		µA
Low Power Setting 1*	3.3V, LP=32	$I_{IQS333LP32}$	-	<6		µA
Low Power Setting 2*	3.3V, LP=128	$I_{IQS333LP128}$	-	<4		µA
Low Power Setting 3*	3.3V, LP=256	$I_{IQS333LP256}$	-	<3		µA

*LP interval period = Low power value x 16ms

Table 11.2 IQS333 Projected Capacitive General Operating Conditions

DESCRIPTION	Conditions	PARAMETER	MIN	TYP	MAX	UNIT
Supply voltage		V_{DDHI}	1.8	3.3V	3.6	V
Internal regulator output	$1.8 \leq V_{DDHI} \leq 3.6$	V_{REG}	1.62	1.7	1.79	V
Default Operating Current	3.3V	I_{IQS333}	-	530		µA

[1]Operating current shown in this datasheet, does not include power dissipation through I^2C pull up resistors.

DESCRIPTION	Conditions	PARAMETER	MIN	TYP	MAX	UNIT
Low Power Setting 1*	3.3V, LP=32	$I_{IQS333LP32}$	-	<6		µA
Low Power Setting 2*	3.3V, LP=128	$I_{IQS333LP128}$	-	<4		µA
Low Power Setting 3*	3.3V, LP=256	$I_{IQS333LP256}$	-	<3		µA

*LP interval period = Low power value x 16ms

Table 11.3 Start-up and shut-down slope Characteristics

DESCRIPTION	Conditions	PARAMETER	MIN	MAX	UNIT
Power On Reset	V_{DDHI} Slope ≥ 100V/s @25°C	POR	1.2	1.6	V
Brown Out Detect	V_{DDHI} Slope ≥ 100V/s @25°C	BOD	1.15	1.6	V

Table 11.4 Initial Touch Times (First Touch)

DESCRIPTION	PARAMETER	MAX	Unit
TURBO MODE[1]	Response time	70	ms

Table 11.5 Repetitive Touch Rates

DESCRIPTION	Conditions	PARAMETER	Rate	UNIT
All power modes	Zoom active	Response Rate[2]	>8	Touches/second

The SCAN PERIOD of the **IQS333** is increased by:

- Faster communication.
- Less data transfer.
- Using the fast charge selection (Turbo Mode) of the **IQS333.**
- Reduced process time by disabling ACF, wheel filter, wheel position and ATI.

[1] Communication and charge frequency to comply with sample rate as reported earlier in this datasheet.

[2] Debounce of 2 up and 2 down, 9 active channels in Event Mode

12 Package information

12.1 IQS333 Package dimensions

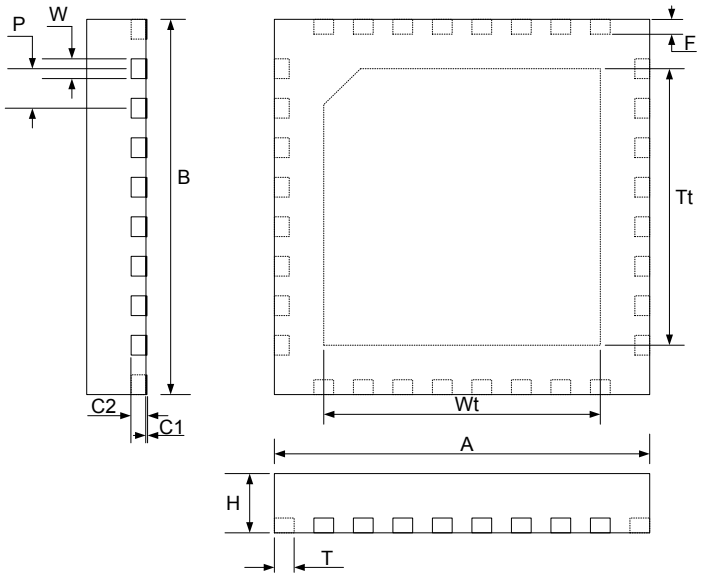


Figure 12.1 QFN(5x5) – 32 Package.

Table 12.1 QFN(5x5)-32 Package Dimensions.

DESCRIPTION	MIN	MAX	Unit
A	4.90	5.10	mm
B	4.90	5.10	mm
C1	0	0.05	mm
C2	0.203TYP		mm
F	0.400TYP		mm
H	0.85	0.95	mm
P	0.5TYP		mm
T	0.3	0.5	mm
T_t		3.25	mm
W	0.25TYP		mm
W_t		3.25	mm

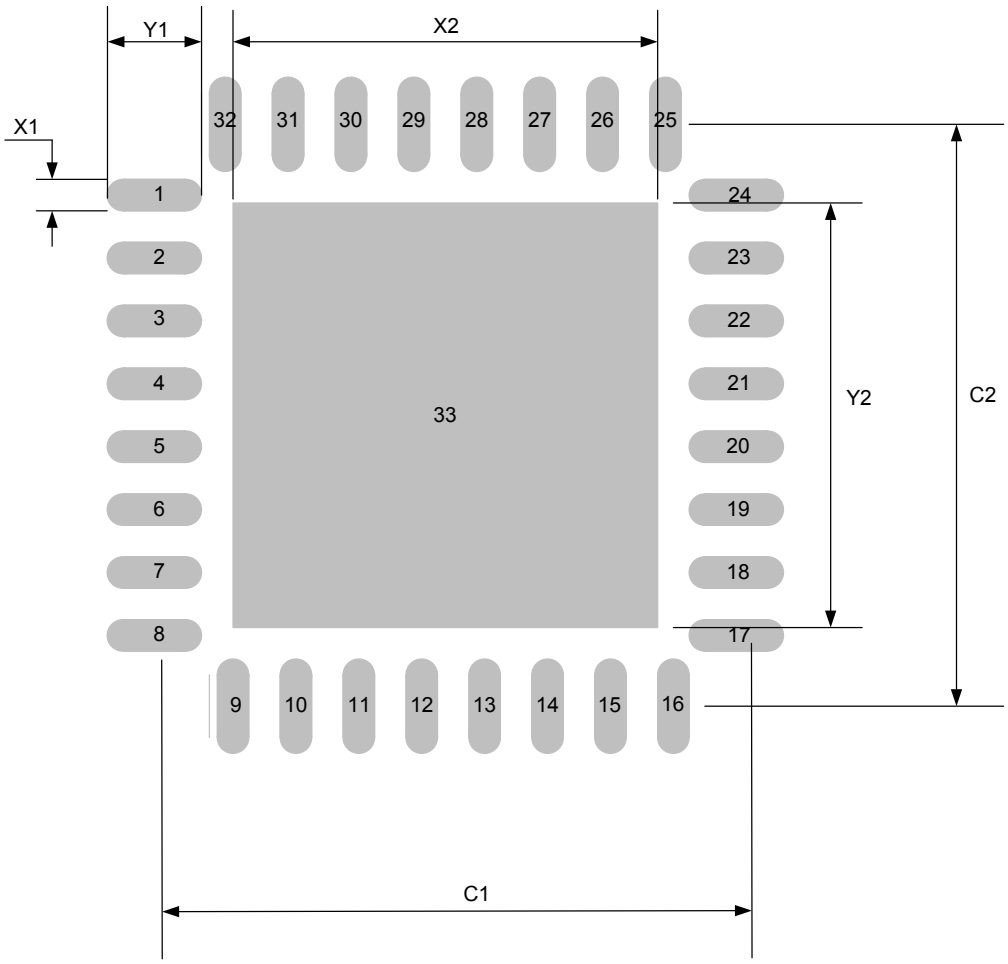


Figure 12.2 QFN(5x5) – 32 Footprint.

Table 12.2 QFN(5x5)-32 Footprint dimensions.

DESCRIPTION	Dimension	Unit
C1	4.90	mm
C2	4.90	mm
X1	0.30	mm
X2	3.25	mm
Y1	0.90	mm
Y2	3.25	mm

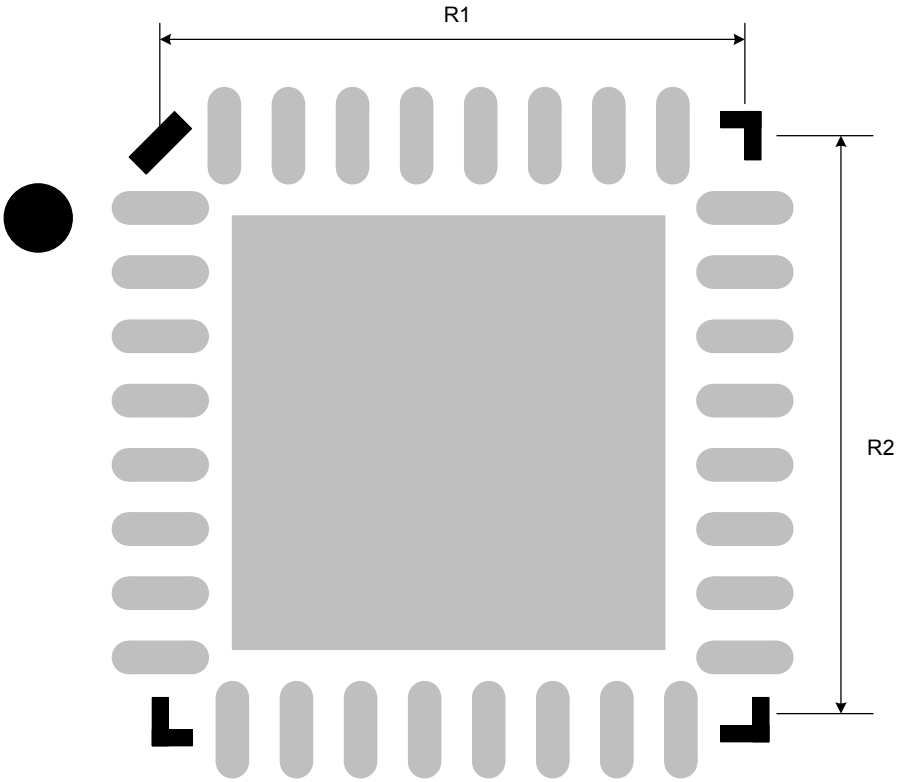
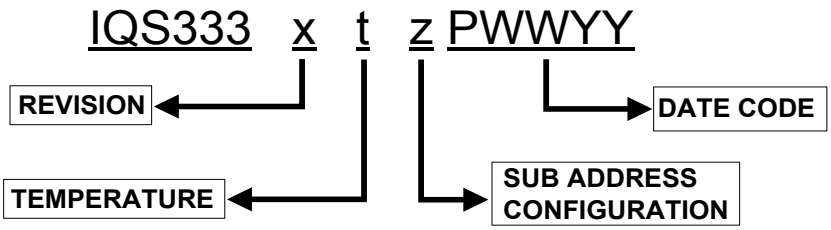


Figure 12.3 QFN(5x5)-32 Silk Screen.

Table 12.3 QFN(5x5)-32 Silk Screen Dimensions.

DESCRIPTION	Dimension	Unit
R1	5.00	mm
R2	5.00	mm

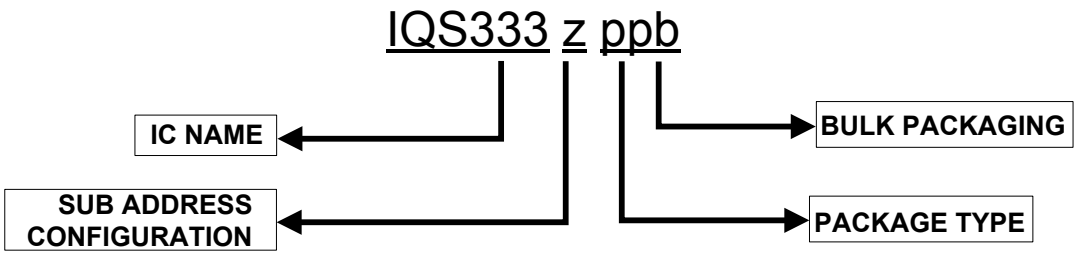
13 Device Marking



REVISION	**x**	=	IC Revision Number
TEMPERATURE RANGE	**t**	=	I -40°C to 85°C (Industrial)
		=	C 0°C to 70°C (Commercial)
IC CONFIGURATION	**z**	=	Sub Address Configuration (Hexadecimal) 0 = 64H 1 = 65H 2 = 66H 3 = 67H
DATE CODE	**P**	=	Package House
	WW	=	Week
	YY	=	Year

14 Ordering Information

Order quantities will be subject to multiples of a full reel. Contact the official distributor for sample quantities. A list of the distributors can be found under the “Distributors” section of www.azoteq.com.



IC NAME	IQS333	=	IQS333
CONFIGURATION	z	=	Sub Address Configuration (hexadecimal) 0 = 64H 1 = 65H 2 = 66H 3 = 67H
PACKAGE TYPE	QN	=	QFN(5x5)-32
BULK PACKAGING	R	=	Reel (3000pcs/reel)

Appendix A. Information for Alpha Customers Only

14.1 QFN20 Pin-out

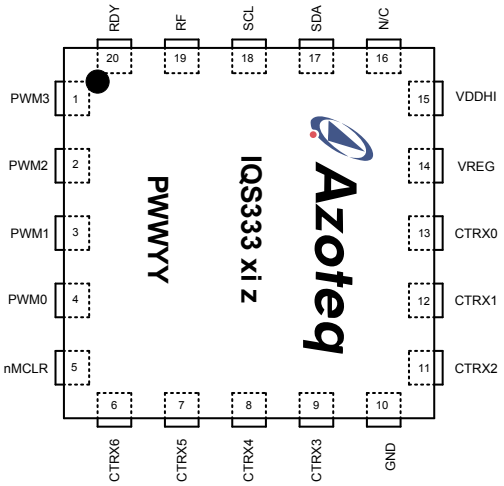


Figure 14.1 IQS333 Pin layout in QFN20

Table 14.1 IQS333 Pin-outs.

IQS333 Pin-out			
Pin #	**Name**	**Description Self-Capacitive**	**Description Projected-Capacitive**
1	PWM3	GPIO with Hardware PWM	GPIO with Hardware PWM
2	PWM2	GPIO with Hardware PWM	GPIO with Hardware PWM
3	PWM1	GPIO with Hardware PWM	GPIO with Hardware PWM
4	PWM0	GPIO with Hardware PWM	GPIO with Hardware PWM
5	/MCLR	Master Clear	Master Clear
6	CTRX6	Sense Electrode	Not Used
7	CTRX5	Sense Electrode	Tx2
8	CTRX4	Sense Electrode	Tx1 – slider two
9	CTRX3	Sense Electrode	Tx0 – slider one
10	GND	Ground	Ground
11	CTRX2	Sense Electrode	Rx2
12	CTRX1	Sense Electrode	Rx1
13	CTRX0	Sense Electrode	Rx0
14	VREG	Regulated Output	Regulated Output
15	VDDHI	Supply Input Voltage	Supply Input Voltage
16	NC	Not Connected	Not Connected
17	SDA	Data	Data
18	SCL	Clock	Clock
19	RF	RF input Antenna	RF input Antenna
20	RDY	Ready	Ready

14.2 IQS333 Package dimensions

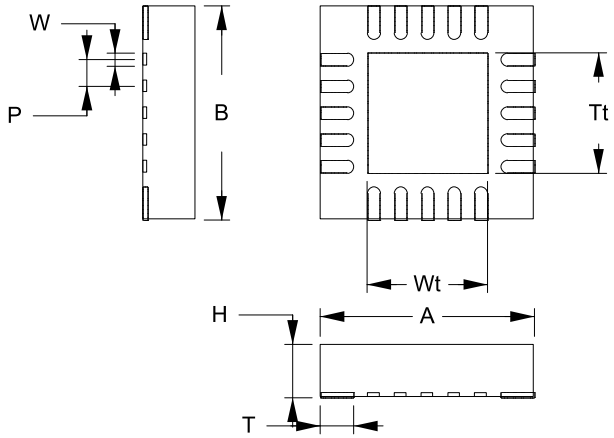


Figure 12.1 QFN(4x4)–20 Package Dimensions

Table 14.2 QFN (4x4)-20 Package Dimensions.

Dimension	Min	Max
A,B	3.85 mm	4.15 mm
C	0.70 mm	1.00 mm
D	0.00 mm	0.05 mm
E	0.203 mm Ref.	
F	0.5 mm Typ	
G	0.30mm	0.50 mm
H	0.18 mm	0.30 mm
I	0.2 mm Min.	
J,K		2.25mm

14.3 Recommended PCB footprint

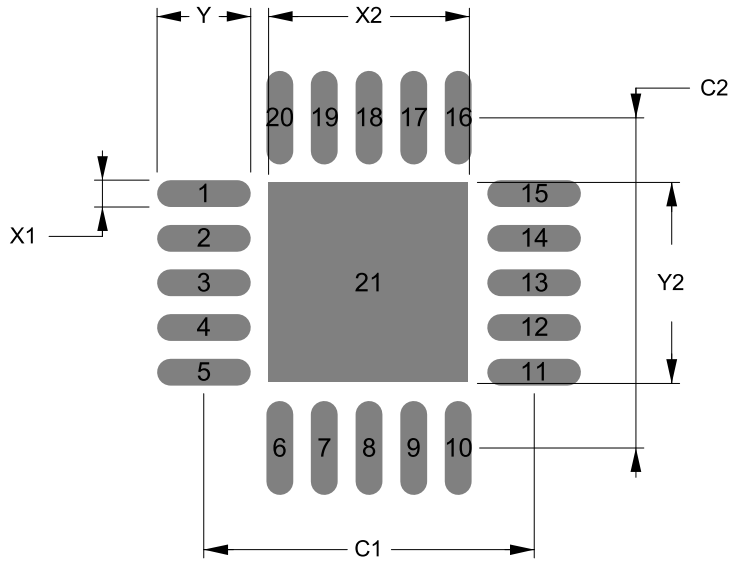


Figure 14.2 IQS333 Recommended PCB footprint

Table 14.3 QFN (4x4) – 20 Footprint Dimensions.

Dimension	[mm]
Pitch	0.50
C1	3.70
Y1	1.05
X1	0.30
C2	3.70
Y2	2.25
X2	2.25

14.4 Reference Design

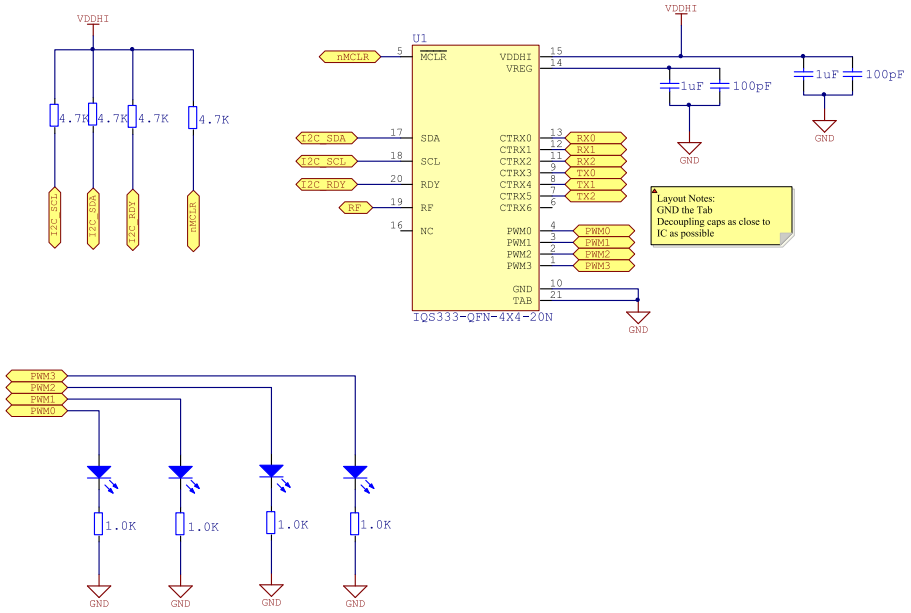


Figure 14.3 IQS333 Reference Design (Projected capacitive sensing).

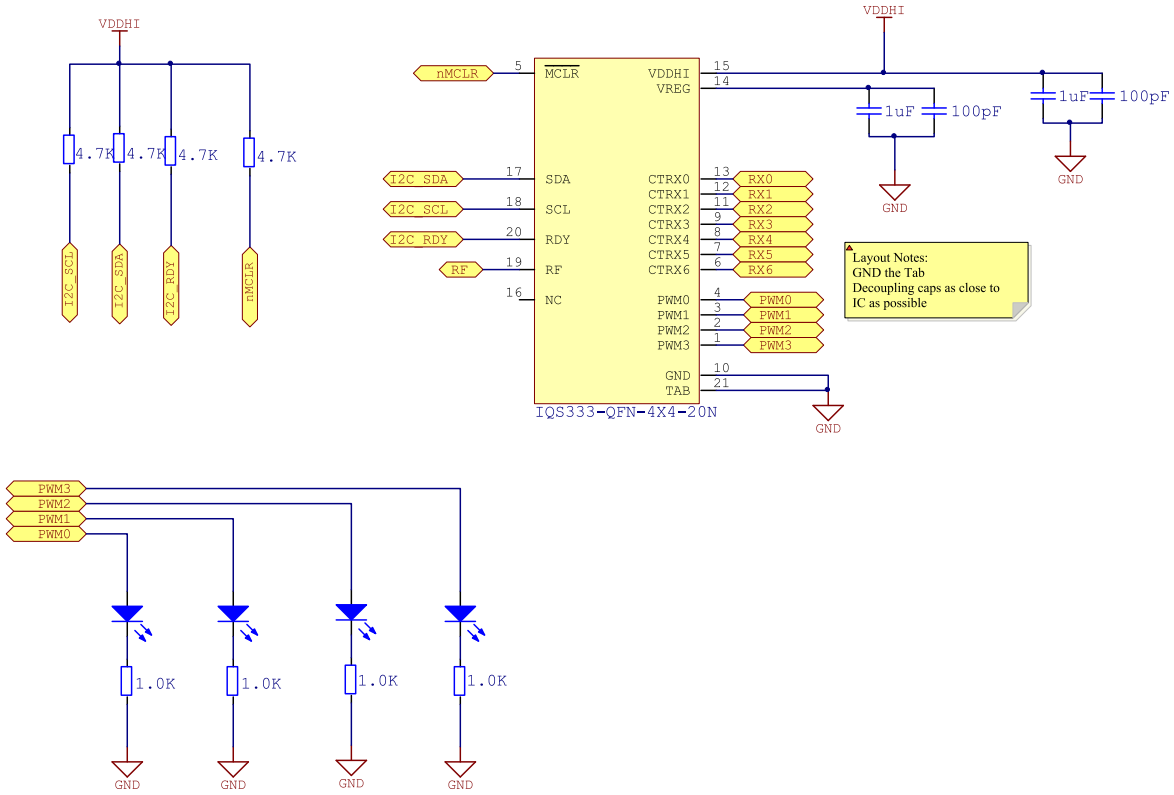


Figure 14.4 IQS333 Self Capacitive Reference Design.

Appendix B. Contact Information

	USA	Asia	South Africa
Physical Address	6507 Jester Blvd Bldg 5, suite 510G Austin TX 78750 USA	Rm1725, Glittery City Shennan Rd Futian District Shenzhen, 518033 China	109 Main Street Paarl 7646 South Africa
Postal Address	6507 Jester Blvd Bldg 5, suite 510G Austin TX 78750 USA	Rm1725, Glittery City Shennan Rd Futian District Shenzhen, 518033 China	PO Box 3534 Paarl 7620 South Africa
Tel	+1 512 538 1995	+86 755 8303 5294 ext 808	+27 21 863 0033
Fax	+1 512 672 8442		+27 21 863 1512
Email	kobusm@azoteq.com	linayu@azoteq.com.cn	info@azoteq.com

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