TJA1052i

Galvanically isolated high-speed CAN transceiver

Rev. 4 — 23 May 2016 Product data sheet

1. General description

The TJA1052i is a high-speed CAN transceiver that provides a galvanically isolated interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The TJA1052i is specifically targeted at Electric Vehicles (EV) and Hybrid Electric Vehicles (HEV), where galvanic isolation barriers are needed between the high- and low-voltage parts.

Safety: Isolation is required for safety reasons, eg. to protect humans from electric shock or to prevent the electronics being damaged by high voltages.

Signal integrity: The isolator uses proprietary capacitive isolation technology to transmit and receive CAN signals. This technology enables more reliable data communications in noisy environments, such as high-voltage battery management systems or the drive and regeneration systems in EVs and HEVs.

Performance: The transceiver is designed for high-speed CAN applications in the automotive industry, supplying the differential transmit and receive capability to a CAN protocol controller in a microcontroller. Integrating the galvanic isolation along with the transceiver in the TJA1052i removes the need for stand-alone isolation. It also improves reliability and system performance parameters such as loop delay.

The TJA1052i belongs to the third generation of high-speed CAN transceivers from NXP Semiconductors, offering significant improvements over first- and second-generation devices. It offers improved ElectroMagnetic Compatibility (EMC) and ElectroStatic Discharge (ESD) performance, and also features ideal passive behavior to the CAN bus when the transceiver supply voltage is off.

The TJA1052i implements the CAN physical layer as defined in the current ISO11898 standard (ISO11898-2:2003). Pending the release of ISO11898-2:2016 including CAN FD and SAE J2284-4/5, additional timing parameters defining loop delay symmetry are specified. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s.

The TJA1052i is an excellent choice for all types of automotive and industrial CAN networks where isolation is required for safety reasons or to enhance signal integrity in noisy environments.

2. Features and benefits

2.1 General

- Isolator and Transceiver integrated into a single SO16 package, reducing board space
- ISO 11898-2:2003 compliant

- Timing guaranteed for data rates up to 5 Mbit/s in the CAN FD fast phase
- Flawless cooperation between the Isolator and the Transceiver
  - Fewer components improves reliability in applications
  - Guaranteed performance (eg. max loop delay <220 ns)
- Electrical transient immunity of 45 kV/μs (typ)
- AEC-Q100 qualified
- Suitable for use in 12 V and 24 V systems; compatible with 3 V to 5 V microcontrollers
- Bus common mode voltage (V_{cm}) = ±25 V
- Low ElectroMagnetic Emission (EME) and high ElectroMagnetic Immunity (EMI)
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)

2.2 Power management

- Functional behavior predictable under all supply conditions
- Transceiver disengages from the bus when not powered up (zero load)

2.3 Protection

- Up to 5 kV (RMS) rated isolation
- Three versions available (1 kV, 2.5 kV and 5 kV)
- Voltage compliant with UL 1577, IEC 61010 and IEC 60950
- 5 kV (RMS) rated isolation voltage compliant with UL 1577, IEC 61010 and IEC 60950
- Supports ISO6469 ‘Electrically propelled road vehicles. Safety specifications.’
- High ESD handling capability on the bus pins
- Bus pins protected against transients in automotive environments
- Transmit Data (TXD) dominant time-out function
- Undervoltage detection on supply pins

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD1}	supply current 1	V_{TXD} = 0 V; bus dominant	-	-	2.6	mA
		V_{TXD} = V_{DD1}; bus recessive	-	-	5.6	mA
I_{DD2}	supply current 2	V_{TXD} = 0 V; bus dominant; 60 Ω load	-	-	70	mA
		V_{TXD} = V_{DD1}; bus recessive	-	-	10	mA
$V_{uvd(swoff)(VDD2)}$	switch-off undervoltage detection voltage on pin V_{DD2}		1.3	-	2.7	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 at pins CANH and CANL	–8	-	+8	kV
V_{CANH}	voltage on pin CANH		–58	-	+58	V
V_{CANL}	voltage on pin CANL		–58	-	+58	V
T_{vj}	virtual junction temperature		–40	-	+150	°C
T_{amb}	ambient temperature		–40	-	+125	°C

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TJA1052IT/5 TJA1052IT/2 TJA1052IT/1	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

Table 3. Voltage ratings

Type number	Rated insulation voltage according to UL 1577, IEC 61010 and IEC 60950
TJA1052IT/5	5 kV (RMS)
TJA1052IT/2	2.5 kV (RMS)
TJA1052IT/1	1 kV (RMS)

5. Block diagram

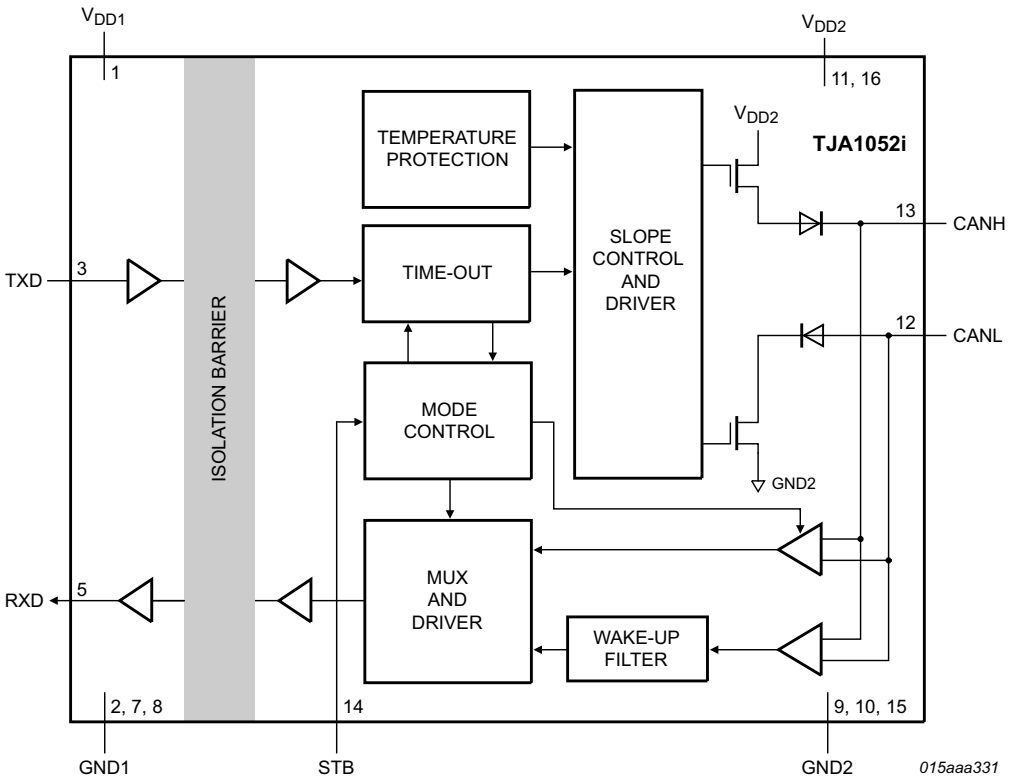


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

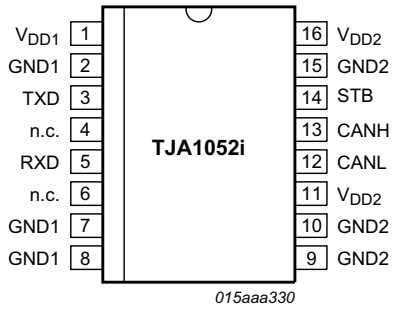


Fig 2. Pin configuration diagram

6.2 Pin description

Table 4. Pin description

Symbol	Pin	Description
V_{DD1}	1	supply voltage 1
GND1	2	ground supply 1[1]
TXD	3	transmit data input
n/c	4	not connected
RXD	5	receive data output; reads out data from the bus lines
n/c	6	not connected
GND1	7	ground supply 1[1]
GND1	8	ground supply 1[1]
GND2	9	ground supply 2[1]
GND2	10	ground supply 2[1]
V_{DD2}	11	supply voltage 2
CANL	12	LOW-level CAN bus line
CANH	13	HIGH-level CAN bus line
STB	14	Standby mode control input[2]
GND2	15	ground supply 2[1]
V_{DD2}	16	supply voltage 2

[1] All GND1 pins (pins 2, 7 and 8) should be connected together and to ground domain 1. All GND2 pins (pins 9, 10 and 15) should be connected together and to ground domain 2. Refer to the application notes for further information.

[2] Setting STB HIGH disables the CAN bus connection.

7. Functional description

7.1 Operation

7.1.1 Normal mode

During normal operation, the TJA1052i transceiver transmits and receives data via bus lines CANH and CANL (see Figure 1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data, which is output on pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME.

The isolator used in the TJA1052i is an AC device that employs on-off keying to guarantee the DC output state at all times. The states of TXD, RXD and the CAN bus at start-up, shut-down and during normal operation are described in Table 5.

Care should be taken regarding power sequencing if the device is used in networks that support remote wake-up (see Section 12 “Application information”).

Table 5. Input/output states at start-up, shut-down and during normal operation

TXD	RXD	V_{DD1}	V_{DD2}	CAN	Comments
H	H	$>V_{uvd(VDD1)}$	$>V_{uvd(stb)VDD2)}$	recessive	Normal mode operation
L	L	$>V_{uvd(VDD1)}$	$>V_{uvd(stb)VDD2)}$	dominant	Normal mode with TXD dominant time-out active
X	X	unpowered	$>V_{uvd(stb)VDD2)}$	dominant	dominant after V_{DD1} power loss until TXD dominant timeout; recessive while V_{DD2} is ramping up from an unpowered state
X	L	$>V_{uvd(VDD1)}$	unpowered	disconnected	RXD transitions L-to-H when V_{DD2} restored

7.1.2 Standby mode

The TJA1052i cannot transmit or receive regular CAN messages in Standby mode. Only the isolator and low-power CAN receiver are active, monitoring the bus lines for activity. The bus wake-up filter ensures that only bus dominant and bus recessive states that persist longer than $t_{fltr(wake)bus}$ are reflected on the RXD pin. To reduce current consumption, the CAN bus is terminated to GND and not biased to $V_{DD2}/2$ as in Normal mode.

Standby mode is selected by setting pin STB HIGH. The TJA1052i also switches to Standby mode when an undervoltage is detected on V_{DD2} ($V_{uvd(swoff)(VDD2)} < V_{DD2} < V_{uvd(stb)(VDD2)}$; Section 7.2.2). An internal pull-up ensures that Standby mode is selected by default when pin STB is not connected.

In Standby mode:

- The CAN transmitter if off
- The normal CAN receiver is off
- The low-power CAN receiver is active
- CANH and CANL are biased to GND
- The signal received at the low-power CAN receiver is reflected on pin RXD
- V_{DD2} undervoltage detection is active

The isolation function of the TJA1052i is not disabled in Standby mode. Overall quiescent current is not reduced significantly in this mode. The TJA1052i is not designed to support CAN bus wake-up functionality with very low quiescent currents.

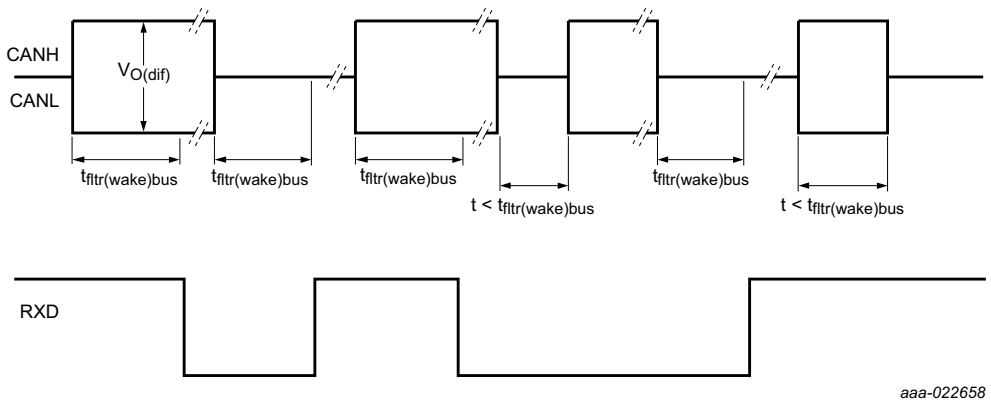


Fig 3. Wake-up timing

7.2 Fail-safe features

7.2.1 TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXD goes LOW. If the LOW state on TXD persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset by a positive edge on TXD. The TXD dominant time-out time also defines the minimum possible bit rate of 40 kbit/s.

7.2.2 Undervoltage protection: V_{DD2}

If the voltage on pin V_{DD2} falls below the standby threshold, $V_{uvd(stb)(VDD2)}$, the transceiver switches to Standby mode. The TJA1052i will remain in Standby mode until V_{DD2} rises above $V_{uvd(stb)(VDD2)}$ (max). The low-power receiver continues to monitor the bus while the TJA1052i is in Standby mode. Data on the bus is still reflected onto RXD, but the transfer speed is reduced.

If the voltage on V_{DD2} falls below the switch-off threshold, $V_{uvd(swoff)(VDD2)}$, the transceiver switches off and disengages from the bus (zero load). It is guaranteed to switch on again in Standby mode when V_{DD2} rises above $V_{uvd(swoff)(VDD2)}$ (max).

7.2.3 Undervoltage protection: V_{DD1}

If the voltage on pin V_{DD1} falls below the undervoltage detection threshold, $V_{uvd(VDD1)}$, the CAN bus switches to dominant state and the TXD dominant timeout timer is started. RXD will not go high again until the supply voltage has been restored on V_{DD1} ($V_{DD1} > V_{uvd(VDD1)}$).

7.2.4 Overtemperature protection

The output drivers are protected against overtemperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, the output drivers are disabled. They are enabled again when the virtual junction temperature falls below $T_{j(sd)}$ and TXD is HIGH. Including the TXD condition ensures that output driver oscillation due to temperature drift is avoided.

7.3 Insulation characteristics and safety-related specifications

Table 6. Isolator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$d_{L(IO1)}$	minimum air gap	[1]	8.6	-	-	mm
$d_{L(IO2)}$	minimum external tracking	[2]	8.1	-	-	mm
R_{ins}	insulation resistance	T_A = 125 °C [3]	100	-	-	GΩ
		T_A = 150 °C [3]	10	-	-	GΩ
-	pollution degree	-	2	-	-	-
-	material group (IEC 60664)		2	-	-	-

[1] Based on the measured data in the package outline. $d_{L(IO1)}$ is the clearance distance. Note that the clearance distance cannot be larger than the creepage distance ($d_{L(IO2)}$).

[2] Based on the measured data in the package outline. $d_{L(IO2)}$ is the creepage distance. According to IEC 60950-1, normative annex F (also IEC60664 chapter 6.2, Example 11), the effective minimum external tracking is 1.0 mm less due to the presence of an intervening, unconnected conductive part.

[3] Guaranteed by design at a voltage differential of 500 V with the pins on each side of the isolation barrier connected together, simulating a 2-pin device.

Table 7. Working voltages and isolation

Insulation Characteristics				
Parameter	Standard	TJA1052i/1	TJA1052i/2	TJA1052i/5
max. working insulation voltage per IEC 60664 (V_{IORM})[1]	IEC 60664	300 V_{RMS}	450 V_{RMS}	800 V_{RMS}
		420 V_{peak}	630 V_{peak}	1120 V_{peak}
max. transient overvoltage per IEC 60664 (V_{IOTM})[2]	t_{TEST} = 1.2/50 µs (certification) IEC 60664	2500 V_{peak}	4000 V_{peak}	6000 V_{peak}
rated insulation voltage per UL 1577 (V_{ISO})	UL 1577			
	t_{TEST} = 60 s (qualification)	1000 V_{RMS}	2500 V_{RMS}	5000 V_{RMS}
	t_{TEST} = 1 s (production)	1200 V_{RMS}	3000 V_{RMS}	6000 V_{RMS}
Insulation classification in terms of Overvoltage Category[3]				
Insulation type	Max. working voltage	TJA1052i/1	TJA1052i/2	TJA1052i/5
basic insulation[4]	≤150 V_{RMS}	I - III	I - IV	I - IV
	≤300 V_{RMS}	I - II	I - III	I - IV
	≤600 V_{RMS}	I	I - II	I - III
	≤1000 V_{RMS}	-	-	I - II
reinforced insulation[4]	≤150 V_{RMS}	I - II	I - III	I - IV
	≤300 V_{RMS}	I	I - II	I - III
	≤600 V_{RMS}	-	I	I - II
	≤1000 V_{RMS}	-	-	I

[1] The working voltage is the input-to-output voltage that can be applied without time limit. Which TJA1052i variant should be selected depends on the overvoltage category and the related insulation voltage.

[2] UL stress test is performed at higher than IEC-specified levels.

[3] Based on transient overvoltages as indicated in IEC60664; creepage and clearance distances not taken into account.

[4] Reinforced insulation should have an impulse withstand voltage one step higher than that specified for basic insulation.

Table 8. Safety approvals

Standard	File number
IEC 60950	CB NL-33788
IEC 61010-1 2nd Edition	CB NL-33789
UL1577	20131213-E361297

8. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages and currents are referenced to GND2 unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	voltage on pin x[1]	on pins CANH, CANL	−58	+58	V
		on pin V_{DD1}[2], V_{DD2}	−0.3	+6.0	V
		on pin STB	−0.3	V_{DD2} + 0.3	V
V_I	input voltage	on pin TXD [2]	−0.3	V_{DD1} + 0.3	V
V_O	output voltage	on pin RXD [2]	−0.3	V_{DD1} + 0.3	V
I_O	output current	on pin RXD [2]	-	10	mA
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL		−27	+27	V
V_{trt}	transient voltage	on pins CANH and CANL [3]			
		pulse 1	−100	-	V
		pulse 2a	-	75	V
		pulse 3a	−150	-	V
		pulse 3b	-	100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω) [4]			
		at pins CANH and CANL	−8	+8	kV
		Human Body Model (HBM); 100 pF, 1.5 kΩ [5]			
		at pins CANH and CANL [6]	−8	+8	kV
		at any other pin	−4	+4	kV
		Machine Model (MM); 200 pF, 0.75 μH, 10 Ω [7]			
		at any pin	−300	+300	V
		Charged Device Model (CDM); field Induced charge; 4 pF [8]			
		at corner pins	−750	+750	V
		at any pin	−500	+500	V
T_{vj}	virtual junction temperature	[9]	−40	+150	°C
T_{amb}	ambient temperature		−40	+125	°C
T_{stg}	storage temperature	[10]	−65	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

[2] Referenced to GND1.

[3] According to IEC TS 62228 (2007), Section 4.2.4; parameters for standard pulses defined in ISO7637 part 2: 2004-06.

[4] According to IEC TS 62228 (2007), Section 4.3; DIN EN 61000-4-2.

[5] According to AEC-Q100-002.

[6] ±8 kV to GND2 and V_{DD2}; ±6 kV to GND1.

[7] According to AEC-Q100-003.

[8] According to AEC-Q100-011 Rev-C1. The classification level is C4B.

[9] An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is a fixed value used in the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

[10] If UL compliance is required, the maximum storage temperature is limited to 130 °C.

9. Thermal characteristics

Table 10. Thermal characteristics

According to IEC 60747-1.

Symbol	Parameter	Conditions	Value	Unit
$R_{th(vj-a)}$	thermal resistance from virtual junction to ambient	in free air	100	K/W

10. Static characteristics

Table 11. Static characteristics

T_{vj} = −40 °C to +150 °C; V_{DD1} = 3.0 V to 5.25 V with respect to GND1; V_{DD2} = 4.75 V to 5.25 V with respect to GND2 unless otherwise specified. Positive currents flow into the IC. All voltages and currents are referenced to GND2 unless otherwise specified[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DC supplies; pin V_{DD1} and V_{DD2}						
I_{DD1}	supply current 1	V_{DD1} = 3 V to 5 V[2]; V_{DD2} = 5 V; V_{TXD} = 0 V[2]; bus dominant	-	-	2.6	mA
		V_{DD1} = 3 V to 5 V[2]; V_{DD2} = 5 V; V_{TXD} = V_{DD1}[2]; bus recessive	-	-	5.6	mA
I_{DD2}	supply current 2	V_{DD1} = 3 V to 5 V[2]; V_{DD2} = 5 V; V_{TXD} = 0 V[2]; bus dominant; R_L = 60 Ω	-	-	67.6	mA
		V_{DD1} = 3 V to 5 V[2]; V_{DD2} = 5 V; V_{TXD} = V_{DD1}[2]; bus recessive; V_{STB} = 0 V	-	-	13.1	mA
		V_{DD1} = 3 V to 5 V[2]; V_{DD2} = 5 V; V_{TXD} = V_{DD1}[2]; bus recessive; V_{STB} = 5 V	-	-	5.6	mA
$V_{uvd(stb)(VDD2)}$	standby undervoltage detection voltage on pin V_{DD2}		3.5	-	4.75	V
$V_{uvd(swoff)(VDD2)}$	switch-off undervoltage detection voltage on pin V_{DD2}		1.3	-	2.7	V
$V_{uvd(VDD1)}$	undervoltage detection voltage on pin V_{DD1}	[2]	1.3	-	2.7	V
V_{uvhys}	undervoltage hysteresis voltage	on pin V_{DD1} [2]	40	-	100	mV
		on pin V_{DD2}	80	-	200	mV
CAN transmit data input; pin TXD						
V_{IH}	HIGH-level input voltage	[2]	2.0	-	V_{DD1}	V
V_{IL}	LOW-level input voltage	[2]	0	-	0.8	V
I_{LI}	input leakage current	[2]	−10	-	+10	µA
CAN receive data output; pin RXD						
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA [2]	V_{DD1} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA [2]	-	-	0.4	V
Standby mode control input; pin STB						
V_{IH}	HIGH-level input voltage		$0.7V_{DD2}$	-	V_{DD2} + 0.3	V

Table 11. Static characteristics *…continued*

T_{vj} = −40 °C to +150 °C; V_{DD1} = 3.0 V to 5.25 V with respect to GND1; V_{DD2} = 4.75 V to 5.25 V with respect to GND2 unless otherwise specified. Positive currents flow into the IC. All voltages and currents are referenced to GND2 unless otherwise specified[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage		−0.3	-	$0.3V_{DD2}$	V
I_{IH}	HIGH-level input current	$V_{STB} = V_{DD2}$	−1	-	+1	µA
I_{IL}	LOW-level input current	V_{STB} = 0 V	−15	-	−1	µA
Bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	V_{TXD} = 0 V; t < $t_{to(dom)TXD}$				
		pin CANH; R_L = 50 Ω to 65 Ω	2.75	3.5	4.5	V
		pin CANL; R_L = 50 Ω to 65 Ω	0.5	1.5	2.25	V
$V_{dom(TX)sym}$	transmitter dominant voltage symmetry	$V_{dom(TX)sym}$ = $V_{DD2} - V_{CANH} - V_{CANL}$	−400	-	+400	mV
V_{TXsym}	transmitter voltage symmetry	$V_{TXsym} = V_{CANH} + V_{CANL}$; f_{TXD} = 250 kHz; C_{SPLIT} = 4.7 nF [3] [4]	$0.9V_{DD2}$	-	$1.1V_{DD2}$	V
$V_{O(dif)}$	differential output voltage	dominant; Normal mode				
		V_{TXD} = 0 V; t < $t_{to(dom)TXD}$; R_L = 45 Ω to 70 Ω [2]	1.5	-	3	V
		V_{TXD} = 0 V; t < $t_{to(dom)TXD}$; R_L = 2240 Ω [2]	1.5	-	5	V
		recessive				
		Normal mode: $V_{TXD} = V_{DD1}$; no load [2]	−50	-	+50	mV
		Standby mode; no load	−0.2	-	+0.2	V
$V_{O(rec)}$	recessive output voltage	Normal mode; $V_{TXD} = V_{DD1}$; no load [2]	2	$0.5V_{DD2}$	3	V
$V_{th(RX)dif}$	differential receiver threshold voltage	Normal mode; −25 V ≤ V_{CANL} ≤ +25 V; −25 V ≤ V_{CANH} ≤ +25 V	0.5	-	0.9	V
		Standby mode; −12 V ≤ V_{CANL} ≤ +12 V; −12 V ≤ V_{CANH} ≤ +12 V [5]	0.4	-	1.15	V
$V_{rec(RX)}$	receiver recessive voltage	Normal mode; −12 V ≤ V_{CANL} ≤ +12 V; −12 V ≤ V_{CANH} ≤ +12 V	−3	-	0.5	V
$V_{dom(RX)}$	receiver dominant voltage	Normal mode; −12 V ≤ V_{CANL} ≤ +12 V; −12 V v V_{CANH} ≤ +12 V	0.9	-	8.0	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	−25 V ≤ V_{CANL} ≤ +25 V; −25 V ≤ V_{CANH} ≤ +25 V; Normal mode	-	165	-	mV
$I_{O(sc)dom}$	dominant short-circuit output current	V_{TXD} = 0 V [2]; t < $t_{to(dom)TXD}$; V_{DD2} = 5 V				
		pin CANH; V_{CANH} = −3 V to +40 V	−100	−70	−40	mA
		pin CANL; V_{CANL} = −3 V to +40 V	40	70	100	mA

Table 11. Static characteristics *…continued*

T_{vj} = −40 °C to +150 °C; V_{DD1} = 3.0 V to 5.25 V with respect to GND1; V_{DD2} = 4.75 V to 5.25 V with respect to GND2 unless otherwise specified. Positive currents flow into the IC. All voltages and currents are referenced to GND2 unless otherwise specified[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{O(sc)rec}$	recessive short-circuit output current	Normal mode; $V_{TXD} = V_{DD1}$[2]; $V_{CANH} = V_{CANL}$ = −27 V to +32 V	−5	-	+5	mA
I_L	leakage current	V_{DD2} = 0 V or V_{DD2} shorted to GND via 47 kΩ; $V_{CANH} = V_{CANL}$ = 5 V;	−3	-	+3	µA
R_i	input resistance		9	15	28	kΩ
ΔR_i	input resistance deviation	between V_{CANH} and V_{CANL}	−3	-	+3	%
$R_{i(dif)}$	differential input resistance		19	30	52	kΩ
$C_{i(cm)}$	common-mode input capacitance	[3]	-	-	20	pF
$C_{i(dif)}$	differential input capacitance	[3]	-	-	10	pF
Temperature detection						
$T_{j(sd)}$	shutdown junction temperature	[3] [6]	-	190	-	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] Referenced to GND1.

[3] Not tested in production; guaranteed by design.

[4] The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in Figure 9.

[5] Standby mode entered when V_{DD2} falls below $V_{uvd(stb)(VDD2)}$.

[6] RXD is LOW during thermal shutdown.

11. Dynamic characteristics

Table 12. Dynamic characteristics

T_{vj} = −40 °C to +150 °C; V_{DD1} = 3.0 V to 5.25 V with respect to GND1; V_{DD2} = 4.75 V to 5.25 V with respect to GND2 unless otherwise specified[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Transceiver timing; pins CANH, CANL, TXD and RXD; see Figure 4						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	Normal mode	-	72	120	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	Normal mode	-	97	120	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	Normal mode	-	67	130	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	Normal mode	-	72	130	ns
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	Normal mode	72	-	220	ns
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	Normal mode	72	-	220	ns
$t_{bit(bus)}$	transmitted recessive bit width	$t_{bit(TXD)}$ = 500 ns [2]	435	-	530	ns
		$t_{bit(TXD)}$ = 200 ns [2]	155	-	210	ns
$t_{bit(RXD)}$	bit time on pin RXD	$t_{bit(TXD)}$ = 500 ns [2]	400	-	550	ns
		$t_{bit(TXD)}$ = 200 ns [2]	120	-	220	ns
Δt_{rec}	receiver timing symmetry	$t_{bit(TXD)}$ = 500 ns	−65	-	+40	ns
		$t_{bit(TXD)}$ = 200 ns	−45	-	+15	ns
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0 V; Normal mode [3]	0.3	1.7	5	ms
CMTI	common-mode transient immunity	$V_I = V_{DD1}$ or V_I = 0 V [4]	20	45	-	kV/µs
$t_{startup}$	start-up time	[5]	-	-	500	µs
$t_{fltr(wake)bus}$	bus wake-up filter time	Standby mode	0.5	1	3	µs

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] See Figure 5.

[3] Referenced to GND1.

[4] V_I is the input voltage on TXD. See Figure 7 for test setup.

[5] The start-up time is the time from the application of power to valid data at the output. Guaranteed by design.

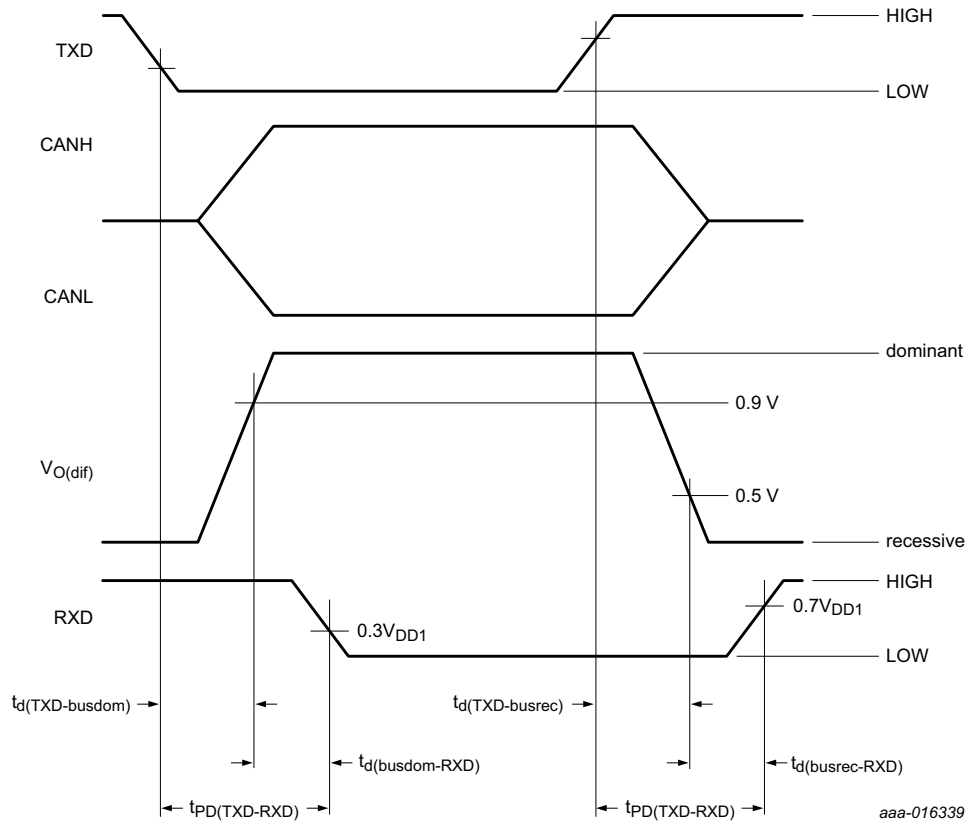


Fig 4. CAN transceiver timing diagram

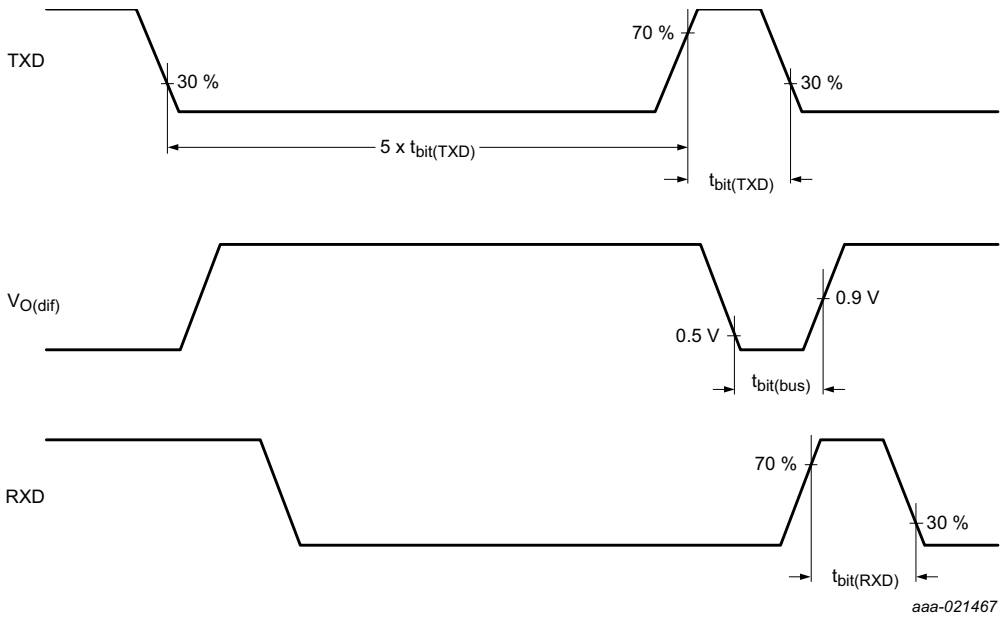


Fig 5. Loop delay symmetry timing diagram

12. Application information

Isolated CAN applications are becoming increasingly common in electric and hybrid electric vehicles. The TJA1052i is the ideal solution in applications that require an isolated CAN node, such as Li-ion battery management, regenerative braking and 48 V-to-12 V level shifting. The device can also be used to isolate high-voltage on-demand pumps and motors in belt elimination projects.

If the TJA1052i is used in a HS-CAN network that supports remote bus wake-up, the power-down sequence of the supplies must be managed properly to avoid a dominant pulse on the CAN bus. V_{DD2} should pass the minimum undervoltage threshold ($V_{uvd(stb)(VDD2)}$ (min)) before V_{DD1} falls below its maximum undervoltage detection threshold ($V_{uvd(VDD1)(max)}$). Power-up sequencing can happen in any order.

Digital inputs and outputs are 3 V compliant, allowing the TJA1052i to interface directly with 3 V and 5 V microcontrollers.

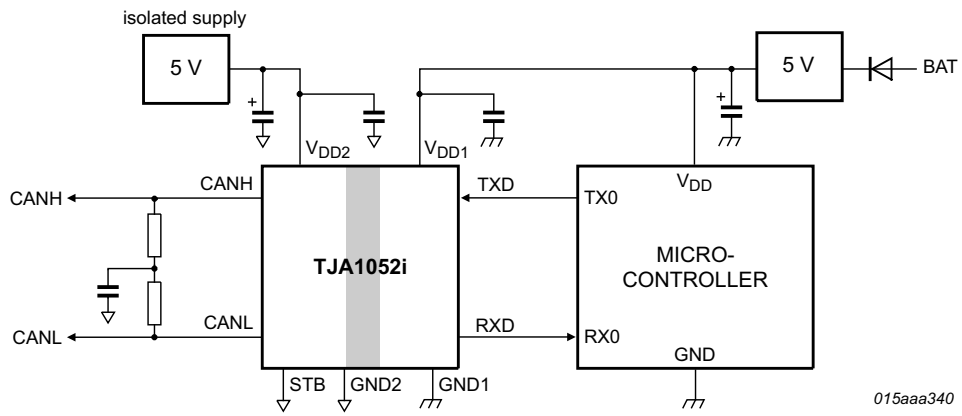


Fig 6. Typical application with TJA1052i and a 5 V microcontroller.

12.1 Application hints

Further information on the application of the TJA1052i can be found in NXP application hints *AH1301 Application Hints - TJA1052i Galvanic Isolated High Speed CAN Transceiver.*

13. Test information

13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-G - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

13.2 Test circuits

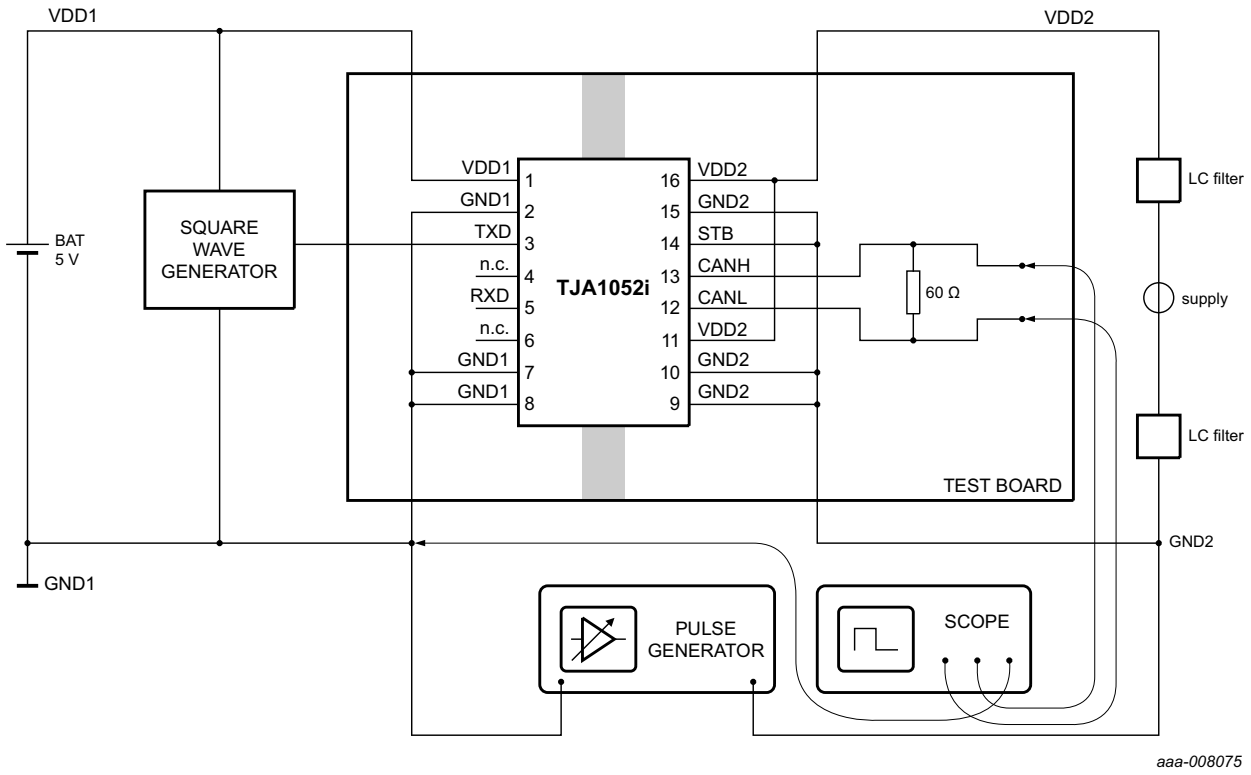


Fig 7. CMTI test setup

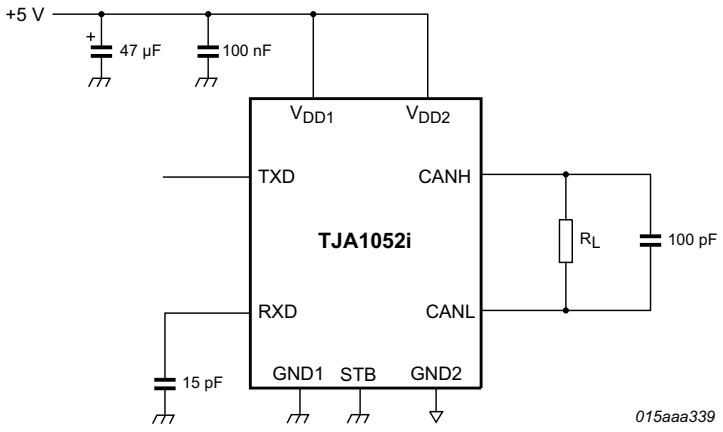


Fig 8. Timing test circuit for CAN transceiver

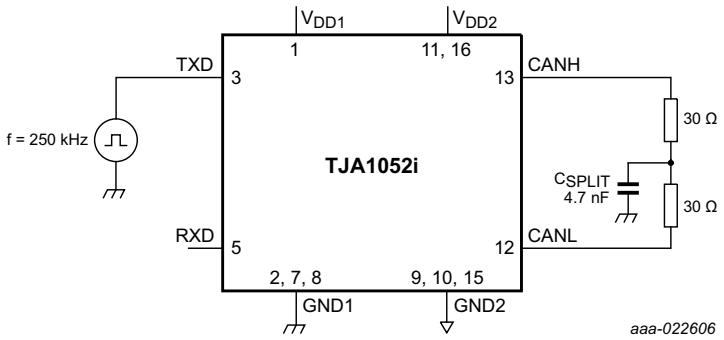
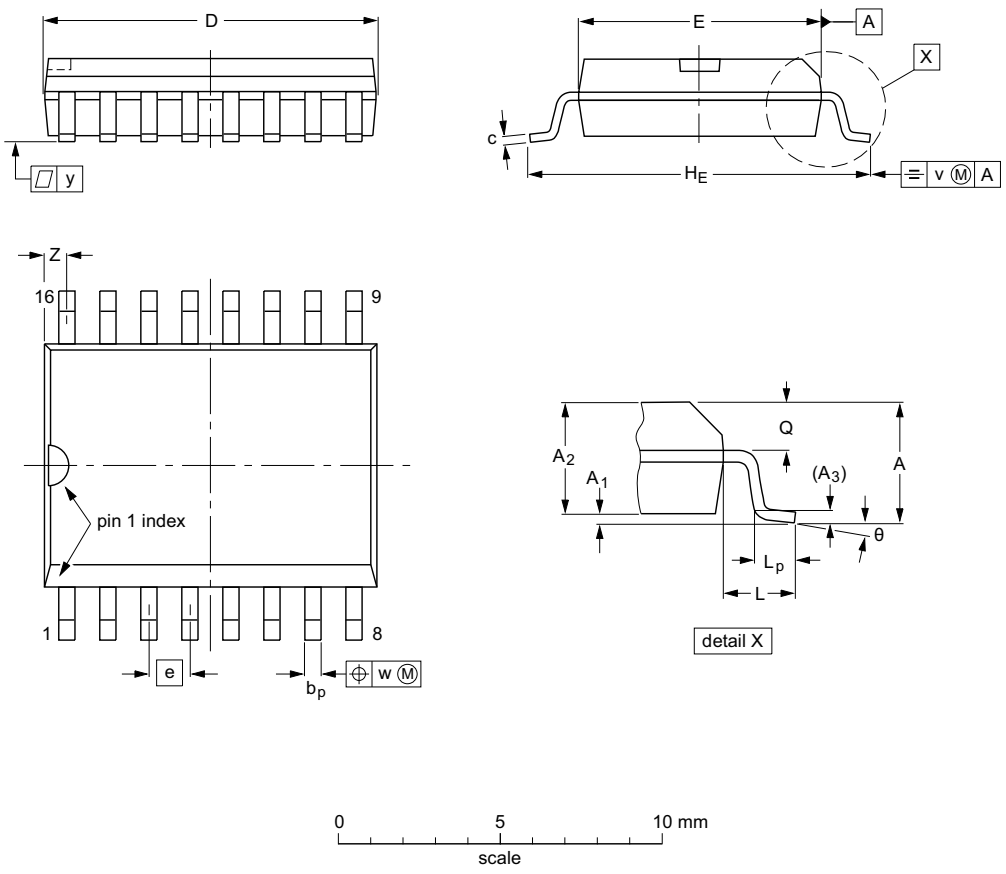


Fig 9. Test circuit for measuring transceiver driver symmetry

14. Package outline

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT162-1	075E03	MS-013				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT162-1 (SO16)

15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 11) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 13 and 14

Table 13. SnPb eutectic process (from J-STD-020D)

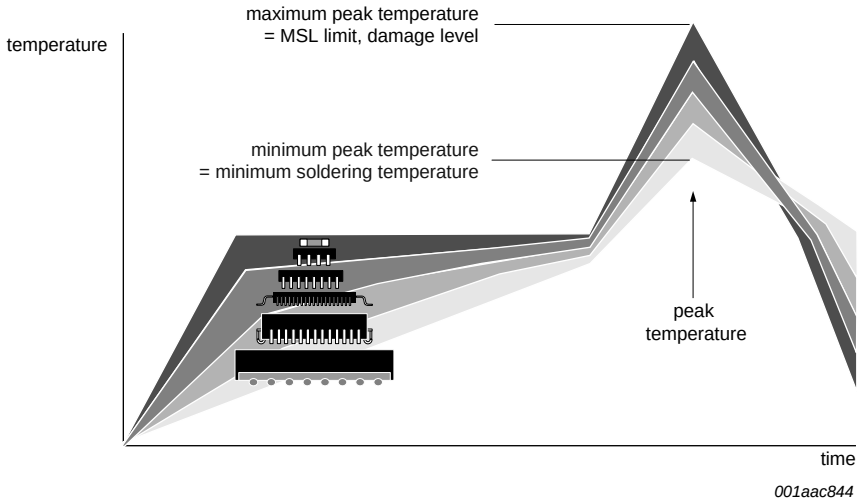
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 14. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 11.



MSL: Moisture Sensitivity Level

Fig 11. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Appendix: ISO 11898-2:2016 parameter cross-reference list

Table 15. ISO 11898-2:2016 to NXP data sheet parameter conversion

ISO 11898-2:2016		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA dominant output characteristics			
Single ended voltage on CAN_H	V_{CAN_H}	$V_{O(dom)}$	dominant output voltage
Single ended voltage on CAN_L	V_{CAN_L}		
Differential voltage on normal bus load	V_{Diff}	$V_{O(dif)}$	differential output voltage
Differential voltage on effective resistance during arbitration			
Optional: Differential voltage on extended bus load range			
HS-PMA driver symmetry			
Driver symmetry	V_{SYM}	V_{TXsym}	transmitter voltage symmetry
Maximum HS-PMA driver output current			
Absolute current on CAN_H	I_{CAN_H}	$I_{O(sc)dom}$	dominant short-circuit output current
Absolute current on CAN_L	I_{CAN_L}		
HS-PMA recessive output characteristics, bus biasing active/inactive			
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{O(rec)}$	recessive output voltage
Single ended output voltage on CAN_L	V_{CAN_L}		
Differential output voltage	V_{Diff}	$V_{O(dif)}$	differential output voltage
Optional HS-PMA transmit dominant timeout			
Transmit dominant timeout, long	t_{dom}	$t_{to(dom)TXD}$	TXD dominant time-out time
Transmit dominant timeout, short			
HS-PMA static receiver input characteristics, bus biasing active/inactive			
Recessive state differential input voltage range Dominant state differential input voltage range	V_{Diff}	$V_{th(RX)dif}$	differential receiver threshold voltage
		$V_{rec(RX)}$	receiver recessive voltage
		$V_{dom(RX)}$	receiver dominant voltage
HS-PMA receiver input resistance (matching)			
Differential internal resistance	R_{Diff}	$R_{i(dif)}$	differential input resistance
Single ended internal resistance	R_{CAN_H} R_{CAN_L}	R_i	input resistance
Matching of internal resistance	MR	ΔR_i	input resistance deviation
HS-PMA implementation loop delay requirement			
Loop delay	t_{Loop}	$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH
		$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW
Optional HS-PMA implementation data signal timing requirements for use with bit rates above 1 Mbit/s up to 2 Mbit/s and above 2 Mbit/s up to 5 Mbit/s			
Transmitted recessive bit width @ 2 Mbit/s / @ 5 Mbit/s, intended	$t_{Bit(Bus)}$	$t_{bit(bus)}$	transmitted recessive bit width
Received recessive bit width @ 2 Mbit/s / @ 5 Mbit/s	$t_{Bit(RXD)}$	$t_{bit(RXD)}$	bit time on pin RXD
Receiver timing symmetry @ 2 Mbit/s / @ 5 Mbit/s	Δt_{Rec}	Δt_{rec}	receiver timing symmetry

Table 15. ISO 11898-2:2016 to NXP data sheet parameter conversion

ISO 11898-2:2016		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}			
Maximum rating V_{Diff}	V_{Diff}	$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL
General maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	V_x	voltage on pin x
Optional: Extended maximum rating VCAN_H and VCAN_L			
HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered			
Leakage current on CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}	I_L	leakage current
HS-PMA bus biasing control timings			
CAN activity filter time, long	t_{Filter}	$t_{wake(busdom)}$[1]	bus dominant wake-up time
CAN activity filter time, short		$t_{wake(busrec)}$[1]	bus recessive wake-up time
Wake-up timeout, short	t_{Wake}	$t_{to(wake)bus}$	bus wake-up time-out time
Wake-up timeout, long			
Timeout for bus inactivity	$t_{Silence}$	$t_{to(silence)}$	bus silence time-out time
Bus Bias reaction time	t_{Bias}	$t_{d(busact-bias)}$	delay time from bus active to bias

[1] $t_{fltr(wake)bus}$ - bus wake-up filter time, in devices with basic wake-up functionality

18. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1052i v.4.01	20160523	Product data sheet	-	TJA1052i v.3
Modifications:	• Figure 1, Figure 4, Figure 6, Figure 8 amended • Section 7.1.2, Section 7.2.2 revised • Table 9: supply pin voltages combined in parameter V_x; Table note 1 added; parameter V_{trt} revised • Table 11: measurement added and values/conditions changed for parameter I_{DD2} • Table 12: added parameter $t_{fltr(wake)bus}$; added Table note 3; Table note 4 revised • ISO 11898-2:2016 compliance: – Section 1: text amended (2nd last paragraph) – Section 2.1: text amended (3rd feature) – Table 9: parameter $V_{(CANH-CANL)}$ added – Table 11: - measurement conditions changed for parameters $V_{O(dom)}$, $V_{O(dif)}$, I_L, $I_{O(sc)dom}$, $V_{hys(RX)dif}$ and $V_{th(RX)dif}$ (associated table note removed) - added parameters V_{TXsym} (and associated table note), $V_{rec(RX)}$ and $V_{dom(RX)}$ - symbol $V_{O(dif)bus}$ renamed as $V_{O(dif)}$ - additional measurements included for parameter $V_{O(dif)}$ – Table 12: - added parameters $t_{bit(bus)}$ and Δt_{rec} - parameter $t_{PD(TXD-RXD)}$ replaced with parameters $t_{d(TXDL-RXDL)}$ and $t_{d(TXDH-RXDH)}$ - additional measurement included for parameter $t_{bit(RXD)}$ – Figure 5 amended; Figure 9 added – Section 17 added			
TJA1052I v.3	20150119	Product data sheet	-	TJA1052I v.2
TJA1052I v.2	20130712	Product data sheet	-	TJA1052I v.1
TJA1052I v.1	20130424	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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