

NTB5412N, NTP5412N

Power MOSFET 60 Amps, 60 Volts N-Channel D²PAK, TO-220

Features

- Low $R_{DS(on)}$
- High Current Capability
- Avalanche Energy Specified
- These are Pb-Free Devices

Applications

- LED Lighting and LED Backlight Drivers
- DC-DC Converters
- DC Motor Drivers
- Power Supplies Secondary Side Synchronous Rectification

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ Unless otherwise specified)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	60	V
Gate-to-Source Voltage – Continuous			V_{GS}	± 20	V
Gate-to-Source Voltage – Nonrepetitive ($T_P < 10 \mu s$)			V_{GS}	± 30	V
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^{\circ}C$	I_D	60	A
		$T_C = 100^{\circ}C$		44	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^{\circ}C$	P_D	125	W
Pulsed Drain Current	$t_p = 10 \mu s$		I_{DM}	155	A
Operating and Storage Temperature Range			T_J, T_{stg}	-55 to 175	$^{\circ}C$
Source Current (Body Diode)			I_S	60	A
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^{\circ}C$ ($V_{DD} = 50 V_{dc}$, $V_{GS} = 10 V_{dc}$, $I_{L(pk)} = 60 A$, $L = 0.1 mH$, $R_G = 25 \Omega$)			E_{AS}	180	mJ
Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds			T_L	260	$^{\circ}C$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) Steady State (Note 1)	$R_{\theta JC}$	1.2	$^\circ\text{C/W}$
	$R_{\theta JA}$	43.2	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [1 oz] including traces).

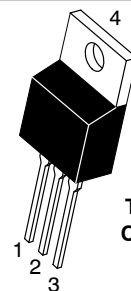
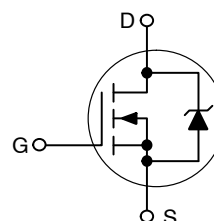


ON Semiconductor®

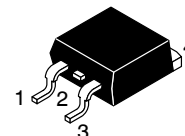
<http://onsemi.com>

$V_{(BR)DS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$ (Note 1)
60 V	14 m Ω @ 10 V	60 A

N-Channel

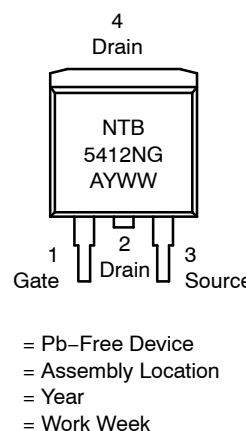
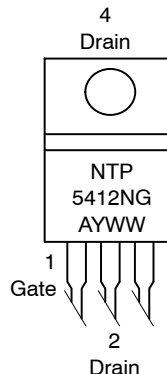


TO-220AB
CASE 221A
STYLE 5



D²PAK
CASE 418B
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENT



G = Pb-Free Device
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTB5412N, NTP5412N

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
-----------------	--------	----------------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{DS} = 0 V, I _D = 250 μA	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			54.6		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V V _{DS} = 60 V	T _J = 25°C		1.0	μA
			T _J = 150°C		100	
Gate-Body Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250 μA	2.0	3.3	4.0	V
Negative Threshold Temperature Coefficient	V _{GS(th)} /T _J			6.4		mV/°C
Drain-to-Source On Voltage	V _{DS(on)}	V _{GS} = 10 V, I _D = 60 A		0.7	1.2	V
		V _{GS} = 10 V, I _D = 30 A, 150°C		0.75		
Static Drain-to-Source On-Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 30 A		11.1	14	mΩ
Forward Transconductance	g _{FS}	V _{GS} = 15 V, I _D = 30 A		58		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{iss}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz		2325	3220	pF
Output Capacitance	C _{oss}			440		
Transfer Capacitance	C _{rss}			170		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 0 V, V _{DS} = 48 V, I _D = 60 A		66	85	nC
Threshold Gate Charge	Q _{G(TH)}			2.8		
Gate-to-Source Charge	Q _{GS}			13.4		
Gate-to-Drain Charge	Q _{GD}			31		

SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)

Turn-On Delay Time	t _{d(on)}	V _{GS} = 10 V, V _{DD} = 48 V, I _D = 60 A, R _G = 2.5 Ω		14		ns
Rise Time	t _r			115		
Turn-Off Delay Time	t _{d(off)}			41		
Fall Time	t _f			89		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V I _S = 60 A	T _J = 25°C		1.0	1.2	V _{dc}
			T _J = 125°C		0.9		
Reverse Recovery Time	t _{rr}	I _S = 60 A _{dc} , V _{GS} = 0 V _{dc} , di _S /dt = 100 A/μs		75		ns	
Charge Time	t _a			54			
Discharge Time	t _b			21			
Reverse Recovery Stored Charge	Q _{RR}			96		nC	

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

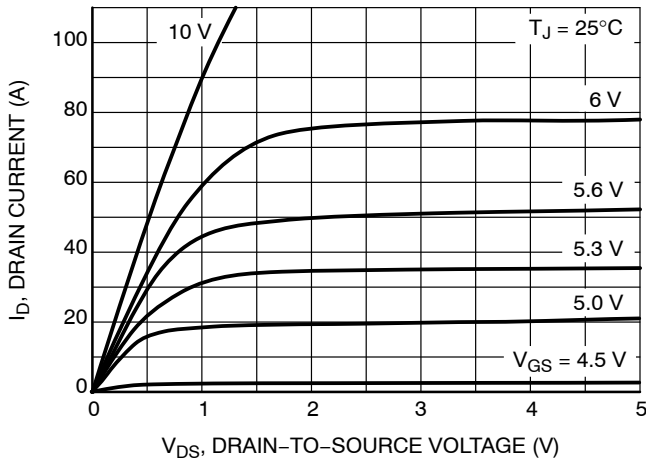


Figure 1. On-Region Characteristics

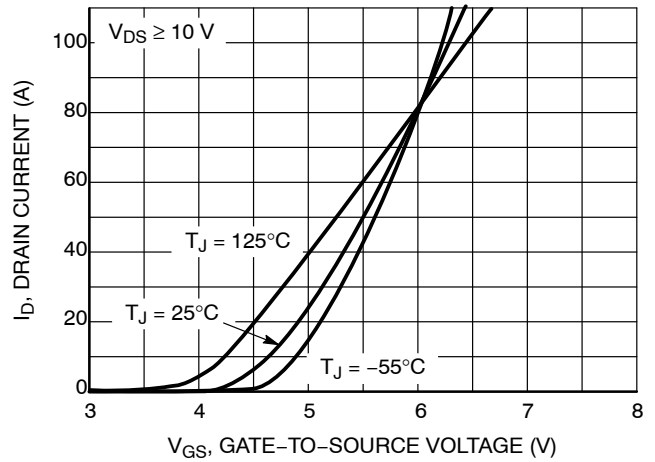


Figure 2. Transfer Characteristics

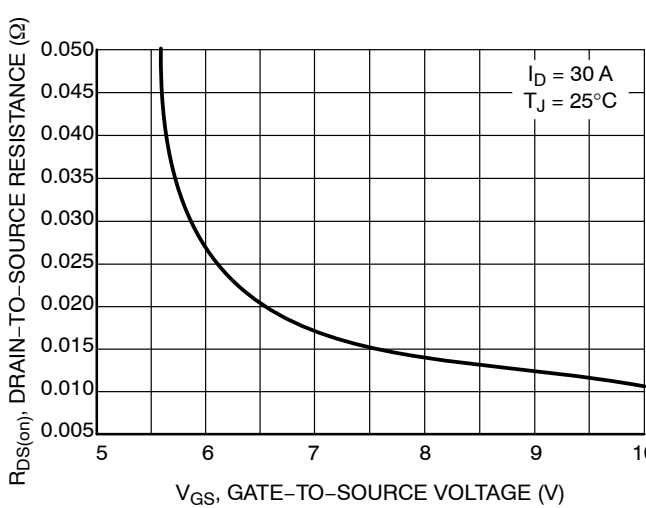


Figure 3. On-Resistance vs. Gate-to-Source Voltage

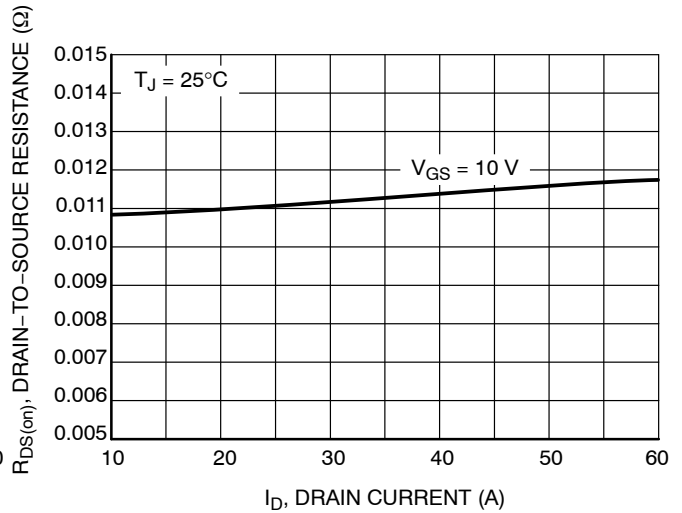


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

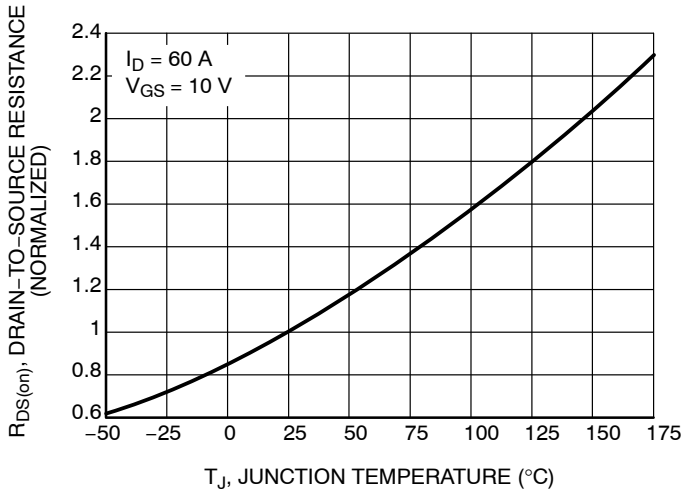


Figure 5. On-Resistance Variation with Temperature

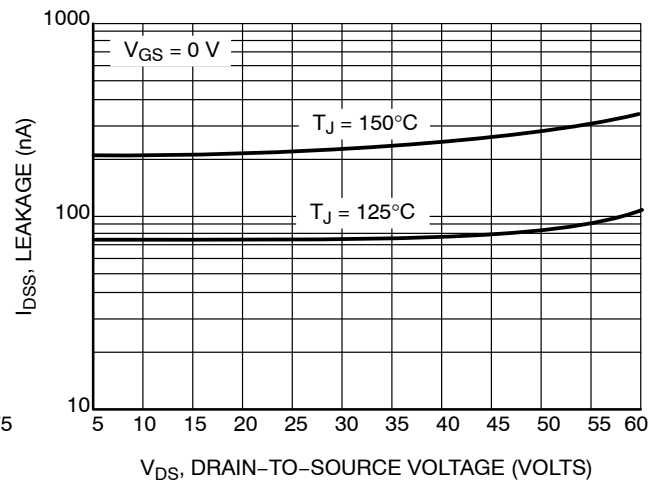


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

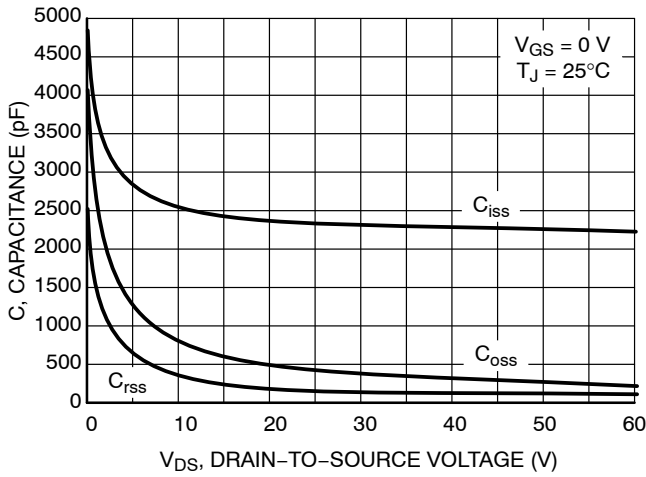


Figure 7. Capacitance Variation

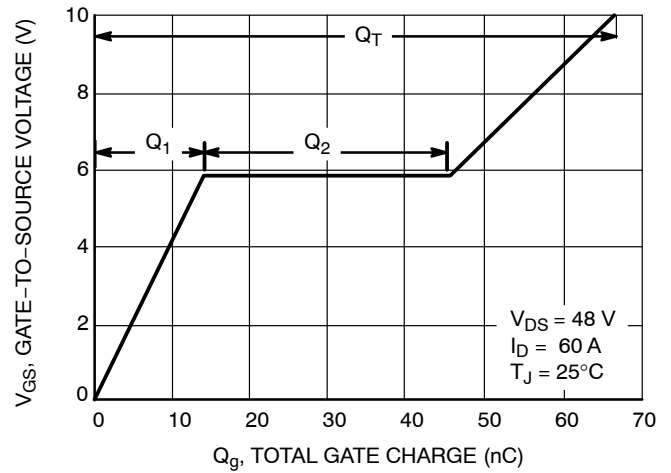


Figure 8. Gate-to-Source Voltage vs. Total Charge

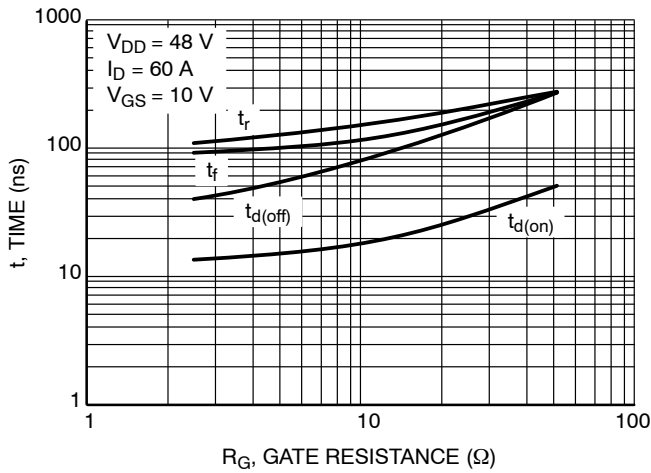


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

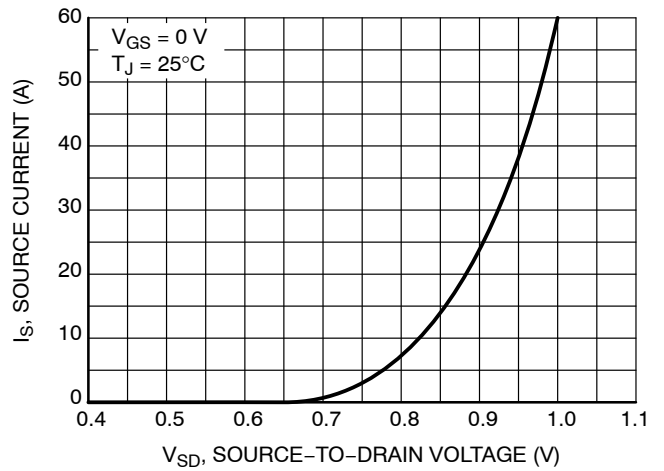


Figure 10. Diode Forward Voltage vs. Current

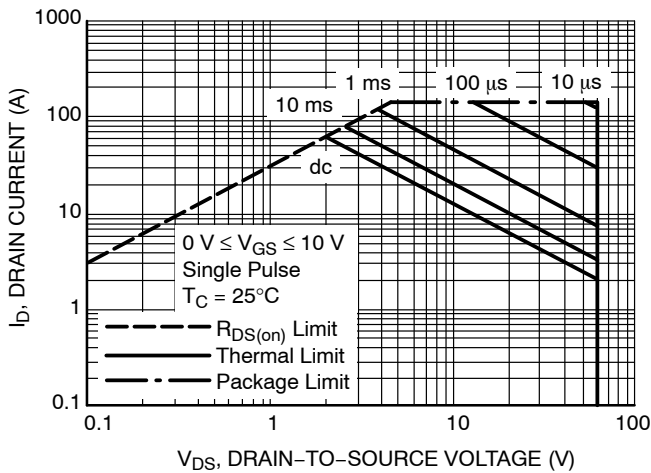


Figure 11. Maximum Rated Forward Biased Safe Operating Area

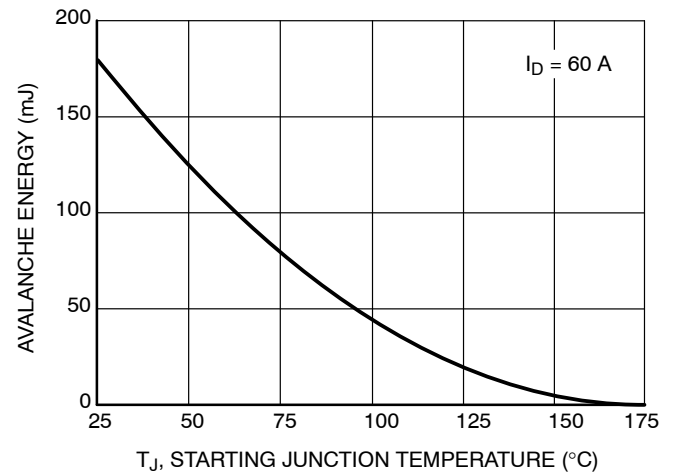


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

NTB5412N, NTP5412N

TYPICAL PERFORMANCE CURVES

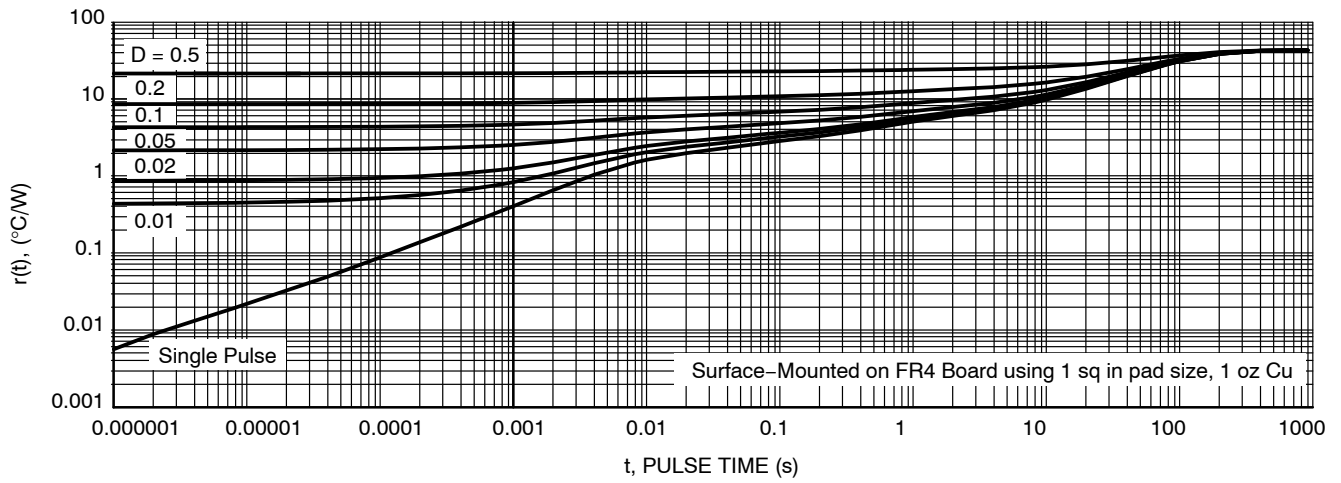


Figure 13. Thermal Response

ORDERING INFORMATION

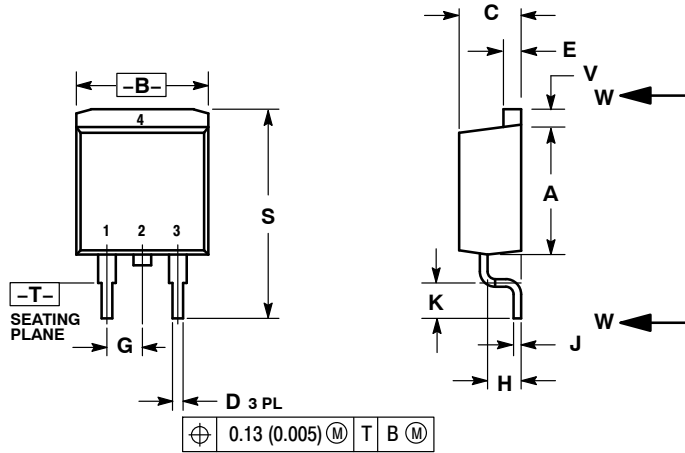
Device	Package	Shipping [†]
NTP5412NG	TO-220AB (Pb-Free)	50 Units / Rail
NTB5412NT4G	D ² PAK (Pb-Free)	800 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTB5412N, NTP5412N

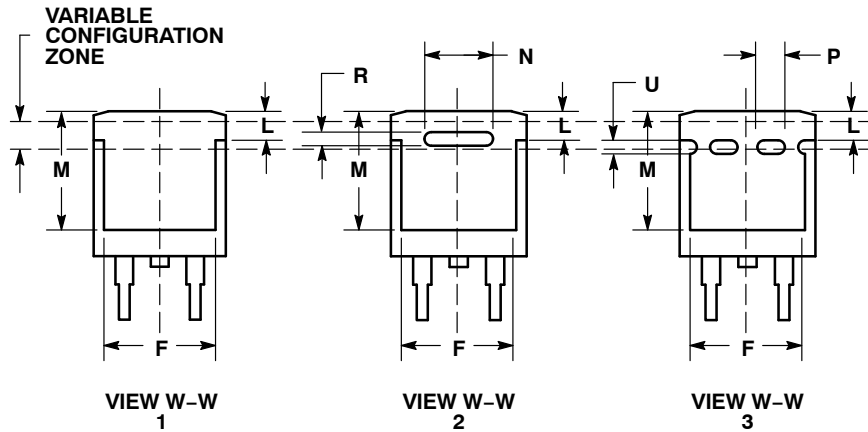
PACKAGE DIMENSIONS

D²PAK 3
CASE 418B-04
ISSUE K



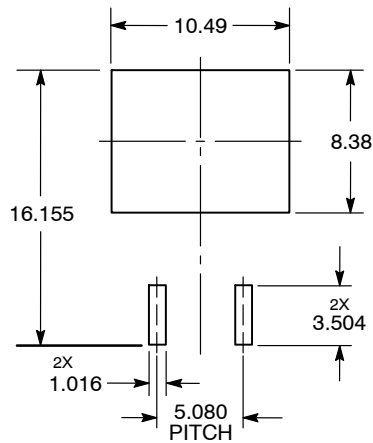
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40



- STYLE 2:
- PIN 1. GATE
 - DRAIN
 - SOURCE
 - DRAIN

SOLDERING FOOTPRINT*



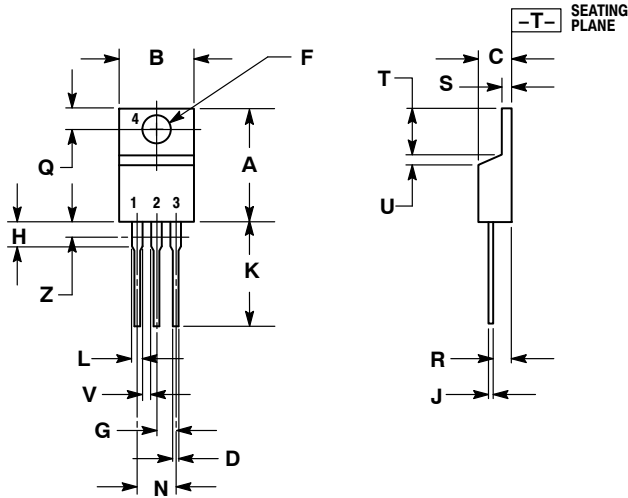
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTB5412N, NTP5412N

PACKAGE DIMENSIONS

TO-220
CASE 221A-09
ISSUE AF



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 5:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local
Sales Representative