TOSHIBA

TOSHIBA Original CMOS 8-Bit Microcontroller

TLCS-870 Series

TMP87P808NG
TMP87P808MG
TMP87P808LNG
TMP87P808LMG

Not Recommended for New Design

TOSHIBA CORPORATION

Semiconductor Company

Document Change Notification

The purpose of this notification is to inform customers about the launch of the Pb-free version of the device. The introduction of a Pb-free replacement affects the datasheet. Please understand that this notification is intended as a temporary substitute for a revision of the datasheet.

Changes to the datasheet may include the following, though not all of them may apply to this particular device.

1. Part number

   Example: TMPxxxxxxF → TMPxxxxxxFG

   All references to the previous part number were left unchanged in body text. The new part number is indicated on the prelims pages (cover page and this notification).

2. Package code and package dimensions

   Example: LQFP100-P-1414-0.50C → LQFP100-P-1414-0.50F

   All references to the previous package code and package dimensions were left unchanged in body text. The new ones are indicated on the prelims pages.

3. Addition of notes on lead solderability

   Now that the device is Pb-free, notes on lead solderability have been added.

4. RESTRICTIONS ON PRODUCT USE

   The previous (obsolete) provision might be left unchanged on page 1 of body text. A new replacement is included on the next page.

5. Publication date of the datasheet

   The publication date at the lower right corner of the prelims pages applies to the new device.

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1. Part number

2. Package code and dimensions

Previous Part Number (in Body Text)	Previous Package Code (in Body Text)	New Part Number	New Package Code	OTP
TMP87P808N	P-SDIP28-400-1.78	TMP87P808NG	SDIP28-P-400-1.78	—
TMP87P808M	P-SOP28-450-1.27	TMP87P808MG	SOP28-P-450-1.27B	—
TMP87P808LN	P-SDIP28-400-1.78	TMP87P808LNG	SDIP28-P-400-1.78	—
TMP87P808LM	P-SOP28-450-1.27	TMP87P808LMG	SOP28-P-450-1.27B	—

*: For the dimensions of the new package, see the attached Package Dimensions diagram.

3. Addition of notes on lead solderability

The following solderability test is conducted on the new device.

Lead solderability of Pb-free devices (with the G suffix)

Test	Test Conditions	Remark
Solderability	(1) Use of Lead (Pb) ·solder bath temperature = 230°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux (2) Use of Lead (Pb)-Free ·solder bath temperature = 245°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux	Leads with over 95% solder coverage till lead forming are acceptable.

4. RESTRICTIONS ON PRODUCT USE

The following replaces the "RESTRICTIONS ON PRODUCT USE" on page 1 of body text.

RESTRICTIONS ON PRODUCT USE 20070701-EN

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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.

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5. Publication date of the datasheet

The publication date of this datasheet is printed at the lower right corner of this notification.

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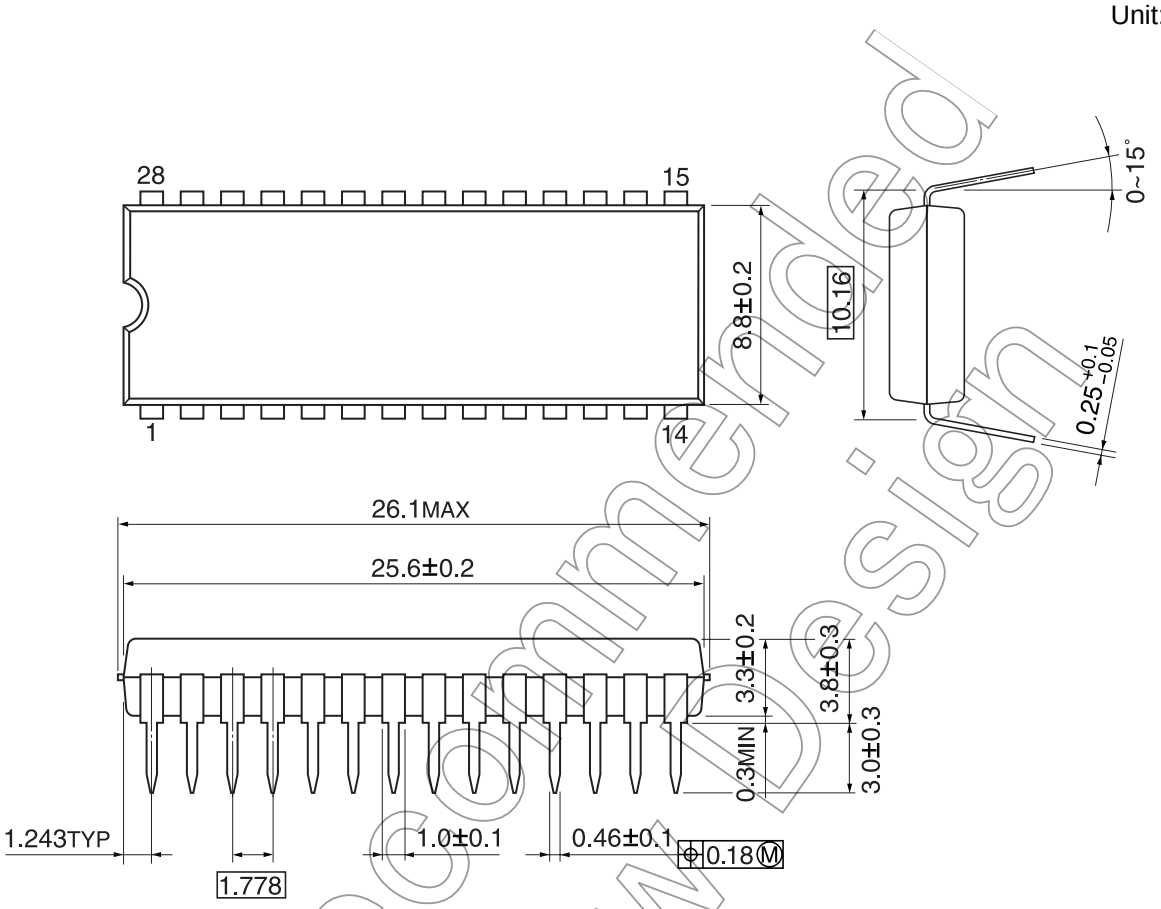
(Annex)

Package Dimensions

SDIP28-P-400-1.78

Unit: mm



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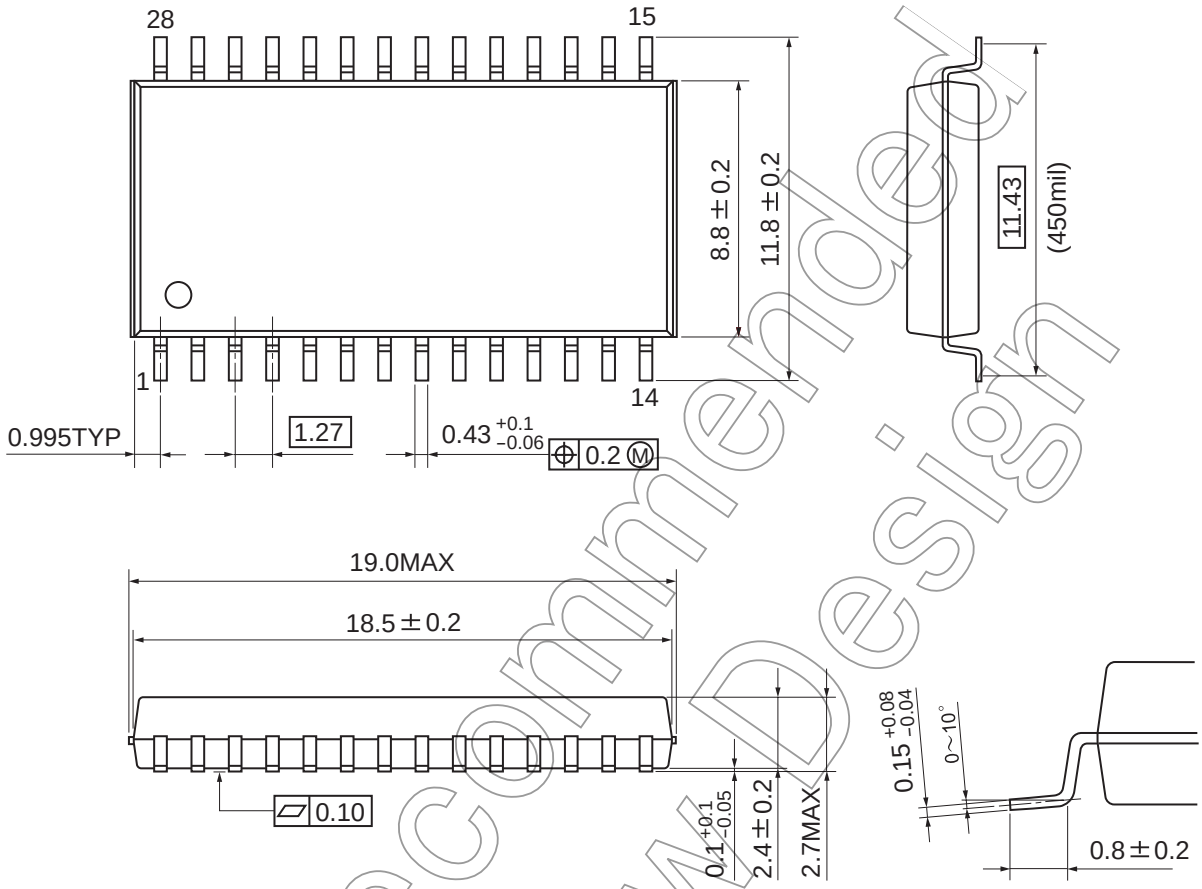
SOP28-P-450-1.27B

Unit: mm



Note: Palladium plated

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CMOS 8-Bit Microcontroller

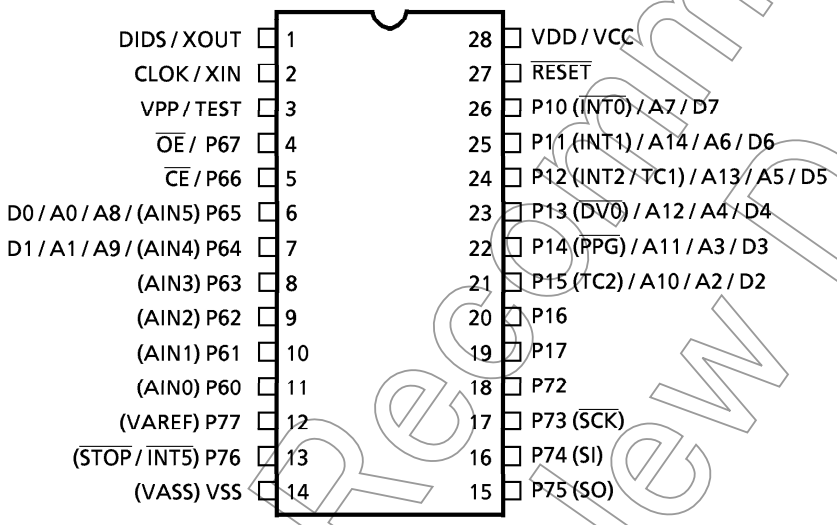
TMP87P808M, TMP87P808N
TMP87P808LM, TMP87P808LN

The 87P808/808L is a high-speed, high-performance 8-bit single chip microcomputer, which has 64K bits One-Time PROM. The 87P808/808L is pin compatible with the 87C408/808/408L/808L. The operations possible with the 87C408/808/408L/808L can be performed by writing programs to PROM. The 87P808/808L can write and verify in the same way as the TC57256AD using an adapter socket and a general-purpose PROM programmer.

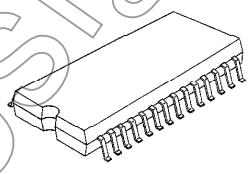
Part No.	ROM	RAM	Package	Adapter socket	Operation Voltage Range
TMP87P808M	8 K × 8-bit	256 × 8-bit	P-SOP28-450-1.27	BM11116	2.7 V to 5.5 V at 4.2 MHz
TMP87P808N			P-SDIP28-400-1.78	BM11122	4.5 V to 5.5 V at 8 MHz
TMP87P808LM			P-SOP28-450-1.27	BM11116	1.8 V to 4.0 V at 4.2 MHz
TMP87P808LN			P-SDIP28-400-1.78	BM11122	

Pin Assignments (Top View)

P-SOP28-400-1.78 / P-SDIP28-450-1.27

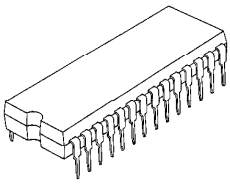


P-SOP28-450-1.27



TMP87P808M
TMP87P808LM

P-SDIP28-400-1.78



TMP87P808N
TMP87P808LN

000707EBP1

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Pin Function

The 87P808/808L has two modes: MCU and PROM.

(1) MCU mode

In this mode, the 87P808/808L is pin compatible with the 87C408/808/408L/808L (fix the TEST pin at low level).

(2) PROM mode

Pin Name (PROM mode)	Input / Output	Functions	Pin name (MCU mode)
A14 to A8	Input	Program memory address inputs	P10 to P15, P64, P65
A7 to A0			P10 to P15, P64, P65
D7 to D0	I/O	Program memory data input/outputs	P10 to P15, P64, P65
$\overline{CE}$	Input	Chip enable signal input	P66
$\overline{OE}$		Output enable signal input	P67
VPP	Power supply	+ 12.5 V / 5 V (Program supply voltage)	TEST
VCC		+ 5 V	VDD
GND		0 V	VSS
P17 to P16	I/O	PROM mode setting pins. Be fixed at low level.	
P63 to P60			
P77 to P72			
$\overline{RESET}$			
XIN	Input	Connect an 8 MHz oscillator to stabilize the internal state.	
XOUT	Output		
VAREF	Power supply	0 V (GND)	
VASS			

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Operational Description

The configuration and function of the 87P808/808L are the same as those of the 87C408/808/408L/808L, except in that a one-time PROM is used instead of an on-chip mask ROM.

1. Operating Mode

The 87P808/808L has two modes: MCU and PROM.

1.1 MCU Mode

The MCU mode is activated by fixing the TEST/VPP pin at low level.
In the MCU mode, operation is the same as with the 87C408/808/408L/808L (TEST/VPP pin cannot be used open because it has no built in pull-down resistance.)

1.1.1 Program Memory

The 87P808/808L have an 8 Kbytes (addresses E000 to FFFF$_H$ in the MCU mode, addresses 6000 to 7FFF$_H$ in the PROM mode) one-time PROM.
When the 87P808/808L is used as a system evaluation of the 87C408/808/408L/808L, the data is written to the program storage area shown in Figure 1-1.

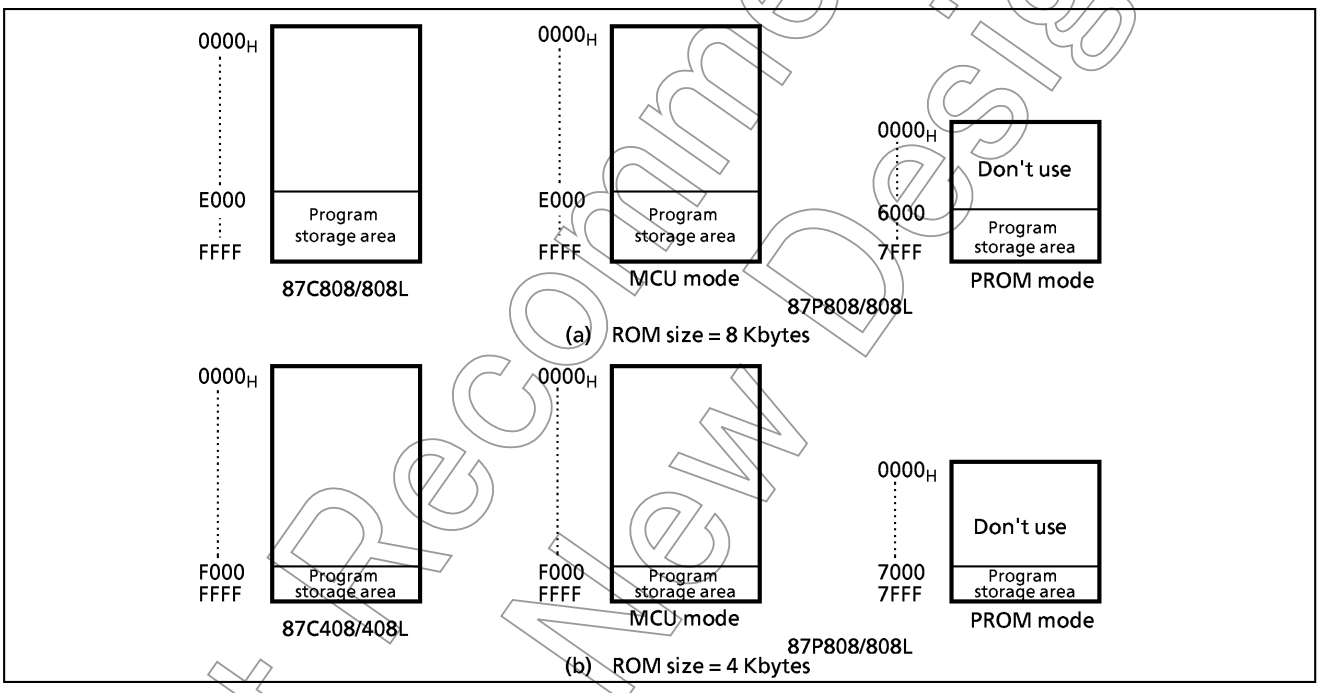

Figure 1-1. Program Memory Area

Note: Either write the data FFH to the unused area or set the general-purpose PROM programmer to access only the program storage area

1.1.2 Data Memory

The 87P808/808L has an 256 bytes data memory (static RAM).

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1.1.3 Input / Output Circuits

(1) Control pins
The control pins of the 87P808/808L are the same as those of the 87C408/808/408L/808L except that the TEST pin has no built-in pull-down resistance.

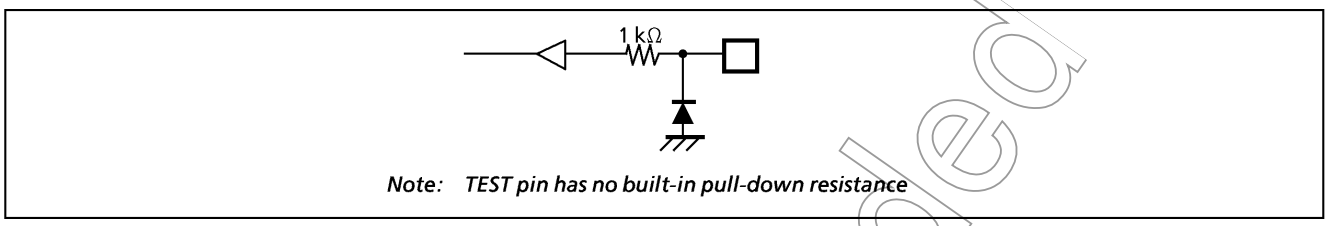

Figure 1-2. TEST Pin

(2) I/O port
The I/O circuits of 87P808/808L ports are the same as 87C408/808/408L/808L.

1.2 PROM Mode

The PROM mode is used to write and verify programs with a general-purpose PROM programmer.

Note: 24The high-speed programming mode (I, II) can be used for program operation. (Please set the high-speed programming mode according to each manual of PROM programmer.) The 87P808/808L is not supported an electric signature mode.

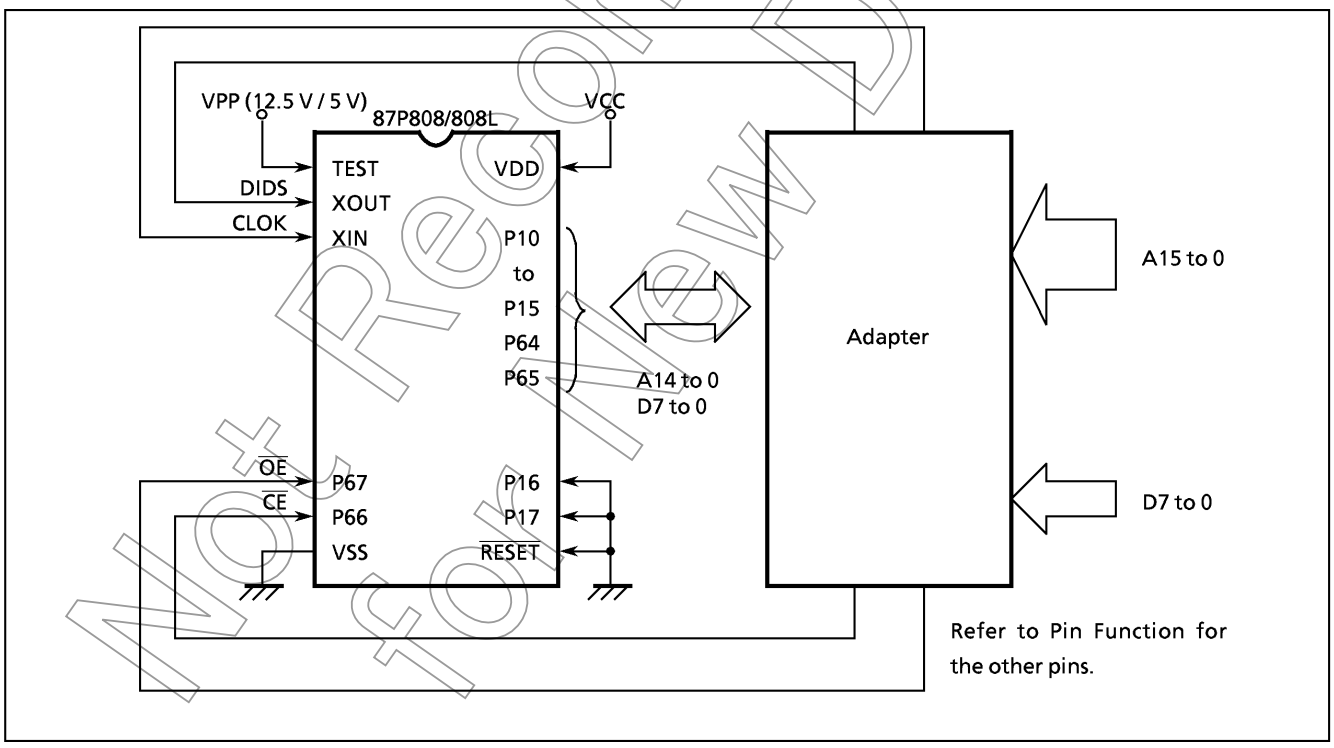

Figure 1-3. Setting for PROM Mode

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1.2.1 Programming Flowchart (High-speed Programming Mode-I)

The high-speed programming mode is achieved by applying the program voltage (+ 12.5 V) to the V_{PP} pin when Vcc = 6 V. After the address and input data are stable, the data is programmed by applying a single 1ms program pulse to the $\overline{CE}$ input. The programmed data is verified. If incorrect, another 1ms program pulse is applied and then the programmed data is verified. This process should be repeated (up to 25 times) until the program operates correctly. Programming for one address is ended by applying additional program pulse with width 3 times that needed for initial programming (number of programmed times × 1 ms). After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with $Vcc = V_{PP} = 5$ V.

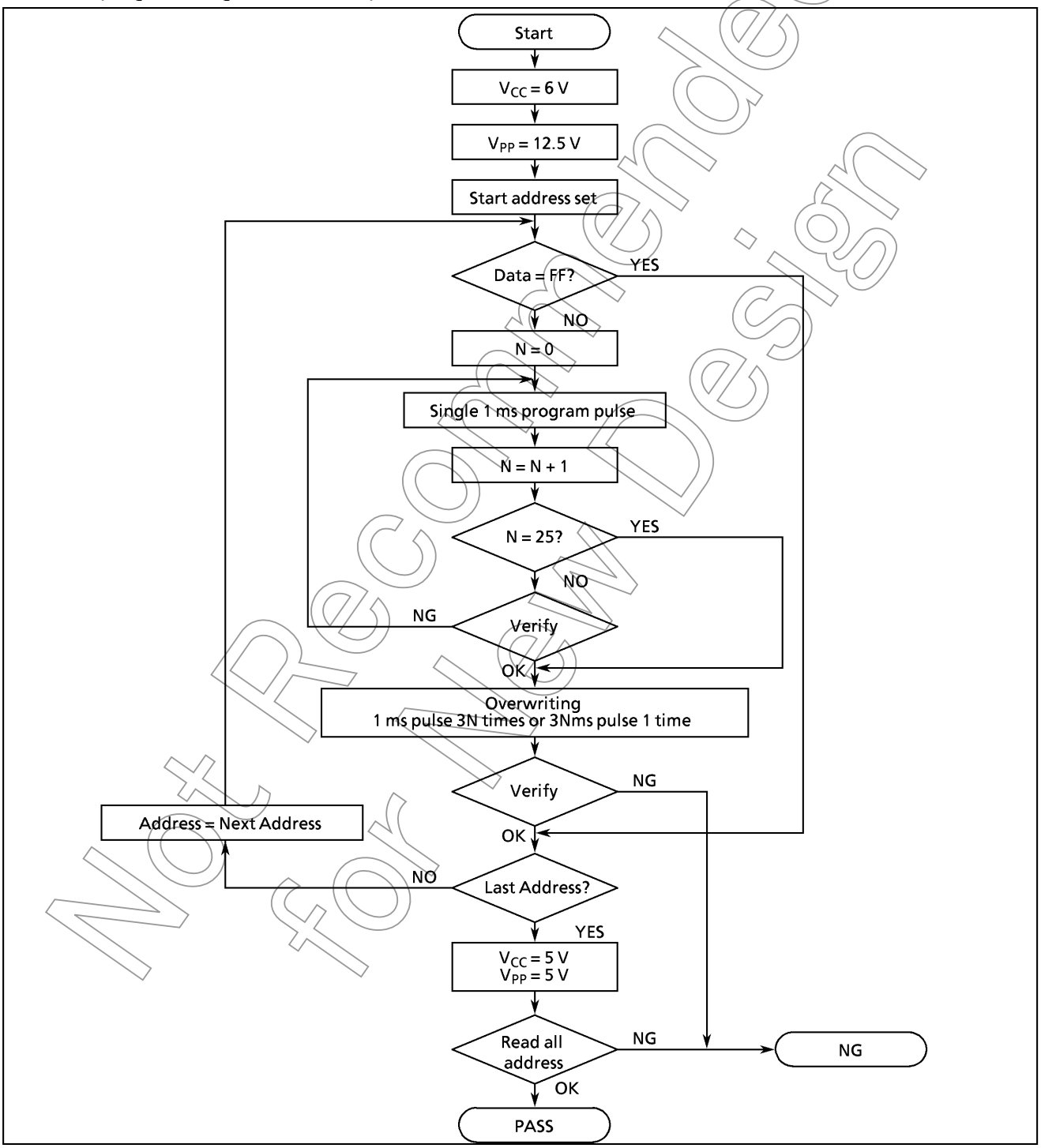

Figure 1-4. Flowchart of High-speed Programming Mode - I

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1.2.2 Programming Flowchart (High-speed Programming Mode-II)

The high-speed programming mode is achieved by applying the program voltage (+ 12.75 V) to the V_{PP} pin when Vcc = 6.25 V. After the address and input data are stable, the data is programmed by applying a single 0.1ms program pulse to the $\overline{CE}$ input. The programmed data is verified. If incorrect, another 0.1ms program pulse is applied and then the programmed data is verified. This process should be repeated (up to 25 times) until the program operates correctly. After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with $V_{CC} = V_{PP} = 5$ V.

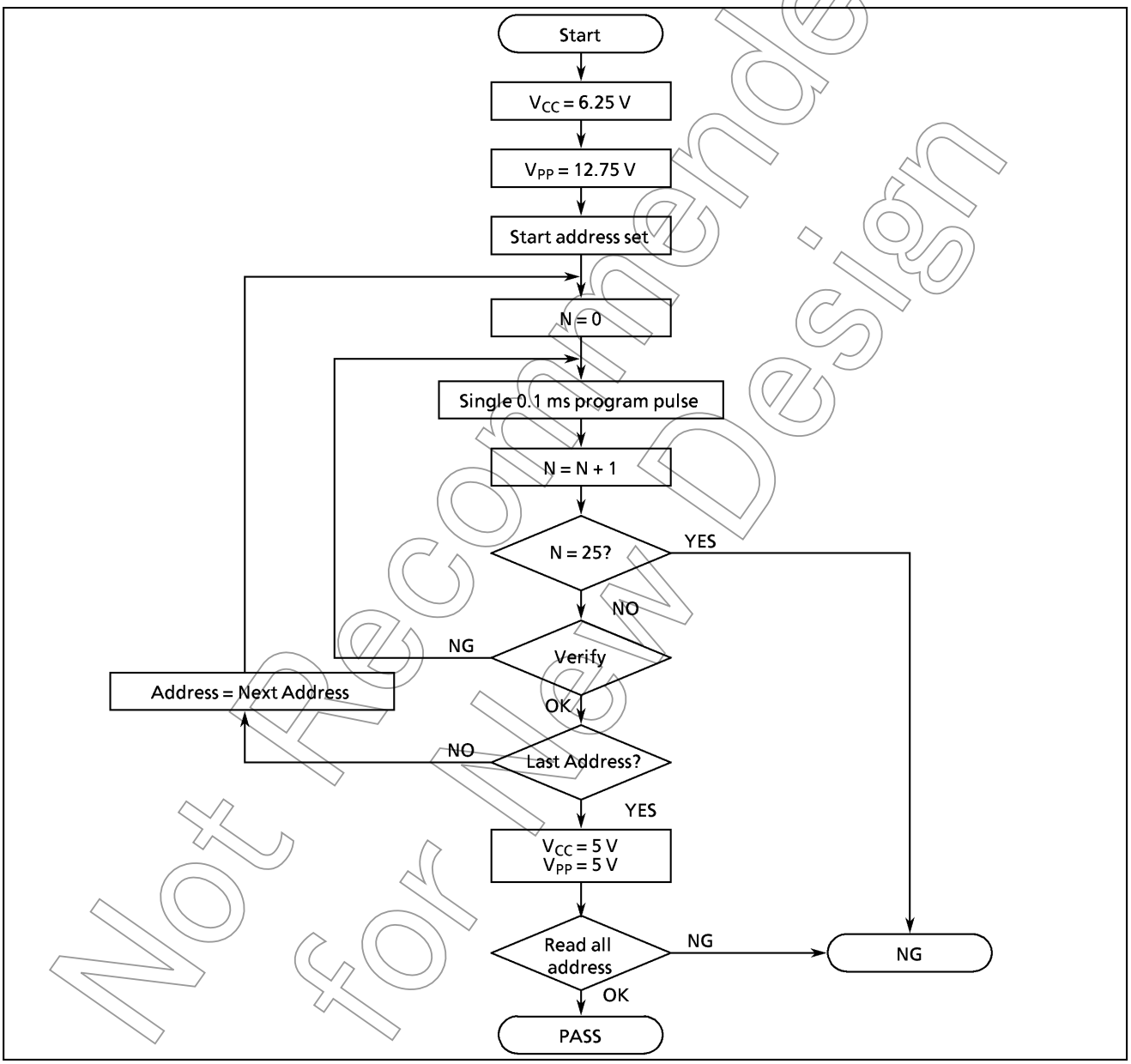

Figure 1-5. Flowchart of High-speed Programming Mode - II

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1.2.3 Writing Method for General-purpose PROM Program

(1) Adapters
BM11116: TMP87P808M/TMP87P808LM
BM11122: TMP87P808N/TMP87P808LN

(2) Adapter setting
Switch (SW1) is set to side N.

(3) PROM programmer specifying
i) PROM type is specified to TC57256AD.
Writing voltage: 12.5 V (high-speed program I mode)
12.75 V (high-speed program II mode)

ii) Data transfer (copy) (note 1)
In TMP87P808/808L, EPROM is within the addresses 6000 to $7FFF_H$. Data is required to be transferred (copied) to the addresses where it is possible to write. The program area in MCU mode and PROM mode is referred to "Program memory area" in Figure 1-1.

Ex. In the block transfer (copy) mode, executed as below.
ROM capacity of 4KB: transferred addresses F000 to $FFFF_H$ to addresses 7000 to $7FFF_H$

iii) Writing address is specified. (note 1)
Start address: 7000_H
End address: $7FFF_H$

(4) Writing
Writing/Verifying is required to be executed in accordance with PROM programmer operating procedure.

Note 1: The specifying method is referred to the PROM programmer description. The data in addresses 0000 to $5FFF_H$ must be specified to FF_H.

Note 2: When MCU is set to an adapter or the adapter is set to PROM programmer, a position of pin 1 must be adjusted. If the setting is reversed, MCU, the adapter and PROM program is damaged.

Note 3: TMP87P808/808L does not support the electric signature mode (hereinafter referred to as "signature"). If the signature is used in PROM program, a device is damaged due to applying 12 V ± 0.5 V to the address pin 9 (A9). The signature must not be used.

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Electrical Characteristics

(1) 87P808

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter		Symbol	Conditions		Ratings	Unit
Supply Voltage		V_{DD}			– 0.3 to 6.5	V
Program Voltage		V_{PP}	TEST /V_{PP} pin		– 0.3 to 13.0	V
Input Voltage		V_{IN}			– 0.3 to V_{DD} + 0.3	V
Output Voltage		V_{OUT}			– 0.3 to V_{DD} + 0.3	V
Output Current (Per 1 pin)	IOL	I_{OUT1}	P1, P6		3.2	mA
		I_{OUT2}	P7 (Middle current port)		15	mA
	IOH	I_{OUT3}	P1, P6, P7		– 1.8	mA
Output Current (Total)	IOL	ΣI_{OUT1}	P1, P6		50	mA
		ΣI_{OUT2}	P7 (Middle current port)		60	mA
	IOH	ΣI_{OUT3}	P1, P6, P7		30	mA
Power Dissipation [Topr = 70°C]		PD		SDIP	300	mW
				SOP	180	
Soldering Temperature (time)		Tsld			260 (10 s)	°C
Storage Temperature		Tstg			– 55 to 125	°C
Operating Temperature		Topr			– 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = –30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 8 MHz	NORMAL mode	4.5	5.5	V
				IDLE mode			
			fc = 4.2 MHz	NORMAL mode	2.7		
				IDLE mode			
				STOP mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		2.7 V $\leqq V_D <$ 4.5 V		$V_{DD} \times 0.90$		
	V_{IH4}		$V_{DD} <$ 2.7 V		$V_{DD} \times 0.95$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		2.7 V $\leqq V_{DD} <$ 4.5 V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V		1.0	8.0	MHz
			V_{DD} = 2.7 to 5.5 V			4.2	

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc: Supply voltage range is specified in NORMAL mode and IDLE mode.

Note 3: Minimum of clock frequency: 1 MHz ≦ fcgck

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D.C. Characteristics

(V_{SS} = 0 V, Topr = –30 to 70°C)

Parameter	Symbol	PINS	Conditions			Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis inputs				–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V V_{IN} = 5.5 V / 0 V			–2	–	2	μA
	I_{IN2}	Tri-state ports							
	I_{IN3}	RESET, STOP							
Input Resistance	R_{IN1}	TEST				30	70	150	kΩ
	R_{IN2}	$\overline{\text{RESET}}$				100	220	450	
	R_{IN3}	STOPi	i = 2 to 5			30	130	250	
Output Leak Current	I_{LO}	Tri-state ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V / 0V			–2	–	2	μA
Output High Voltage	V_{OH2}	Tri-state ports Ports P1, P6	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA			4.1	–	–	V
Low Output Voltage	V_{OL}	Except XOUT and P7	V_{DD} = 4.5V, I_{OL} = 1.6 mA			–	–	0.4	V
Low Output Current	I_{OL3}	P7	V_{DD} = 4.5 V, V_{OL} = 1.0 V			–	7	–	mA
Supply Current in NORMAL mode	I_{DD}		V_{DD} = 5.5 V fc = 8 MHz V_{IN} = 5.3 V / 0.2V	fcgck	fc	–	7.0	11	mA
					fc/2	–	4.4	7.0	
					fc/4	–	2.8	5.1	
					fc/8	–	2.2	4.5	
Supply Current in IDLE mode				fcgck	fc	–	3.6	5.5	
					fc/2	–	2.6	4.2	
					fc/4	–	2.0	3.7	
					fc/8	–	1.7	3.5	
Supply Current in NORMAL mode			V_{DD} = 3.0 V fc = 4.19 MHz V_{IN} = 2.8 V / 0.2V	fcgck	fc	–	1.7	2.8	
					fc/2	–	1.1	2.0	
					fc/4	–	0.7	1.4	
Supply Current in IDLE mode				fcgck	fc	–	0.9	1.6	
					fc/2	–	0.7	1.4	
					fc/4	–	0.5	1.0	
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V			–	0.5	10	μA

Note 1: Typical values show those at Topr = 25°C, VDD = 5 V.
Note 2: Input Current I_{IN1}, I_{IN3}: The current through resistor is not included, when the input resistor (pull-up or pull-down) is contained.
Note 3: I_{DD} ; Except for I_{REF}

A/D Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5V, Topr = –30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		2.7	–	V_{DD}	V
	V_{ASS}		V_{SS}			
Analog Input Voltage Range	V_{AIN}		V_{ASS}	–	V_{AREF}	V
Analog Reference Current	I_{REF}	V_{AREF} = 5.5 V, V_{ASS} (V_{SS}) = 0.0 V	–	0.8	1.0	mA
Nonlinearity Error		V_{DD} = 5.0 V, V_{AREF} = 5.000 V V_{ASS} (V_{SS}) = 0.000 V or V_{DD} = 2.7 V, V_{AREF} = 2.700 V V_{ASS} (V_{SS}) = 0.000 V	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

Note: Quantizing error is not contained in those errors.

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A.C. Characteristics (I)

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = –30 to 70°C)

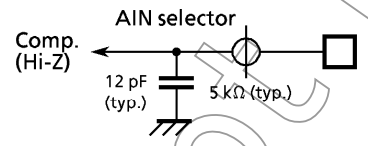
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Timer	tcy	In NORMAL mode	0.5	–	4	μs
		In IDLE mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation	50	–	–	ns
Low Level Clock Pulse Width	t_{WCL}	fc = 8 MHz				
A/D Conversion Time	t_{ADC}	ACK = 0	–	46	–	tcy
		ACK = 1		184		
A/D Sampling Time	t_{AIN}		–	4	–	

A.C. Characteristics (II)

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 30 to 70°C)

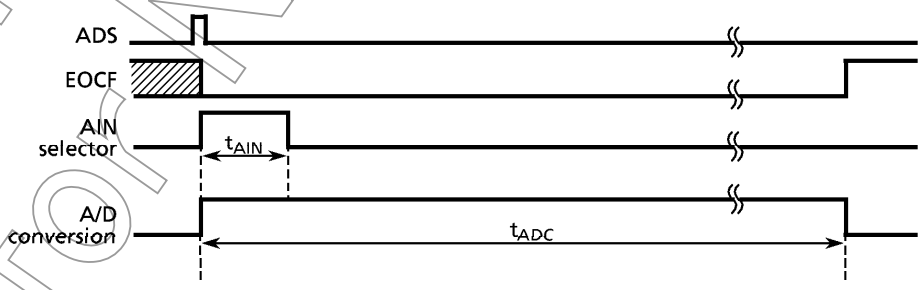
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	In NORMAL mode	0.95	–	4	μs
		In IDLE mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation	110	–	–	ns
Low Level Clock Pulse Width	t_{WCL}	fc = 4.2 MHz				
A/D Conversion Time	t_{ADC}	ACK = 0	–	46	–	tcy
		ACK = 1		184		
A/D Sampling Time	t_{AIN}		–	4		

Note: A/D conversion timing:
Internal circuit for AIN0 to 5



※ To maintain a precision of A/D conversion, internal condenser must be charged until t_{AIN} is over.

A/D conversion timing



Not Recommended for New Design

Recommended Oscillating Conditions (Ⅰ)

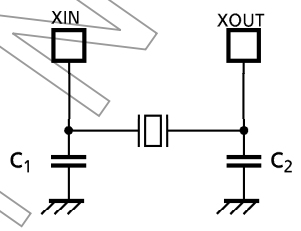
(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Conditions C_1	Recommended Conditions C_2
High-frequency Oscillation	Ceramic Resonator	8 MHz (VDD = 4.5 to 5.5 V)	KYOCERA	KBR8.0M	30 pF	30 pF
			MURATA	CSAC8.00MT	30 pF	30 pF
			MURATA	CSA8.00MTZ CST8.00MTW CSTS8.00MT	—	—
		4.19 MHz (VDD = 2.7 to 5.5 V)	MURATA	CSA4.19MG	30 pF	30 pF
			MURATA	CST4.19MGW	—	—
		4 MHz (VDD = 2.7 to 5.5 V)	KYOCERA	KBR4.0MS	30 pF	30 pF
	Crystal Oscillator	8 MHz (VDD = 4.5 to 5.5 V)	TOYOCOM	210B 8.0000	20 pF	20 pF
		4 MHz (VDD = 2.7 to 5.5 V)	TOYOCOM	204B 4.000		

Recommended Oscillating Conditions (Ⅱ)

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Conditions C_1	Recommended Conditions C_2
High-frequency Oscillation	Ceramic Resonator	4.19 MHz (VDD = 2.7 to 5.5 V)	MURATA	CSA4.19MG	30 pF	30 pF
			MURATA	CST4.19MGW	—	—
		4 MHz (VDD = 2.7 to 5.5 V)	MURATA	CSA4.00MG	30 pF	30 pF
				CSA4.00MGC	—	—
			MURATA	CST4.00MGW CSTC4.00MG	—	—
			MURATA	CSTCS4.00MG	—	—



(1) High-frequency Oscillation

Note: When used in high electric field such as a picture tube, the package is recommended to be electrically shielded to maintain a regular operation.

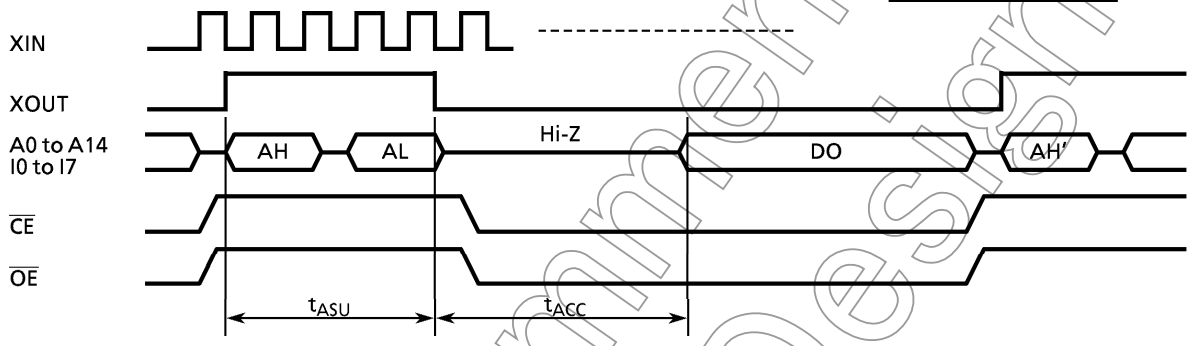
Not Recommended for New Design

D.C. Characteristics, A.C. Characteristics (V_{SS} = 0 V)

(1) Read Operation (T_{opr} = 0 to 70°C)

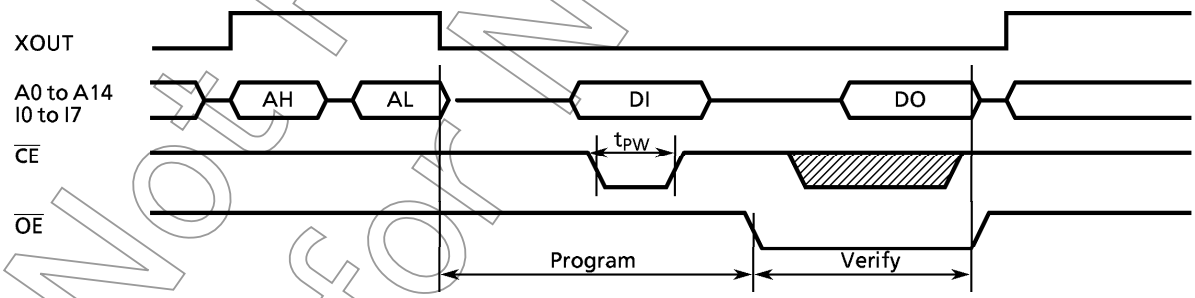
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input High Voltage	V_{IH4}		$V_{CC} \times 0.67$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.3$	V
Supply Voltage	V_{CC}		4.75	5.00	5.25	V
Program Supply Voltage	V_{PP}		$V_{CC} - 0.6$	V_{CC}	$V_{CC+0.6}$	
Address Set-up Time	t_{ASU}		400	–	–	ns
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25 V	–	5tcyc	–	ns

Note: tcyc = 400 ns



(2) Program Operation (High speed write mode - Ⅰ) (Topr = 25 ± 5°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.12$	V
Supply Voltage	V_{CC}		5.75	6.0	6.25	V
Program Supply Voltage	V_{PP}		12.0	12.5	13.0	V
Initial Program Pulse Width	t_{PW}	V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.25 V	0.95	1.0	1.05	ms



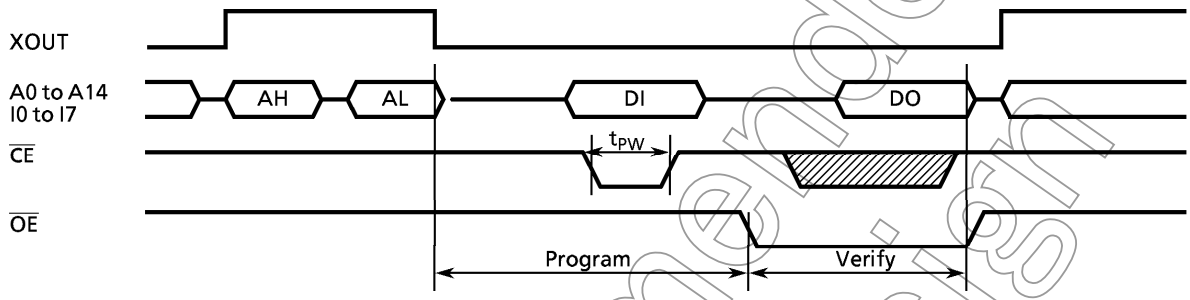
Note: DO ; Data output (I0 to I7) AL ; Address input (A0 to A7)
DI ; Data input (I0 to I7) AH ; Address input (A8 to A14)

Note 1: When V_{CC} power supply is turned on or after, V_{PP} must be increased.
When V_{CC} power supply is turned off or before, V_{PP} must be decreased.
Note 2: The device must not be set to the EPROM programmer or picked up from it under applying the program voltage (12.5 V ± 0.5 V) to the V_{PP} pin as the device is damaged.
Note 3: Be sure to execute the recommended programing mode with the recommended programing adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.

Not Recommended for New Design

(3) Program Operation (High speed write mode - II) (Topr = 25 ± 5°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.12$	V
Supply Voltage	V_{CC}		6.00	6.25	6.50	V
Program Supply Voltage	V_{PP}		12.50	12.75	13.0	V
Initial Program Pulse Width	t_{PW}	V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 V ± 0.25 V	0.095	0.1	0.105	ms



Note: DO ; Data output (I0 to I7) AL ; Address input (A0 to A7)
DI ; Data input (I0 to I7) AH ; Address input (A8 to A14)

Note 1: When V_{CC} power supply is turned on or after, V_{PP} must be increased.
When V_{CC} power supply is turned off or before, V_{PP} must be decreased.
Note 2: The device must not be set to the EPROM programmer or picked up from it under applying the program voltage (12.5 V ± 0.5 V) to the V_{PP} pin as the device is damaged.
Note 3: Be sure to execute the recommended programing mode with the recommended programing adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.

Recommended EPROM Programmer

DATA I/O	UNISTTE (SITE40)
ADVANTEST	R4945A
AVAL DATA	PECKER11 MARK-II (version 5.5)

Not Recommended for New Design

Electrical Characteristics

(1) 87P808L

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter		Symbol	Conditions		Ratings	Unit
Supply Voltage		V_{DD}			– 0.3 to 6.5	V
Program Voltage		V_{PP}	TEST /V_{PP} pin		– 0.3 to 13.0	V
Input Voltage		V_{IN}			– 0.3 to V_{DD} + 0.3	V
Output Voltage		V_{OUT}			– 0.3 to V_{DD} + 0.3	V
Output Current (Per 1 pin)	IOL	I_{OUT1}	P1, P6		3.2	mA
		I_{OUT2}	P7 (Middle current port)		15	mA
	IOL	I_{OUT3}	P1, P6, P7		– 1.8	mA
Output Current (Total)	IOL	ΣI_{OUT1}	P1, P6		50	mA
		ΣI_{OUT2}	P7 (Middle current port)		60	mA
	IOL	ΣI_{OUT3}	P1, P6, P7		30	mA
Power Dissipation [Topr = 70°C]		PD		SDIP	300	mW
				SOP	180	
Soldering Temperature (time)		Tsld			260 (10 s)	°C
Storage Temperature		Tstg			– 55 to 125	°C
Operating Temperature		Topr			– 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = –30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 4.2 MHz	NORMAL mode	1.8	4.0	V
				IDLE mode			
			STOP mode				
Input High Voltage	V_{IH}				V_{DD} × 0.90	V_{DD}	V
Input Low Voltage	V_{IL}				0	V_{DD} × 0.10	V
Clock Frequency	fc	XIN, XOUT	V_{DD} = 1.8 to 4.0 V		1.0	4.2	MHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc: Supply voltage range is specified in NORMAL mode and IDLE mode.

Note 3: Minimum of clock frequency: 1 MHz ≦ fcgck

Not Recommended for New Design

D.C. Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	PINS	Conditions			Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis inputs				–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 4.0 V V_{IN} = 4.0 V / 0 V			–2	–	2	μA
	I_{IN2}	Tri-state ports							
	I_{IN3}	RESET, STOP							
Input Resistance	R_{IN1}	TEST				30	70	150	kΩ
	R_{IN2}	RESET				100	220	450	
	R_{IN3}	STOPi	i = 2 to 5			30	130	250	
Output Leakl Current	I_{LO}	Tri-state ports	V_{DD} = 4.0 V, V_{OUT} = 4.0 V / 0V			–2	–	2	μA
Output High Voltage	V_{OH2}	Tri-state ports	V_{DD} = 4.0 V, I_{OH} = – 0.5 mA			3.6	–	–	V
Output Low Voltage	V_{OL}	Except XOUT and P7	V_{DD} = 4.0V, I_{OL} = 1.3 mA			–	–	0.4	V
Output Low Current	I_{OL3}	P7	V_{DD} = 4.0 V, V_{OL} = 1.0 V			–	6	–	mA
Supply Current in NORMAL mode	I_{DD}		V_{DD} = 4 V fc = 4.19 MHz V_{IN} = 3.8 V / 0.2V	fcgck	fc	–	2.25	3.6	mA
					fc/2	–	1.35	2.5	
					fc/4	–	0.9	1.9	
					fc/8	–	0.7	1.65	
Supply Current in IDLE mode				fcgck	fc	–	1.2	1.9	
					fc/2	–	0.9	1.7	
					fc/4	–	0.7	1.5	
					fc/8	–	0.6	1.4	
Supply Current in NORMAL mode			V_{DD} = 3.0 V fc = 4.19 MHz V_{IN} = 2.8 V / 0.2V	fcgck	fc	–	1.5	2.5	
					fc/2	–	0.85	1.6	
					fc/4	–	0.6	1.2	
					fc/8	–	0.4	1.0	
Supply Current in IDLE mode				fcgck	fc	–	0.8	1.4	
					fc/2	–	0.55	1.1	
					fc/4	–	0.45	0.9	
					fc/8	–	0.35	0.85	
Supply Current in NORMAL mode			V_{DD} = 1.8 V fc = 4.19 MHz V_{IN} = 1.6 V / 0.2V	fcgck	fc	–	0.9	1.3	
					fc/2	–	0.5	0.8	
					fc/4	–	0.3	0.45	
					fc/8	–	0.2	0.35	
Supply Current in IDLE mode				fcgck	fc	–	0.35	0.5	
					fc/2	–	0.23	0.35	
					fc/4	–	0.17	0.26	
					fc/8	–	0.14	0.24	
Supply Current in STOP mode			V_{DD} = 4.0 V V_{IN} = 3.8 V / 0.2 V			–	0.5	10	μA

Note 1: Typical values show those at Topr = 25°C, VDD = 4 V.

Note 2: Input Current I_{IN1}, I_{IN3}: The current through resistor is not included, when the input resistor (pull-up or pull-down) is contained.

Note3: IDD ; Except for I_{REF}

Not Recommended for New Design

A/D Conversion Characteristics (Ⅰ)

(V_{DD} = 1.8 to 4.0 V, Topr = − 30 to 70°C, V_{SS} = 0V)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		1.8	−	V_{DD}	V
	V_{ASS}		V_{SS}			
Analog Input Voltage Range	V_{AIN}		V_{ASS}	−	V_{AREF}	V
Nonlinearity Error		1.8 V ≦ V_{AREF} < 2.7 V V_{AREF} ≦ V_{DD} ≦ 4.0 V_{ASS} (V_{SS}) = 0.000V ACK = 1 (Note2)	−	−	± 2	LSB
Zero Point Error			−	−	± 2	
Full Scale Error			−	−	± 2	
Total Error			−	−	± 4	

Note1: Quantizing error is not contained in those errors.
Note2: ACK ; bit5 of ADCCR (#000E_H) . conversion time = 184 tcy (175.6 μs / at fcgck = 4.19 MHz)

A/D Conversion Characteristics (Ⅱ)

(V_{SS} = 0V, V_{DD} = 2.7 to 4.0 V, Topr = − 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		2.7	−	V_{DD}	V
	V_{ASS}		V_{SS}			
Analog Input Voltage Range	V_{AIN}		V_{ASS}	−	V_{AREF}	V
Analog Reference Current	I_{REF}	V_{AREF} = 4.0V, V_{ASS} (V_{SS}) = 0.0V	−	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 4.0 V V_{AREF} = 4.000V V_{ASS} (V_{SS}) = 0.000V or V_{DD} = 2.7 V V_{AREF} = 2.700V V_{ASS} (V_{SS}) = 0.000V	−	−	± 1	LSB
Zero Point Error			−	−	± 1	
Full Scale Error			−	−	± 1	
Total Error			−	−	± 2	

Note: Quantizing error is not contained in those errors.

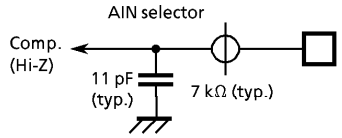
Not Recommended for New Design

A.C. Characteristics

(V_{SS} = 0 V, V_{DD} = 1.8 to 4.0 V, Topr = – 30 to 70°C)

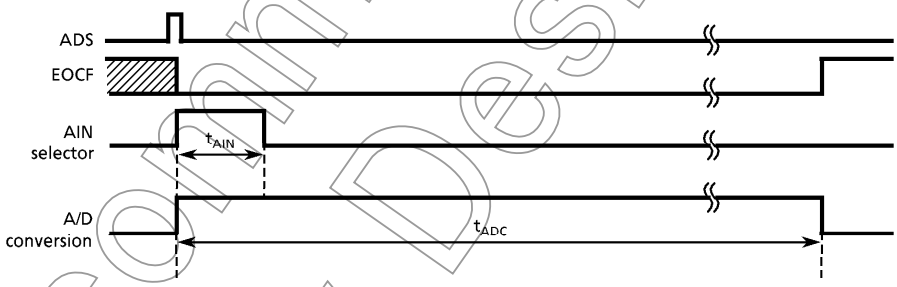
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	In NORMAL mode	0.95	–	4	μs
		In IDLE mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation	110	–	–	ns
Low Level Clock Pulse Width	t_{WCL}	fc = 4.2 MHz				
A/D Conversion Time	t_{ADC}	ACK = 0	–	46	–	tcy
		ACK = 1		184		
A/D Sampling Time	t_{AIN}		–	4		

Note: A/D conversion timing:
Internal circuit for AIN 0 to 5



※ To maintain a precision of A/D conversion, internal condenser must be charged until t_{AIN} is over.

A/D conversion timing

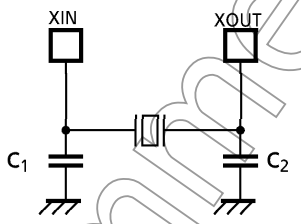


Not Recommended for New Design

Recommended Oscillating Conditions

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Conditions C_1	Recommended Conditions C_2
High-frequency Oscillation	Ceramic Resonator	4.19 MHz (VDD = 2.7 to 5.5 V)	MURATA	CSA4.19MG	30 pF	30 pF
			MURATA	CST4.19MGW	—	—
		4 MHz (VDD = 2.7 to 5.5 V)	MURATA	CSA4.00MG	30 pF	30 pF
				CSA4.00MGC	—	—
			MURATA	CST4.00MGW	—	—
				CSTC4.00MG		
			MURATA	CSTCS4.00MG	—	—



(1) High-frequency Oscillation

Note: When used in high electric field such as a picture tube, the package is recommended to be electrically shielded to maintain a regular operation.

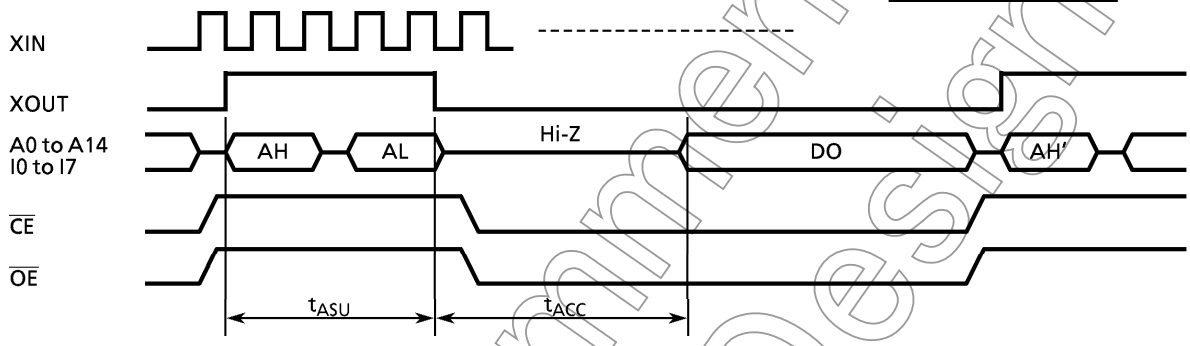
Not Recommended for New Design

D.C. Characteristics, A.C. Characteristics (V_{SS} = 0 V)

(1) Read Operation (T_{opr} = 0 to 70°C)

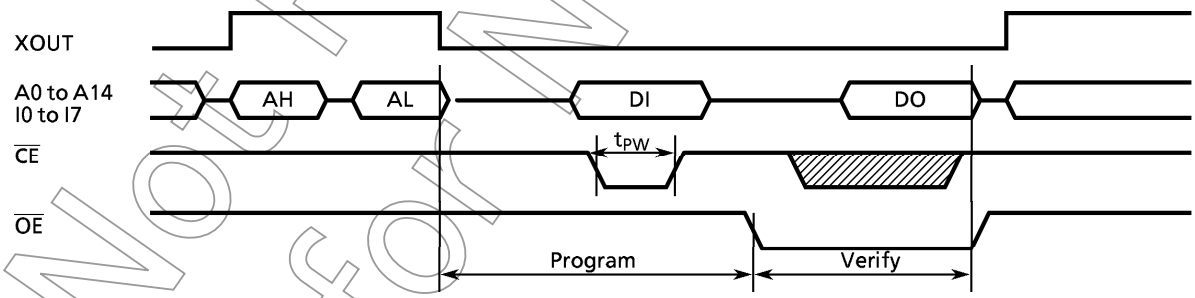
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input High Voltage	V_{IH4}		$V_{CC} \times 0.67$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.3$	V
Supply Voltage	V_{CC}		4.75	5.00	5.25	V
Program Supply Voltage	V_{PP}		$V_{CC} - 0.6$	V_{CC}	$V_{CC + 0.6}$	
Address Set-up Time	t_{ASU}		400	–	–	ns
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25 V	–	5tcyc	–	ns

Note: tcyc = 400 ns



(2) Program Operation (High speed write mode - Ⅰ) (Topr = 25 ± 5°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.12$	V
Supply Voltage	V_{CC}		5.75	6.0	6.25	V
Program Supply Voltage	V_{PP}		12.0	12.5	13.0	V
Initial Program Pulse Width	t_{PW}	V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.25 V	0.95	1.0	1.05	ms



Note: DO ; Data output (I0 to I7) AL ; Address input (A0 to A7)
DI ; Data input (I0 to I7) AH ; Address input (A8 to A14)

Note 1: When V_{CC} power supply is turned on or after, V_{PP} must be increased.
When V_{CC} power supply is turned off or before, V_{PP} must be decreased.

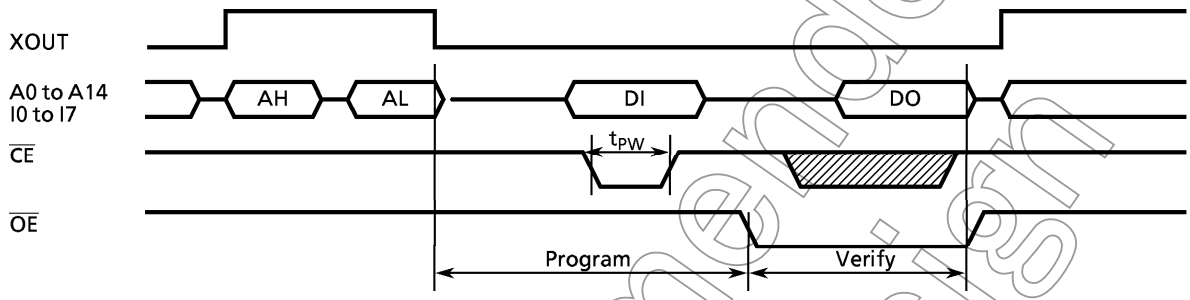
Note2: The device must not be set to the EPROM programmer or picked up from it under applying the program voltage (12.5 V ± 0.5 V) to the V_{PP} pin as the device is damaged.

Note3: Be sure to execute the recommended programing mode with the recommended programing adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.

Not Recommended for New Design

(3) Program Operation (High speed write mode - II) (Topr = 25 ± 5°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.12$	V
Supply Voltage	V_{CC}		6.00	6.25	6.50	V
Program Supply Voltage	V_{PP}		12.50	12.75	13.0	V
Initial Program Pulse Width	t_{PW}	V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 V ± 0.25 V	0.095	0.1	0.105	ms



Note: *DO ; Data output (I0 to I7)* *AL ; Address input (A0 to A7)*
DI ; Data input (I0 to I7) *AH ; Address input (A8 to A14)*

Note1: When V_{CC} power supply is turned on or after, V_{PP} must be increased.
When V_{CC} power supply is turned off or before, V_{PP} must be decreased.

Note2: The device must not be set to the EPROM programmer or picked up from it under applying the program voltage (12.5 V ± 0.5 V) to the V_{PP} pin as the device is damaged.

Note3: Be sure to execute the recommended programing mode with the recommended programing adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.

Recommended EPROM Programmer

DATA I/O	UNISTTE (SITE40)	
ADVANTEST	R4945A	
AVAL DATA	PECKER11	MARK-II (version 5.5)

Not Recommended for New Design