

August 1997

Features

- 70A, 55V
- **Ultra Low On-Resistance**, $r_{DS(ON)} = 0.012\Omega$
- **Diode Exhibits Both High Speed and Soft Recovery**
- **Temperature Compensating PSpice Model**
- **Thermal Impedance PSpice Model**
- **Peak Current vs Pulse Width Curve**
- **UIS Rating Curve**

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF75339G3	TO-247	75339G
HUF75339P3	TO-220AB	75339P
HUF75339S3	TO-262AA	75339S
HUF75339S3S	TO-263AB	75339S

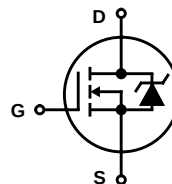
NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUF75339S3ST.

Description

The HUF75339 N-Channel power MOSFET is manufactured using the innovative *UltraFET™* process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

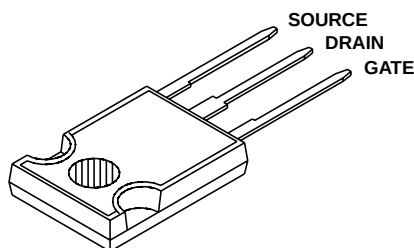
Formerly developmental type TA75339.

Symbol

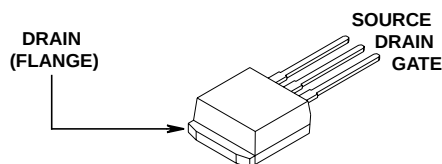


Packaging

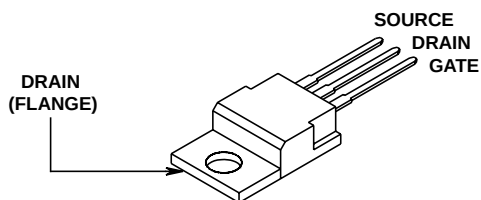
JEDEC TO-247



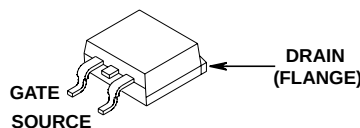
JEDEC TO-262AA



JEDEC TO-220AB



JEDEC TO-263AB



HUF75339G3, HUF75339P3, HUF75339S3, HUF75339S3S

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

Drain to Source Voltage	V_{DS}	55	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	V_{DGR}	55	V
Gate to Source Voltage	V_{GS}	± 20	V
Drain Current			
Continuous (Figure 2)	I_D	70	A
Pulsed Drain Current	I_{DM}	Figure 5	
Pulsed Avalanche Rating	E_{AS}	Figures 12, 14, 15	
Power Dissipation (Figure 4)	P_D	124	W
Derate Above 25°C (Figure 1)		0.83	W/ $^{\circ}\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	$^{\circ}\text{C}$
Soldering Temperature of Leads for 10s	T_L	260	$^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 10)		55	-	-	V
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 9)		2	-	4	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 50V, V _{GS} = 0V		-	-	1	μA
		V _{DS} = 45V, V _{GS} = 0V, T _C = 150 ⁰ C		-	-	250	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V		-	-	100	nA
Drain to Source On Resistance	r _{DS(ON)}	I _D = 70A, V _{GS} = 10V (Figure 8)		-	-	0.012	Ω
Turn-On Time	t _{ON}	V _{DD} = 30V, I _D ≅ 70A, R _L = 0.428Ω, V _{GS} = 10V, R _{GS} = 5.1Ω (Figures 18, 19)		-	-	110	ns
Turn-On Delay Time	t _{d(ON)}			-	15	-	ns
Rise Time	t _r			-	60	-	ns
Turn-Off Delay Time	t _{d(OFF)}			-	20	-	ns
Fall Time	t _f			-	25	-	ns
Turn-Off Time	t _{OFF}			-	-	70	ns
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 20V	V _{DD} = 30V, I _D ≅ 70A, R _L = 0.428Ω I _{g(REF)} = 1.0mA (Figures 13,16,17)	-	110	130	nC
Gate Charge at 10V	Q _{g(10)}	V _{GS} = 0V to 10V		-	60	75	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 2V		-	3.7	4.5	nC
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz (Figure 11)		-	2000	-	pF
Output Capacitance	C _{OSS}			-	700	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	160	-	pF
Thermal Resistance Junction to Case	R _{θJC}	(Figure 3)		-	-	1.21	°C/W
Thermal Resistance Junction to Ambient	R _{θJA}	TO-247		-	-	30	°C/W
		TO-220, TO-262, and TO-263		-	-	62	°C/W

Source to Drain Diode Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 70\text{A}$	-	-	1.25	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 70\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	85	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 70\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	160	nC

Typical Performance Curves

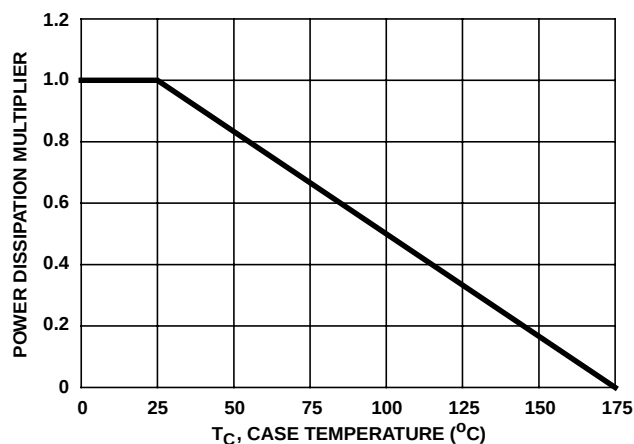


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

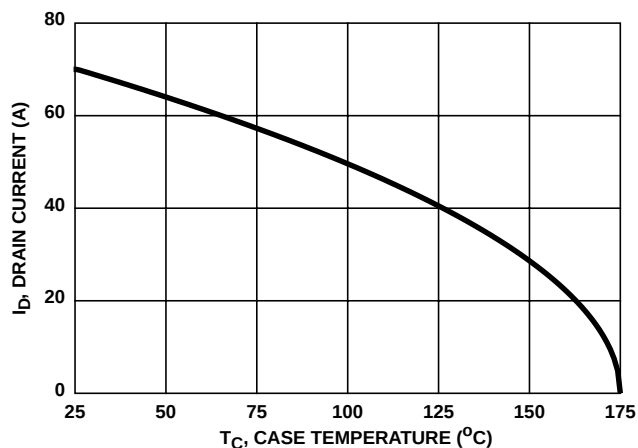


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

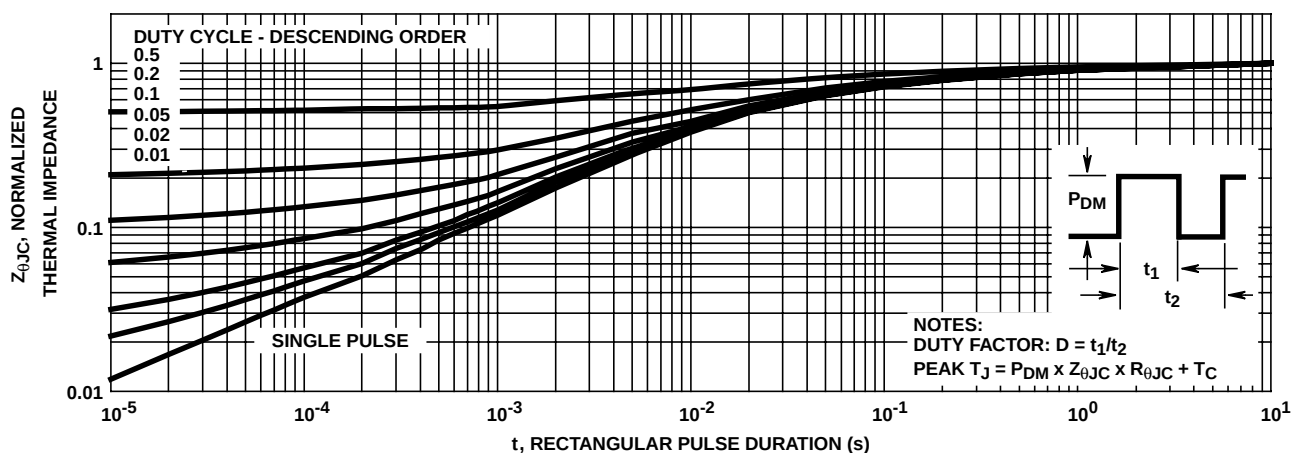


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

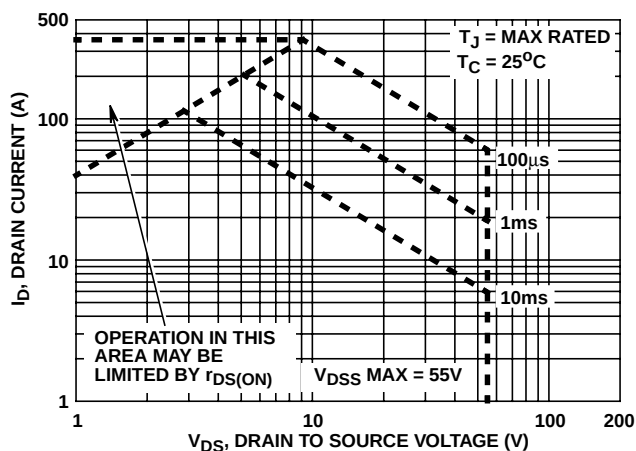


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

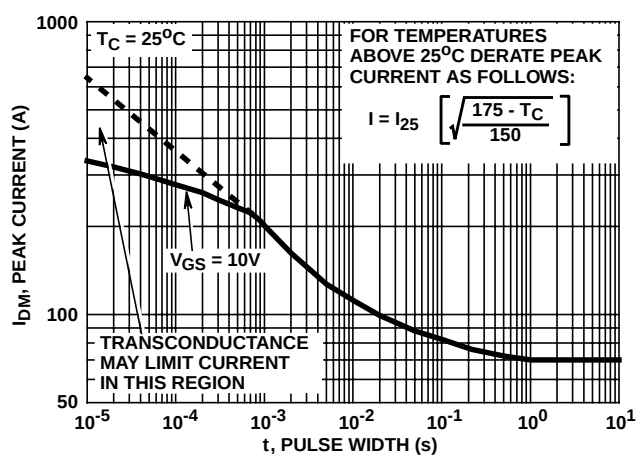


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

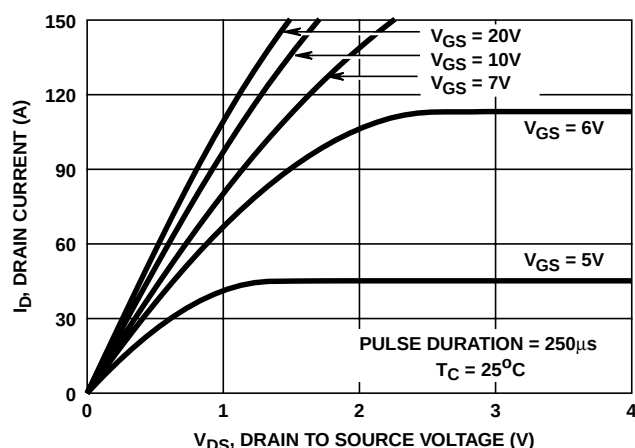


FIGURE 6. SATURATION CHARACTERISTICS

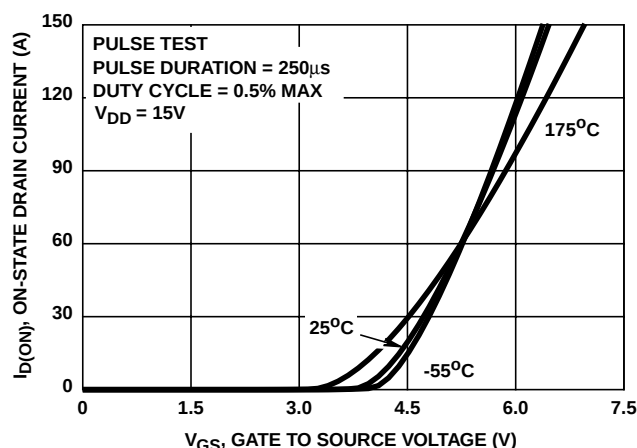


FIGURE 7. TRANSFER CHARACTERISTICS

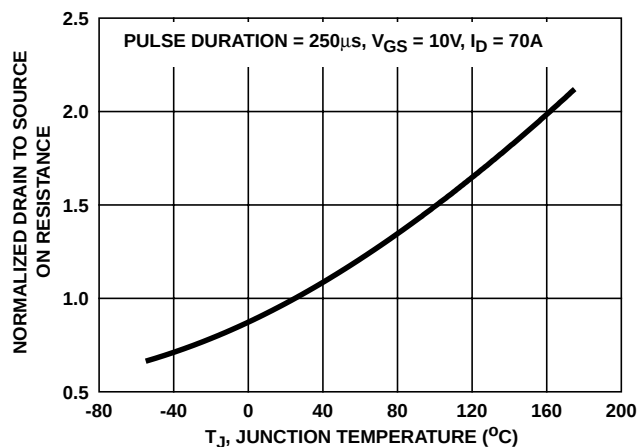


FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

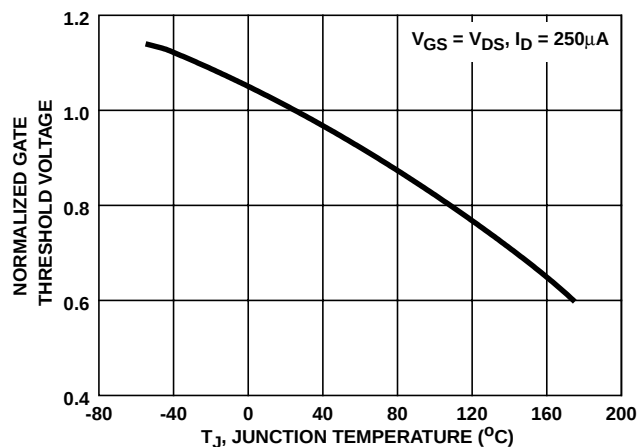


FIGURE 9. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

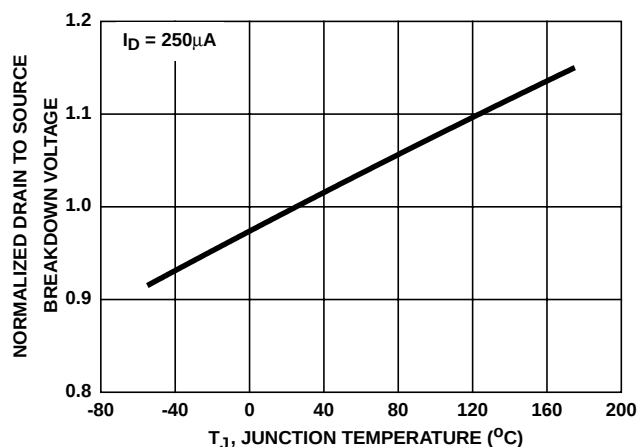


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

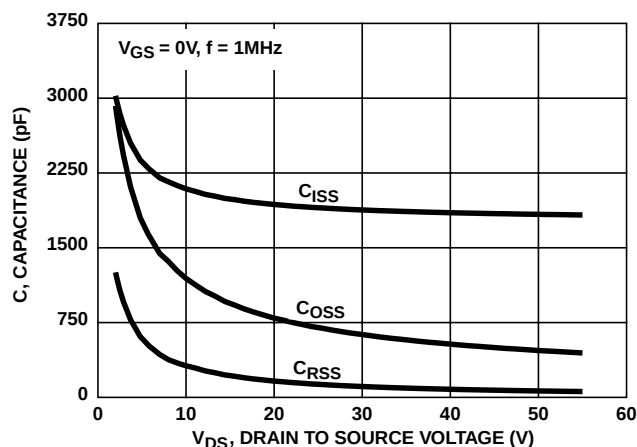
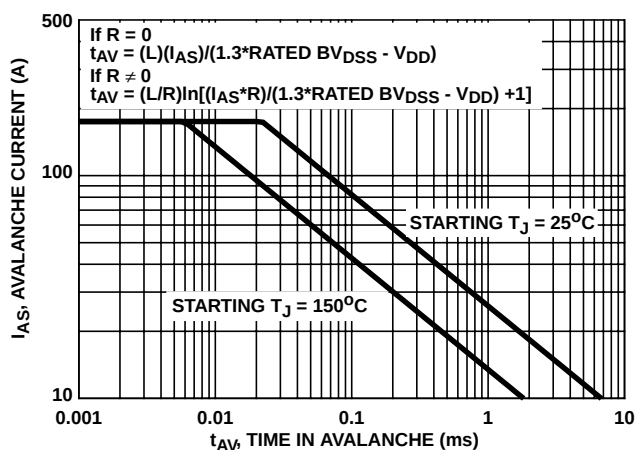


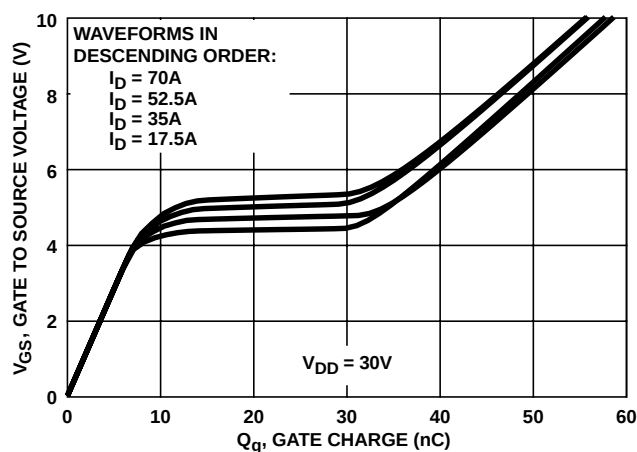
FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves (Continued)



NOTE: Refer to Harris Application Notes AN9321 and AN9322.

FIGURE 12. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

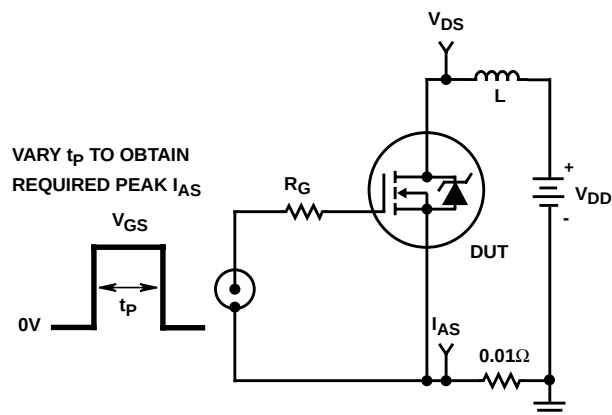


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

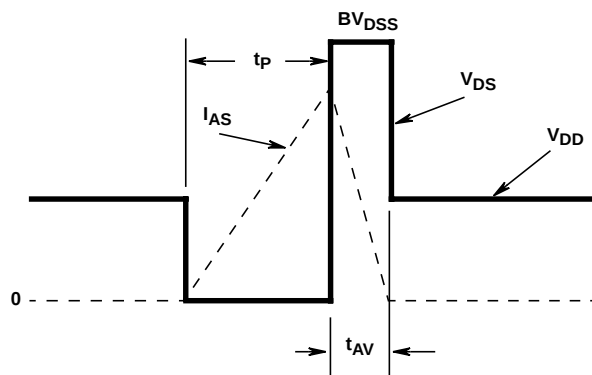


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

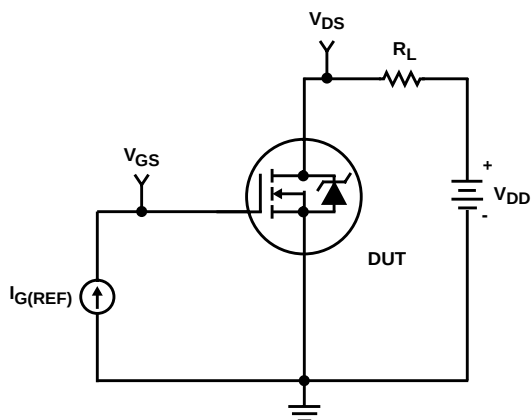


FIGURE 16. GATE CHARGE TEST CIRCUIT

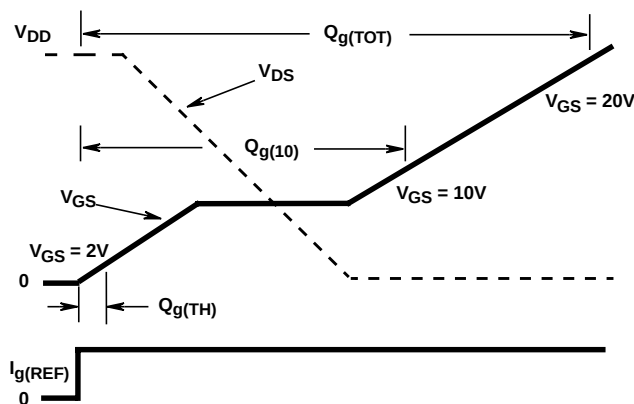


FIGURE 17. GATE CHARGE WAVEFORM

Test Circuits and Waveforms (Continued)

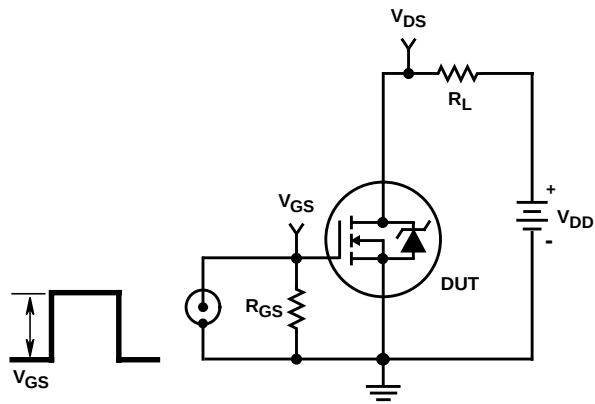


FIGURE 18. SWITCHING TIME TEST CIRCUIT

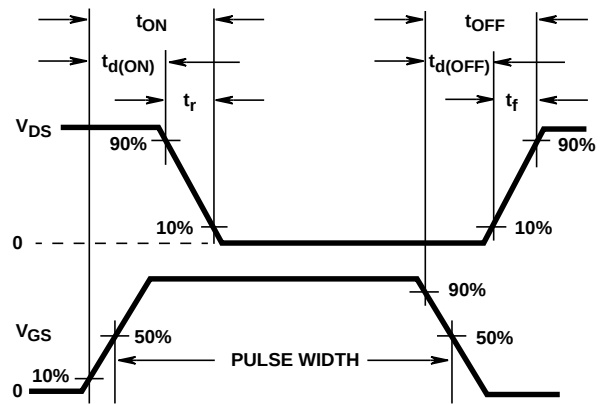


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

HUF75339G3, HUF75339P3, HUF75339S3, HUF75339S3S

PSICE Electrical Model

SUBCKT HUF75339 2 1 3 ; rev 6/25/97

CA 12 8 2.8e-9
CB 15 14 2.7e-9
CIN 6 8 1.77e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 59.2
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 2.0e-9
LSOURCE 3 7 4.69e-10
K1 LSOURCE LGATE 0.0302

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 1.95e-3
RGATE 9 20 0.34
RLDRAIN 2 5 10
RLGATE 1 9 20
RLSOURCE 3 7 4.7
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 6.0e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

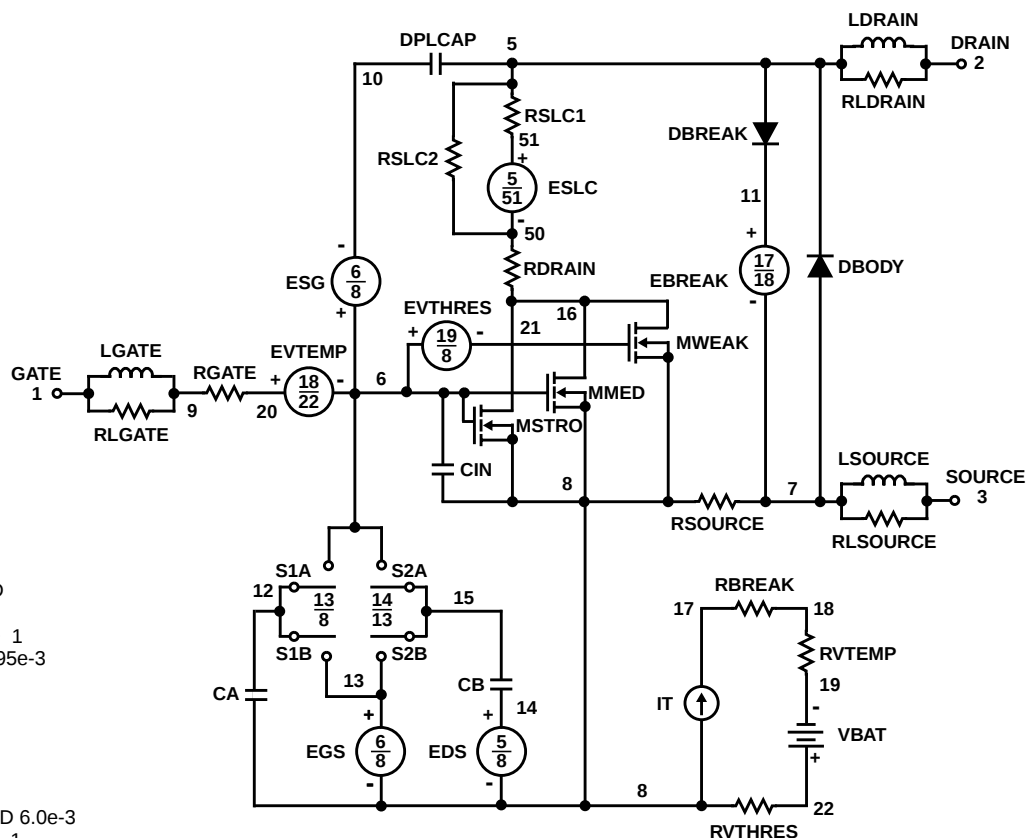
ESLC 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*230),4))}

.MODEL DBODYMOD D (IS = 3.5e-12 RS = 3.02e-3 TRS1 = 3e-3 TRS2 = 4e-6 CJO = 2.9e-9 TT = 4.35e-8 M = 0.5 N = 1.02 XTI = 5.5)
.MODEL DBREAKMOD D (RS = 8.5e-2 TRS1 = 8e-4 TRS2 = 1e-7)
.MODEL DPLCAPMOD D (CJO = 40e-10 IS = 1e-30 N = 10 M = 1.05)
.MODEL MMEDMOD NMOS (VTO = 3.1 KP = 1.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MSTROMOD NMOS (VTO = 3.73 KP = 86.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 2.7 KP = 0.01 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBREAKMOD RES (TC1 = 1.08e-3 TC2 = -2.5e-7)
.MODEL RDRAINMOD RES (TC1 = 2.05e-2 TC2 = 1.6e-5)
.MODEL RSLCMOD RES (TC1 = 6e-3 TC2 = -2.8e-6)
.MODEL RSOURCEMOD RES (TC1 = 5.5e-4 TC2 = 1.75e-5)
.MODEL RVTHRESMOD RES (TC = -3.65e-3 TC2 = -6e-6)
.MODEL RVTEMPMOD RES (TC1 = -2.3e-3 TC2 = -4e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -9.0 VOFF = -5.5)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5.5 VOFF = -9.0)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.0 VOFF = 2.1)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.1 VOFF = 0.0)

.ENDS

NOTE: For further discussion of the PSICE model, consult **A New PSICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



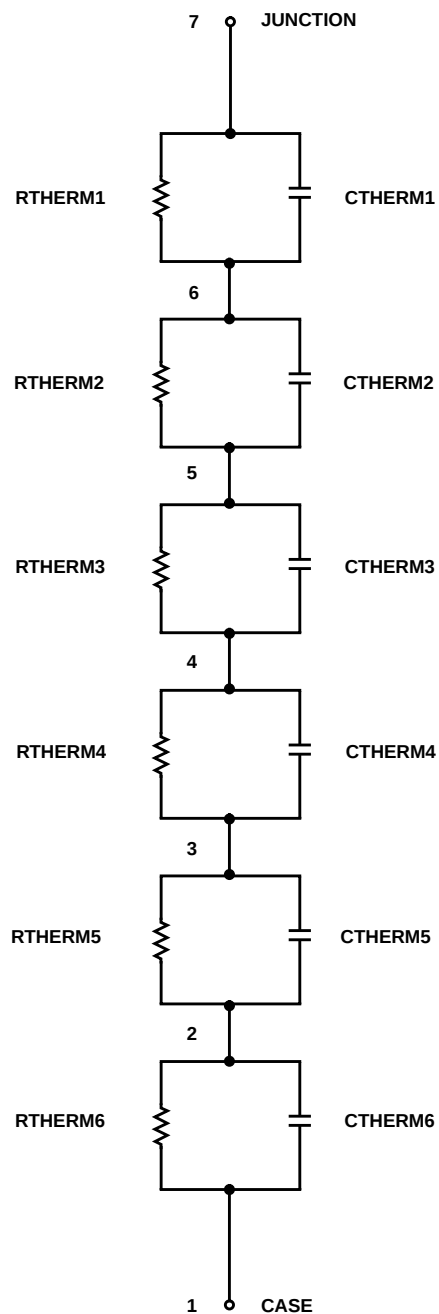
PSPICE Thermal Model

REV 27 June 97

HUF75339

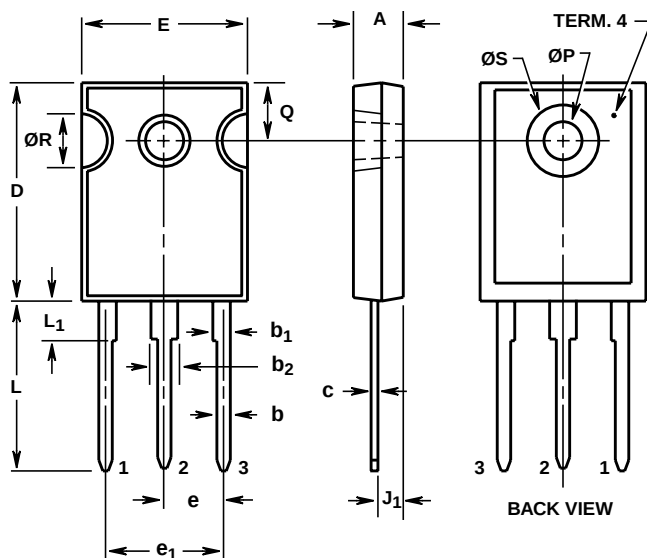
CTHERM1 7 6 6.50e-3
CTHERM2 6 5 1.00e-3
CTHERM3 5 4 2.24e-3
CTHERM4 4 3 8.60e-3
CTHERM5 3 2 5.80e-2
CTHERM6 2 1 2.5

RTHERM1 7 6 3.00e-7
RTHERM2 6 5 7.00e-6
RTHERM3 5 4 3.30e-2
RTHERM4 4 3 2.75e-1
RTHERM5 3 2 5.50e-1
RTHERM6 2 1 2.60e-1



TO-247

3 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE



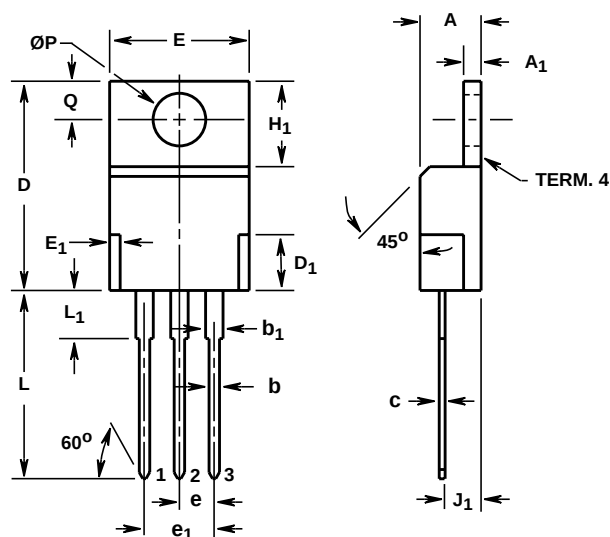
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b ₁	0.060	0.070	1.53	1.77	1, 2
b ₂	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.219 TYP		5.56 TYP		4
e ₁	0.438 BSC		11.12 BSC		4
J ₁	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L ₁	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L₁.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

TO-220AB

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



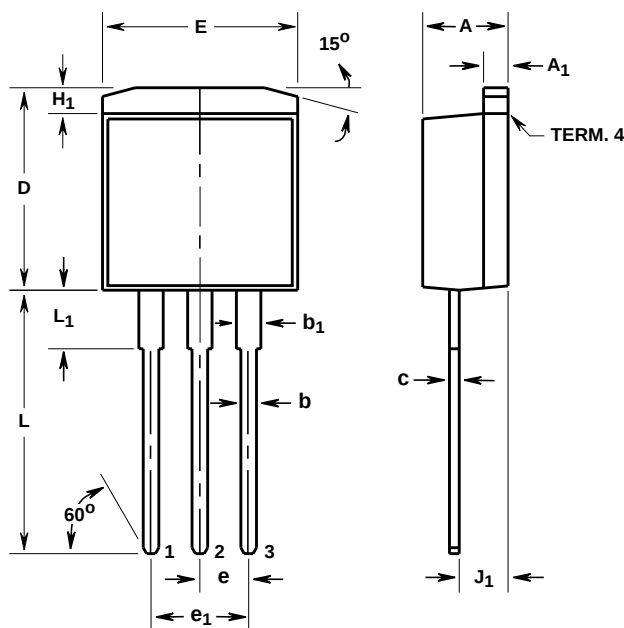
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b ₁	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D ₁	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E ₁	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e ₁	0.200 BSC		5.08 BSC		5
H ₁	0.235	0.255	5.97	6.47	-
J ₁	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L ₁	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L₁.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 7-97.

HUF75339G3, HUF75339P3, HUF75339S3, HUF75339S3S

TO-262AA 3 LEAD JEDEC TO-262AA PLASTIC PACKAGE

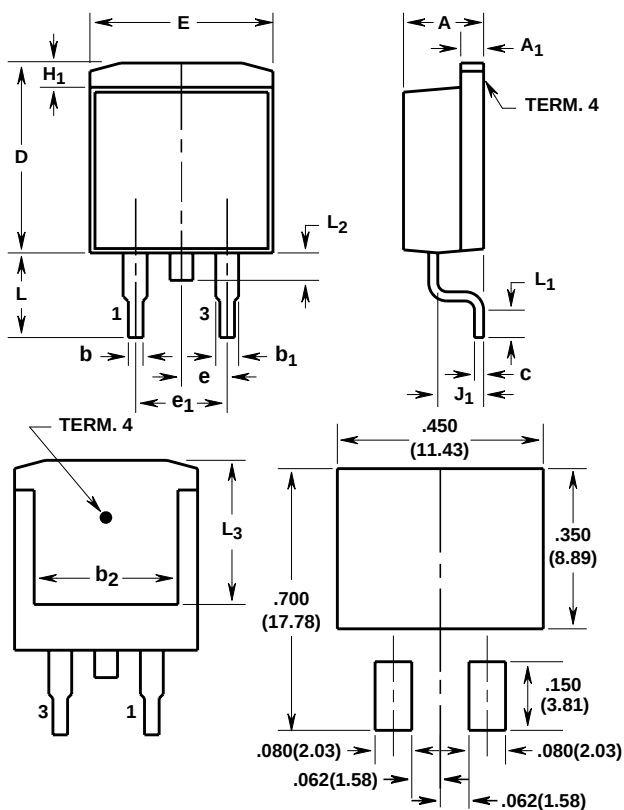


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	3, 4
b	0.030	0.034	0.77	0.86	3, 4
b ₁	0.045	0.055	1.15	1.39	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		5
e ₁	0.200 BSC		5.08 BSC		5
H ₁	0.045	0.055	1.15	1.39	-
J ₁	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L ₁	0.110	0.130	2.80	3.30	2

NOTES:

- These dimensions are within allowable dimensions of Rev. A of JEDEC TO-262AA outline dated 6-90.
- Solder finish uncontrolled in this area.
- Dimension (without solder).
- Add typically 0.002 inches (0.05mm) for solder plating.
- Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
- Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
- Controlling dimension: Inch.
- Revision 5 dated 7-97.

TO-263AB SURFACE MOUNT JEDEC TO-263AB PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	4, 5
b	0.030	0.034	0.77	0.86	4, 5
b ₁	0.045	0.055	1.15	1.39	4, 5
b ₂	0.310	-	7.88	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		7
e ₁	0.200 BSC		5.08 BSC		7
H ₁	0.045	0.055	1.15	1.39	-
J ₁	0.095	0.105	2.42	2.66	-
L	0.175	0.195	4.45	4.95	-
L ₁	0.090	0.110	2.29	2.79	4, 6
L ₂	0.050	0.070	1.27	1.77	3
L ₃	0.315	-	8.01	-	2

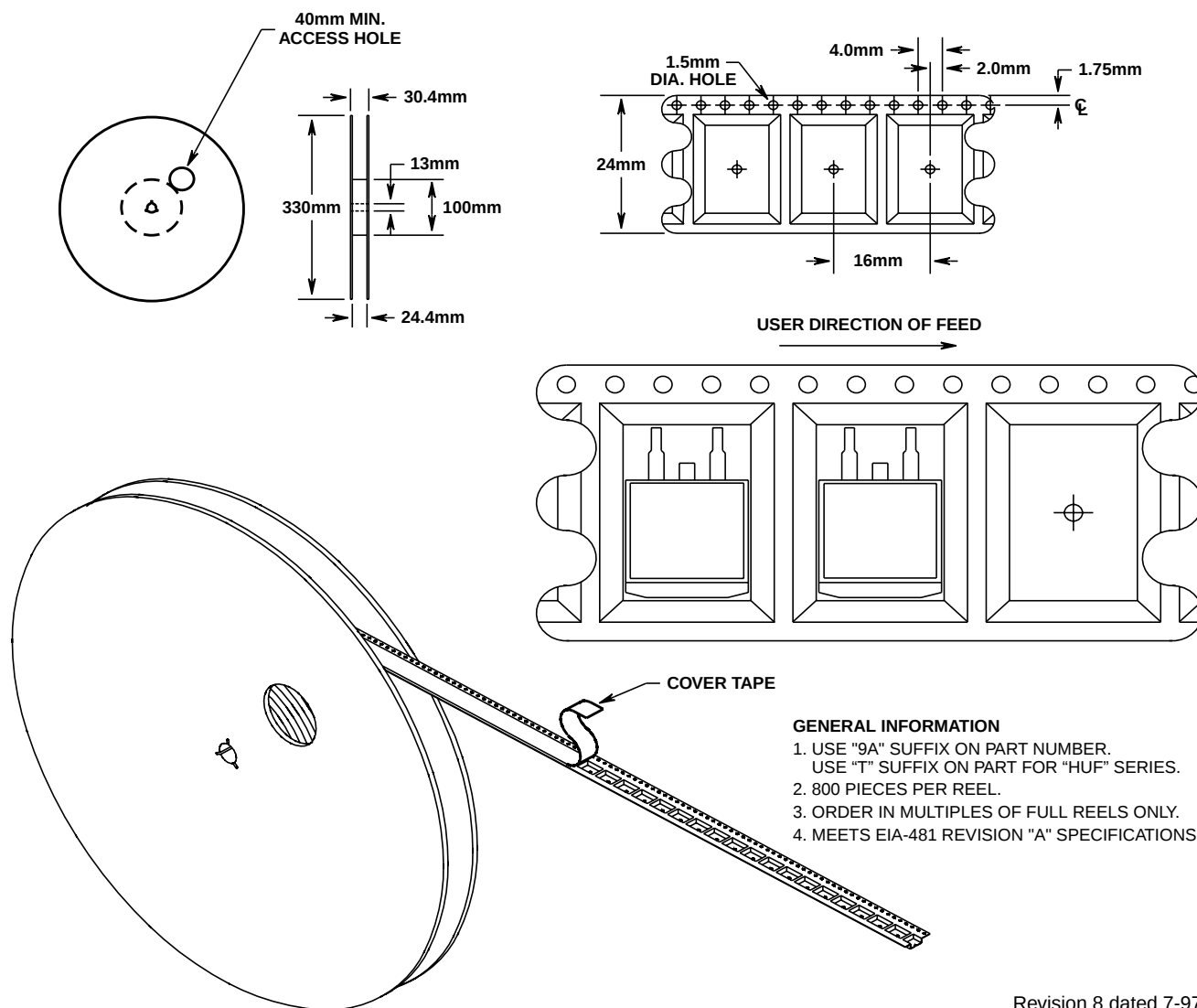
NOTES:

- These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
- L₃ and b₂ dimensions established a minimum mounting surface for terminal 4.
- Solder finish uncontrolled in this area.
- Dimension (without solder).
- Add typically 0.002 inches (0.05mm) for solder plating.
- L₁ is the terminal length for soldering.
- Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
- Controlling dimension: Inch.
- Revision 8 dated 7-97.

MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

TO-263AB

24mm TAPE AND REEL



GENERAL INFORMATION

1. USE "9A" SUFFIX ON PART NUMBER.
USE "T" SUFFIX ON PART FOR "HUF" SERIES.
2. 800 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revision 8 dated 7-97

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Harris Semiconductor products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Harris is believed to be accurate and reliable. However, no responsibility is assumed by Harris or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Harris or its subsidiaries.

Sales Office Headquarters

For general information regarding Harris Semiconductor and its products, call **1-800-4-HARRIS**

NORTH AMERICA

Harris Semiconductor
P. O. Box 883, Mail Stop 53-210
Melbourne, FL 32902
TEL: 1-800-442-7747
(407) 729-4984
FAX: (407) 729-5321

EUROPE

Harris Semiconductor
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Harris Semiconductor PTE Ltd.
No. 1 Tannery Road
Cencon 1, #09-01
Singapore 1334
TEL: (65) 748-4200
FAX: (65) 748-0400

