NCP4810

X2 Capacitors Discharger

The NCP4810 is a HV switch suitable for implementation of the X2 capacitor discharge function in applications with extremely low standby consumption requirements. It contains two high voltage MOSFETs with 700 V peak capabilities that can be connected directly to AC line voltage. Implementing this IC helps to design optimized EMI filter with appropriate X2 capacitor and reduced EMI coil volume and losses.

Features

- Build−in 700 V MOSFET
- Minimum Discharge Capability 0.85 mA
- Self Consumption Below 11 mW @ 700 V
- NoV_{CC} Necessary
- Compact SOIC−8 Package
- −40°C to + 125°C Operating Temperature Range
- This is a Pb−Free Device

Typical Applications

- Auxiliary Power Supply
- AC−DC Adapter
- Standby Power Supply
- Offline Battery Charger

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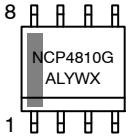
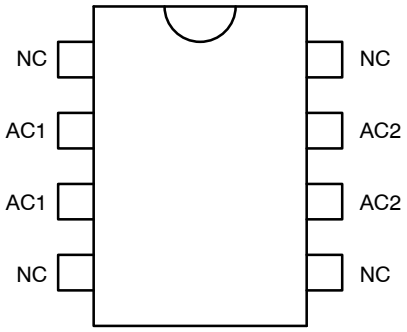
MARKING DIAGRAM

SOIC−8
D SUFFIX
CASE 751



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
X	= Assembly Lot
G	= Pb−Free Package

PINOUT



ORDERING INFORMATION

Device	Package	Shipping†
NCP4810DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

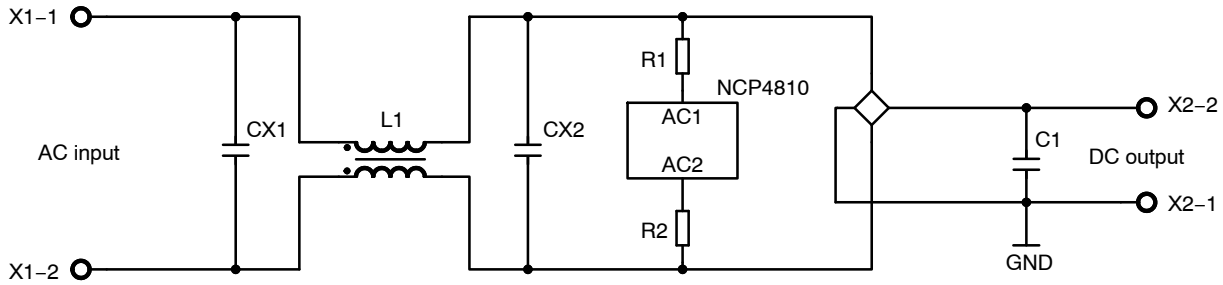


Figure 1. Typical Application Example of the X2 Discharger

PIN FUNCTION DESCRIPTION

Pin N°	Pin Name	Function	Pin Description
1	NC	Not connected	–
2	AC1	Alternate Current 1	Terminal for connections AC line
3	AC1	Alternate Current 1	Terminal for connections AC line
4	NC	Not connected	–
5	NC	Not connected	–
6	AC2	Alternate Current 2	Terminal for connections AC line
7	AC2	Alternate Current 2	Terminal for connections AC line
8	NC	Not connected	–

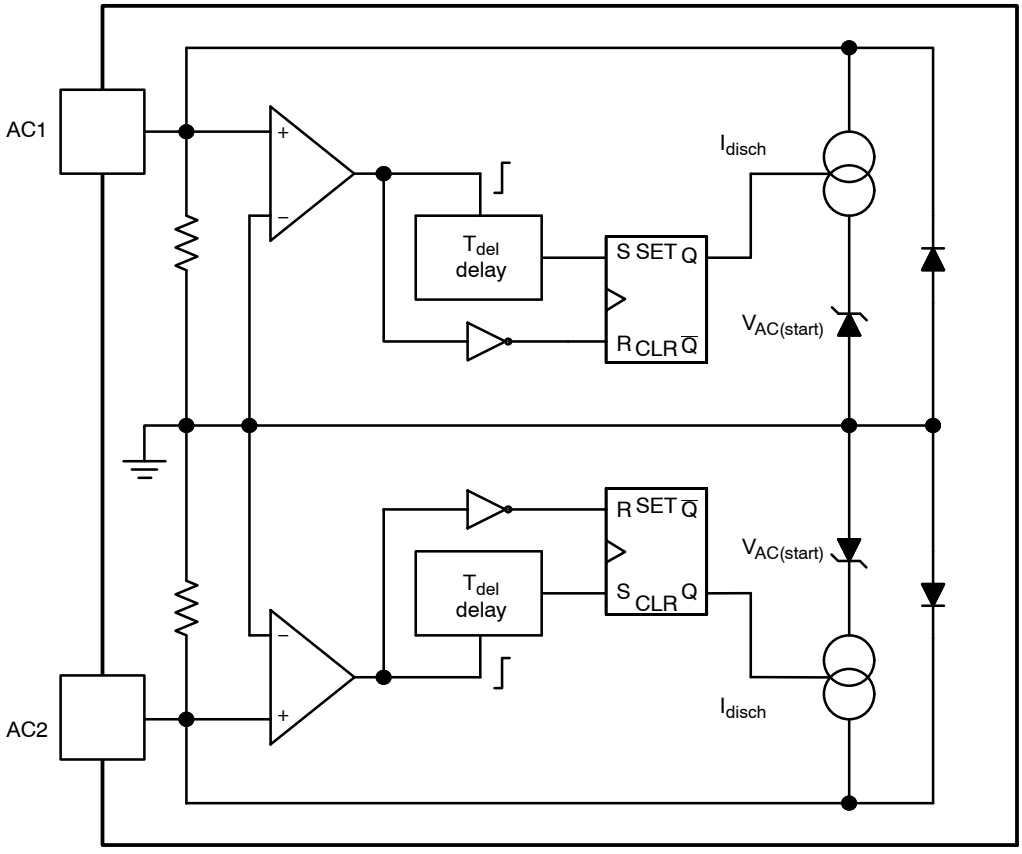


Figure 2. Simplified Circuit Architecture

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
AC1 pin Voltage related to AC2 pin	V_{HV}	−700 to 700	V
Thermal Resistance, Junction−to−Air (50 mm^2 x 35 μm Cu)	$R_{\theta J-A}$	162	°C/W
Junction Temperature	T_J	−40 to +150	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C
ESD Capability, HBM model per JEDEC standard JESD22, Method A114E	$V_{ESD-HBM}$	4	kV
ESD Capability, Machine Model per JEDEC standard JESD22, Method A115A	V_{ESD-MM}	600	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The latchup tests were not provided on this device because of two function pins only.

ELECTRICAL CHARACTERISTICS

(for typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, unless otherwise noted.)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
HV PIN						
Discharge current capability	V_{AC} = 400 Vdc	I_{disch}	0.85	–	–	mA
Minimum HV voltage	$I_{AC} = I_{disch} * 0.95$	$V_{AC(start)}$	–	–	40	Vdc
I_{HV} or $I_{HV(strat)}$ leakage current	V_{AC} = 700 Vdc	$I_{AC(leak)}$	–	7	15	μA
INTERNAL TIMER						
Internal timer	–	T_{del}	15	–	–	ms

TYPICAL CHARACTERISTICS

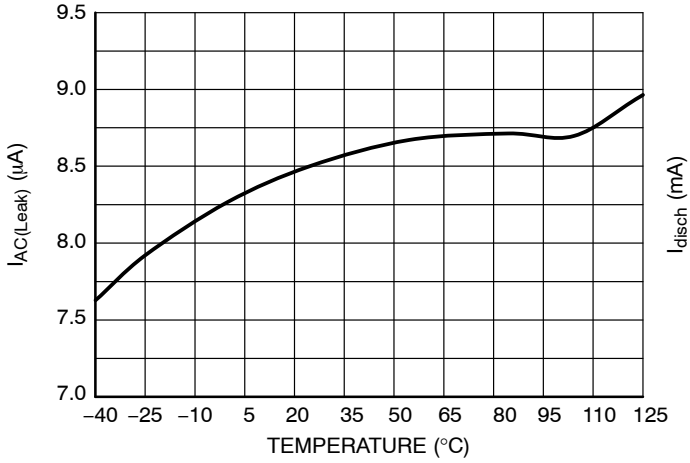


Figure 3. I_{HV} or $I_{HV(start)}$ Leakage Current, $I_{AC(Leak)}$

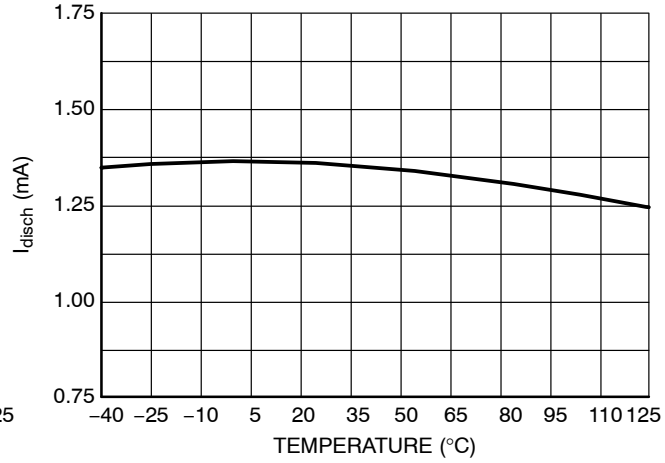


Figure 4. Discharge Current Capability, I_{disch}

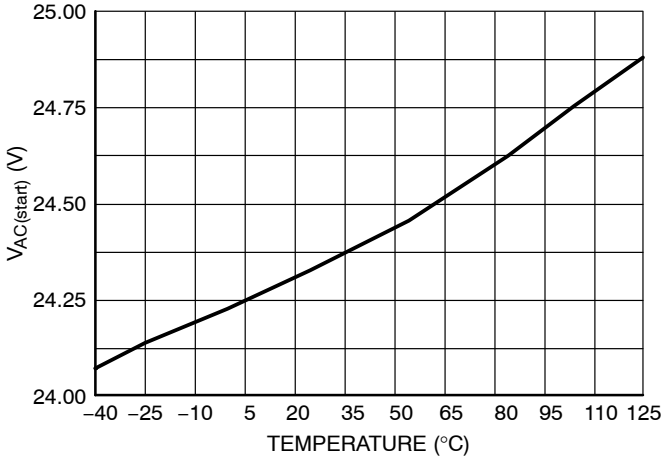


Figure 5. Minimum HV Voltage, $V_{AC(start)}$

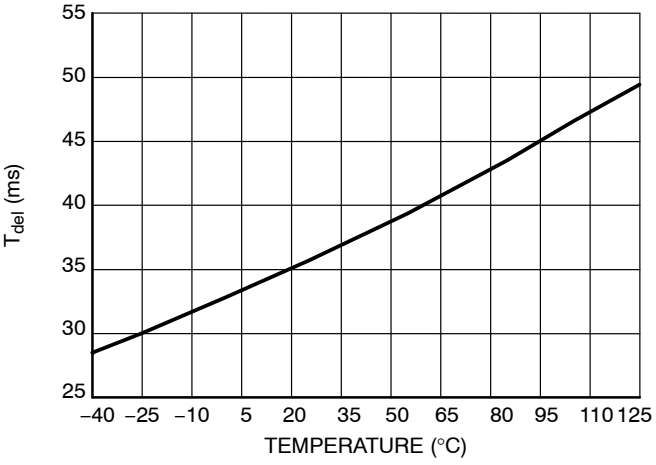


Figure 6. Internal Timer, T_{del}

Function Description:

The input sinusoidal voltage resets the relevant internal timer by transitioning across zero level at each its half wave. If no zero cross is detected, the internal timer expires and the appropriate current sink is turned on. This discharging path (the current sink and opposite diode) is established until the X2 capacitors are discharged (the input terminal voltage V_{AC} drops to zero) or the input AC voltage is restored by re−plugging the mains. The minimum discharge voltage is defined by $V_{AC(start)}$. Low $V_{AC(start)}$ allows to use serial resistors to distribute loss during discharging process. The recommended resistors values (R1 and R2) for any X2 capacitor are mentioned in Table 1. Every possibility of IC function refer to the input voltage behavior is described on Figure 7.

Table 1. RECOMMENDED SERIES RESISTORS VALUES

X2 Capacitance	Total Series Resistance (R1 + R2)
≤500 nF	1.5 MΩ
750 nF	1.02 MΩ
1 μF	780 kΩ
1.5 μF	480 kΩ
2 μF	360 kΩ

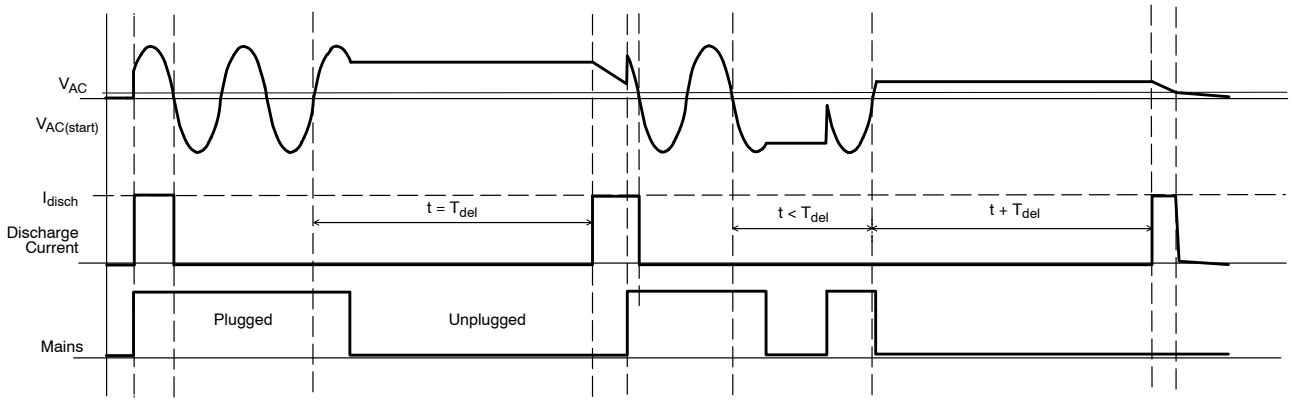
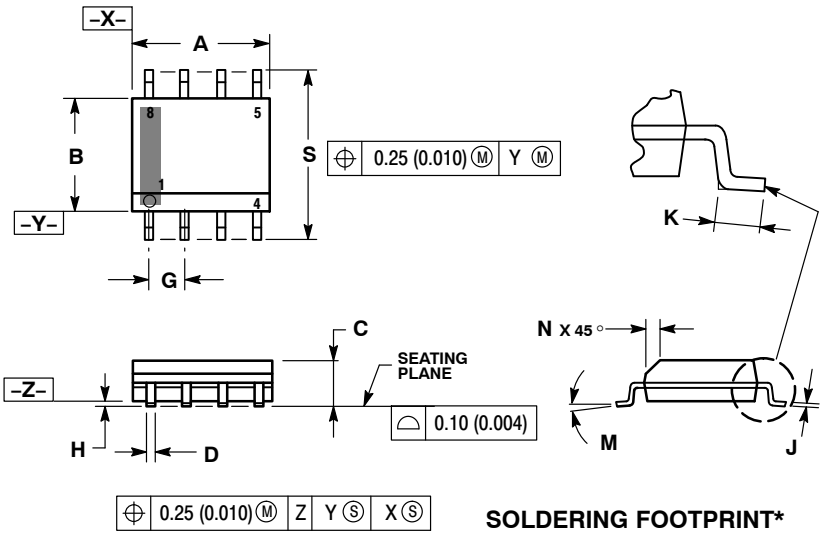


Figure 7. Function Description

PACKAGE DIMENSIONS

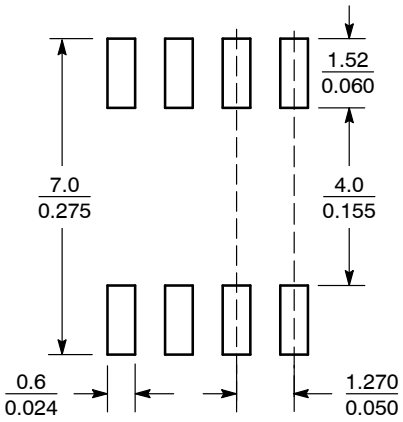
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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