Precision Low Noise CMOS Rail-to-Rail Input/Output Operational Amplifiers

AD8605/AD8606/AD8608

FEATURES
Low offset voltage: 65 µV maximum
Low input bias currents: 1 pA maximum
Low noise: 8 nV/√Hz
Wide bandwidth: 10 MHz
High open-loop gain: 120 dB
Unity gain stable
Single-supply operation: 2.7 V to 5.5 V
MicroCSP™

APPLICATIONS
Photodiode amplification
Battery-powered instrumentation
Multipole filters
Sensors
Barcode scanners
Audio

GENERAL DESCRIPTION

The AD8605, AD8606, and AD8608[1] are single, dual, and quad rail-to-rail input and output, single-supply amplifiers. They feature very low offset voltage, low input voltage and current noise, and wide signal bandwidth. They use Analog Devices' patented DigiTrim® trimming technique, which achieves superior precision without laser trimming.

The combination of low offsets, low noise, very low input bias currents, and high speed makes these amplifiers useful in a wide variety of applications. Filters, integrators, photodiode amplifiers, and high impedance sensors all benefit from the combination of performance features. Audio and other ac applications benefit from the wide bandwidth and low distortion. Applications for these amplifiers include optical control loops, portable and loop-powered instrumentation, and audio amplification for portable devices.

The AD8605, AD8606, and AD8608 are specified over the extended industrial temperature range (−40°C to +125°C). The AD8605 single is available in the 5-lead SOT-23 and 5-bump MicroCSP packages. The 5-bump MicroCSP offers the smallest available footprint for any surface-mount operational amplifier. The AD8606 dual is available in an 8-lead MSOP package and a narrow SOIC surface-mount package. The AD8608 quad is available in a 14-lead TSSOP and a narrow 14-lead SOIC package. MicroCSP, SOT, MSOP, and TSSOP versions are available in tape and reel only.

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[1] Protected by U.S. Patent No. 5,969,657; other patents pending.
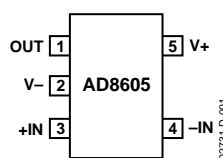
FUNCTIONAL BLOCK DIAGRAMS
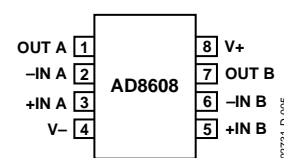

Figure 1. 5-Lead SOT-23 (RT Suffix)
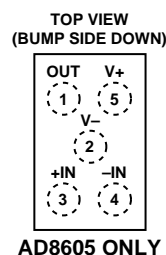

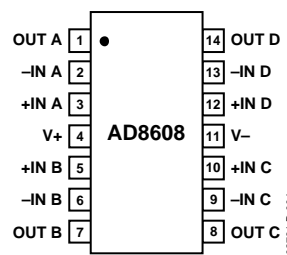Figure 2. 8-Lead SOIC (R Suffix)

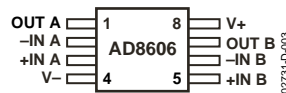Figure 3. 5-Bump MicroCSP (CB Suffix)

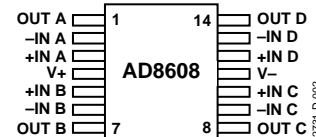Figure 4. 14-Lead SOIC (R Suffix)

Figure 5. 8-Lead MSOP (RM Suffix)

Figure 6. 14-Lead TSSOP (RU Suffix)

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AD8605/AD8606/AD8608

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REVISION HISTORY

5 V ELECTRICAL SPECIFICATIONS

Table 1. @ V_S = 5 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
AD8605/AD8606		V_S = 3.5 V, V_{CM} = 3 V		20	65	µV
AD8608		V_S = 3.5 V, V_{CM} = 2.7 V		20	75	µV
		V_S = 5 V, V_{CM} = 0 V to 5 V		80	300	µV
		−40°C < T_A < +125°C			750	µV
Input Bias Current	I_B			0.2	1	pA
AD8605/AD8606		−40°C < T_A < +85°C			50	pA
AD8605/AD8606		−40°C < T_A < +125°C			250	pA
AD8608		−40°C < T_A < +85°C			100	pA
AD8608		−40°C < T_A < +125°C			300	pA
Input Offset Current	I_{OS}			0.1	0.5	pA
		−40°C < T_A < +85°C			20	pA
		−40°C < T_A < +125°C			75	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	85	100		dB
		−40°C < T_A < +125°C	75	90		dB
Large Signal Voltage Gain	A_{VO}	V_O = 0.5 V to 4.5 V	300	1,000		V/mV
		R_L = 2 kΩ, V_{CM} = 0 V				
Offset Voltage Drift						
AD8605/AD8606	$\Delta V_{OS}/\Delta T$			1	4.5	µV/°C
AD8608	$\Delta V_{OS}/\Delta T$			1.5	6.0	µV/°C
INPUT CAPACITANCE						
Common-Mode Input Capacitance				8.8		pF
Differential Input Capacitance				2.59		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	4.96	4.98		V
		I_L = 10 mA	4.7	4.79		V
		−40°C < T_A < +125°C	4.6			V
Output Voltage Low	V_{OL}	I_L = 1 mA		20	40	mV
		I_L = 10 mA		170	210	mV
		−40°C < T_A < +125°C			290	mV
Output Current	I_{OUT}			±80		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		10		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR					
AD8605/AD8606		V_S = 2.7 V to 5.5 V	80	95		dB
AD8608		V_S = 2.7 V to 5.5 V	77	92		dB
		−40°C < T_A < +125°C	70	90		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		1	1.2	mA
		−40°C < T_A < +125°C			1.4	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		5		V/µs
Settling Time	t_S	To 0.01%, 0 V to 2 V step		< 1		µs
Full Power Bandwidth	BW_P	< 1% distortion		360		kHz
Gain Bandwidth Product	GBP				10	MHz
Phase Margin	φ_O			65		Degrees

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		2.3	3.5	µV p-p
Voltage Noise Density	e_n	f = 1 kHz		8	12	nV/$\sqrt{Hz}$
Voltage Noise Density	e_n	f = 10 kHz		6.5		nV/$\sqrt{Hz}$
Current Noise Density	i_n	f = 1 kHz		0.01		pA/$\sqrt{Hz}$

2.7 V ELECTRICAL SPECIFICATIONS

Table 2. @ V_S = 2.7 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
AD8605/AD8606		V_S = 3.5 V, V_{CM} = 3 V		20	65	µV
AD8608		V_S = 3.5 V, V_{CM} = 2.7 V		20	75	µV
		V_S = 2.7 V, V_{CM} = 0 V to 2.7 V		80	300	µV
		−40°C < T_A < +125°C			750	µV
Input Bias Current	I_B			0.2	1	pA
AD8605/AD8606		−40°C < T_A < +85°C			50	pA
AD8605/AD8606		−40°C < T_A < +125°C			250	pA
AD8608		−40°C < T_A < +85°C			100	pA
AD8608		−40°C < T_A < +125°C			300	pA
Input Offset Current	I_{OS}			0.1	0.5	pA
		−40°C < T_A < +85°C			20	pA
		−40°C < T_A < +125°C			75	pA
Input Voltage Range			0		2.7	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.7 V	80	95		dB
		−40°C < T_A < +125°C	70	85		dB
Large Signal Voltage Gain	A_{VO}	RL = 2 kΩ, V_O= 0.5 V to 2.2 V	110	350		V/mV
Offset Voltage Drift						
AD8605/AD8606	$\Delta V_{OS}/\Delta T$			1	4.5	µV/°C
AD8608	$\Delta V_{OS}/\Delta T$			1.5	6.0	µV/°C
INPUT CAPACITANCE						
Common-Mode Input Capacitance				8.8		pF
Differential Input Capacitance				2.59		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	2.6	2.66		V
		−40°C < T_A < +125°C	2.6			V
Output Voltage Low	V_{OL}	I_L = 1 mA		25	40	mV
		−40°C < T_A < +125°C			50	mV
Output Current	I_{OUT}			±30		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		12		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR					
AD8605/AD8606		V_S = 2.7 V to 5.5 V	80	95		dB
AD8608		V_S = 2.7 V to 5.5 V	77	92		dB
		−40°C < T_A < +125°C	70	90		dB
Supply Current/Amplifier	ISY	V_O = 0 V		1.15	1.4	mA
		−40°C < T_A < +125°C			1.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		5		V/µs
Settling Time	t_S	To 0.01%, 0 V to 1 V step		< 0.5		µs
Gain Bandwidth Product	GBP			9		MHz
Phase Margin	φ_O			50		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		2.3	3.5	µV p-p
Voltage Noise Density	e_n	f = 1 kHz		8	12	nV/$\sqrt{Hz}$
Voltage Noise Density	e_n	f = 10 kHz		6.5		nV/$\sqrt{Hz}$
Current Noise Density	i_n	f = 1 kHz		0.01		pA/$\sqrt{Hz}$

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to V_S
Differential Input Voltage	6 V
Output Short-Circuit Duration to GND	Observe Derating Curves
Storage Temperature Range	
All Packages	−65°C to +150°C
Operating Temperature Range	
AD8605/AD8606/AD8608	−40°C to +125°C
Junction Temperature Range	
All Packages	−65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Table 4. Package Type

Package Type	θ_{JA}[1]	θ_{JC}	Unit
5-Bump MicroCSP (CB)	220	220	°C/W
5-Lead SOT-23 (RT)	230	92	°C/W
8-Lead MSOP (RM)	210	45	°C/W
8-Lead SOIC (R)	158	43	°C/W
14-Lead SOIC (R)	120	36	°C/W
14-Lead TSSOP (RU)	180	35	°C/W

[1] θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for device in socket for PDIP packages; θ_{JA} is specified for device soldered onto a circuit board for surface-mount packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

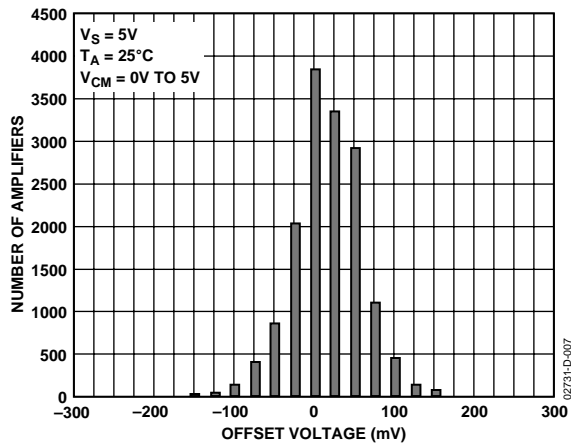# TYPICAL PERFORMANCE CHARACTERISTICS

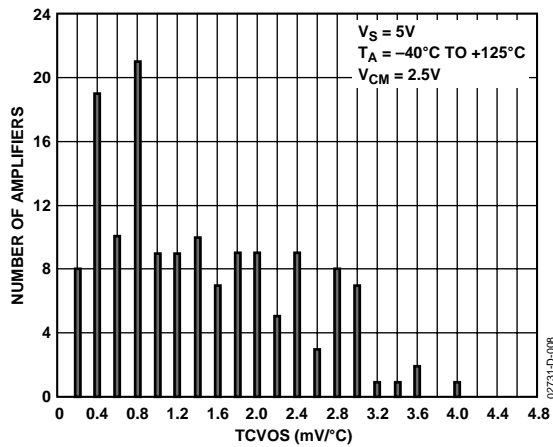Figure 7. Input Offset Voltage Distribution

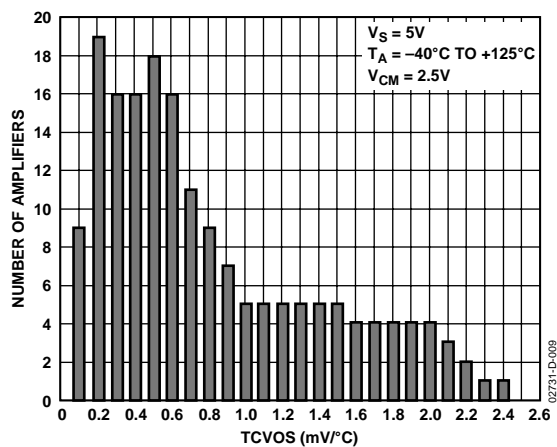Figure 8. AD8608 Input Offset Voltage Drift Distribution

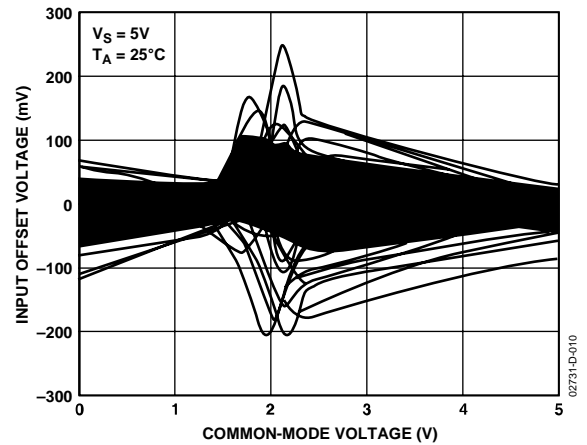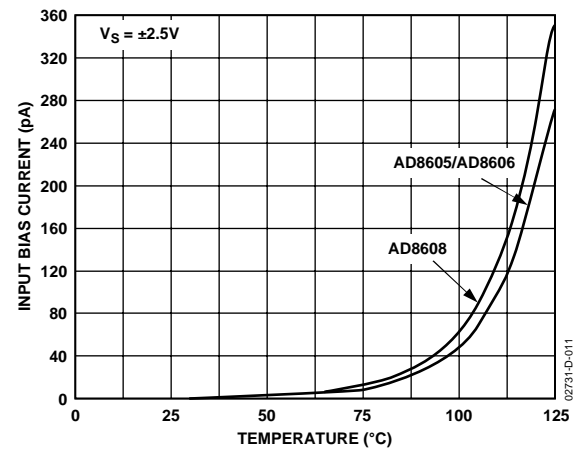Figure 9. AD8605/AD8606 Input Offset Voltage Drift Distribution

Figure 10. Input Offset Voltage vs. Common-Mode Voltage
(200 Units, 5 Wafer Lots, Including Process Skews)
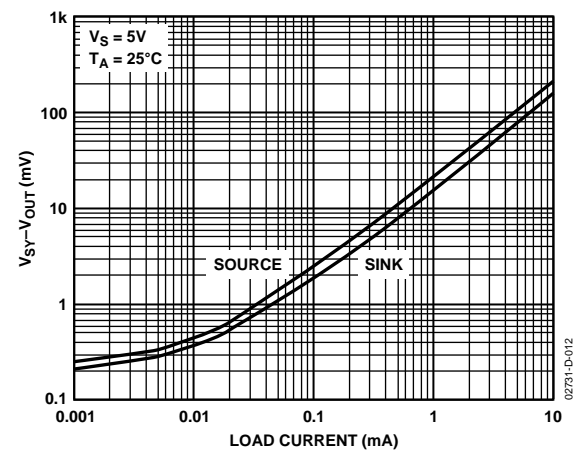

Figure 11. Input Bias Current vs. Temperature

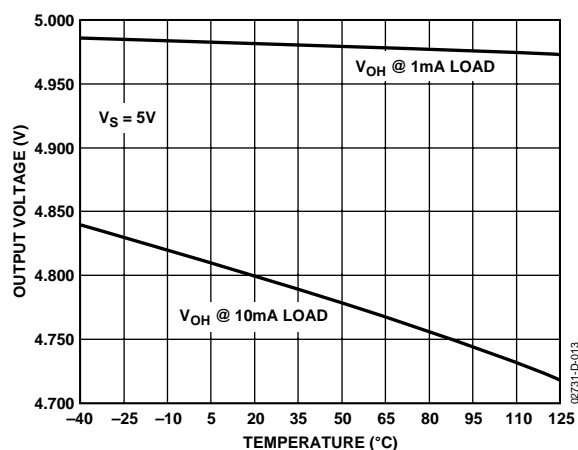Figure 12. Output Voltage to Supply Rail vs. Load Current

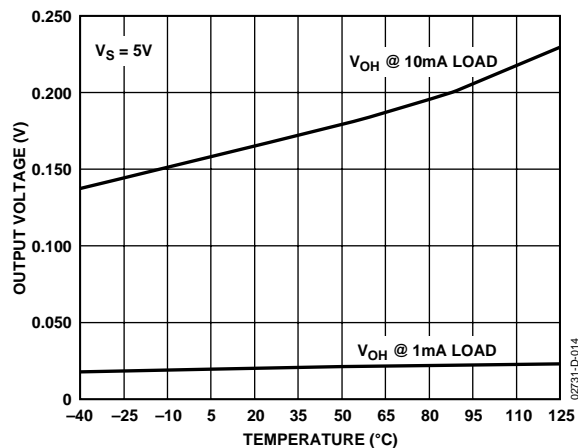Figure 13. Output Voltage Swing vs. Temperature

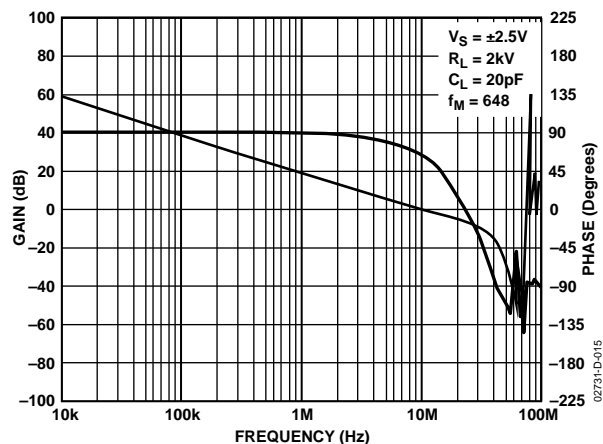Figure 14. Output Voltage Swing vs. Temperature

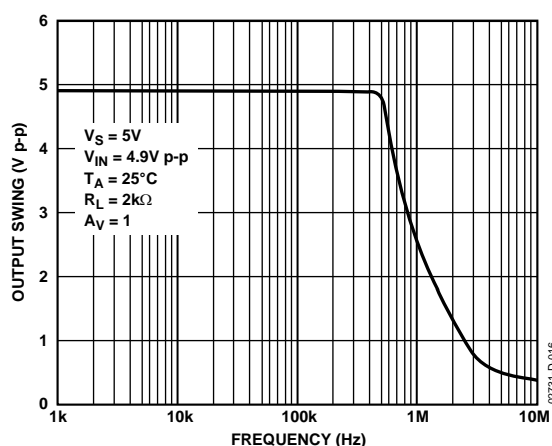Figure 15. Open-Loop Gain and Phase vs. Frequency

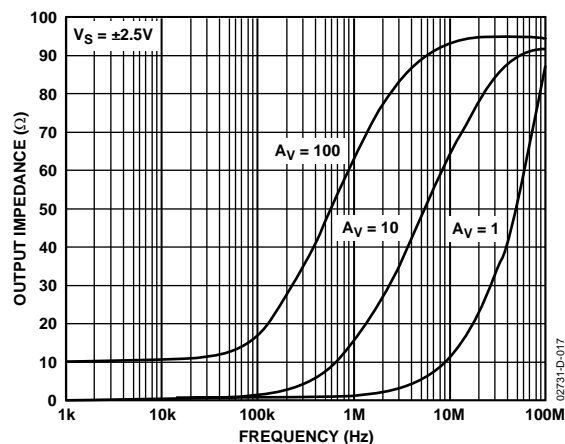Figure 16. Closed-Loop Output Voltage Swing

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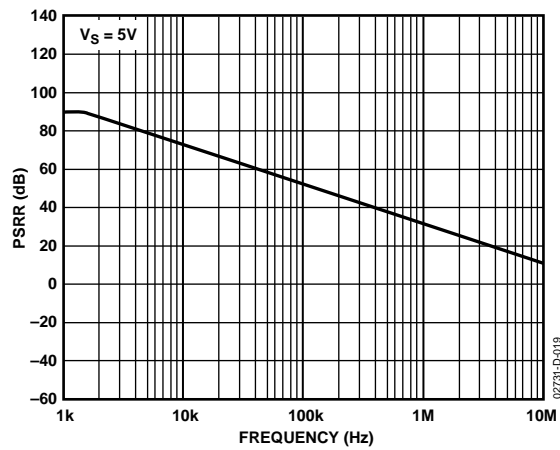
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Figure 20. Small Signal Overshoot vs. Load Capacitance

Figure 21. Supply Current vs. Temperature

Figure 22. Supply Current vs. Supply Voltage

Figure 23. 0.1 Hz to 10 Hz Input Voltage Noise
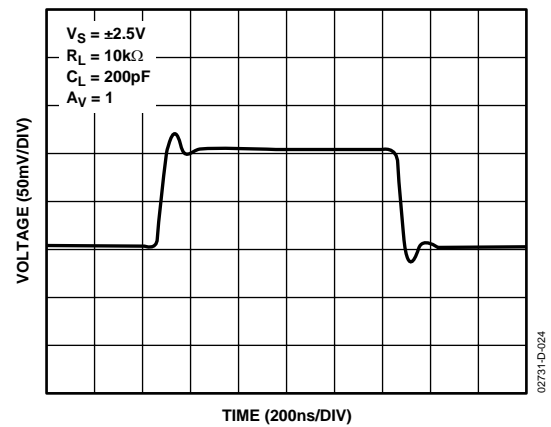
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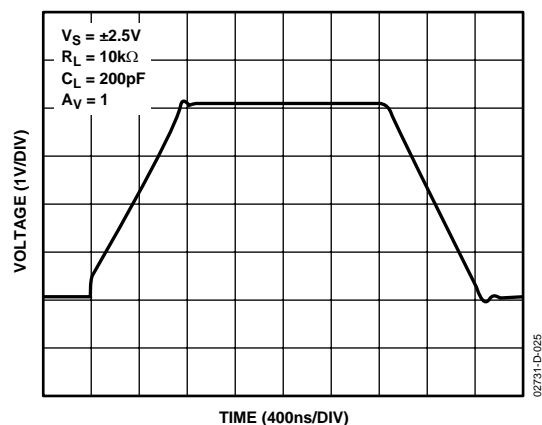
Figure 25. Large Signal Transient Response
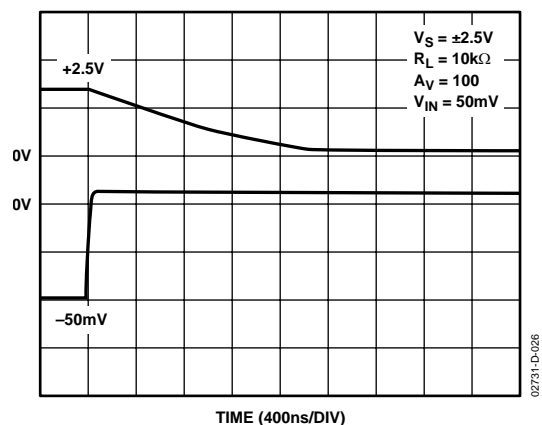
Figure 26. Negative Overload Recovery
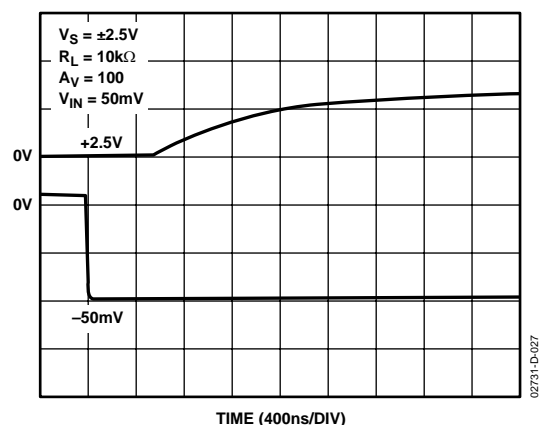
Figure 27. Positive Overload Recovery
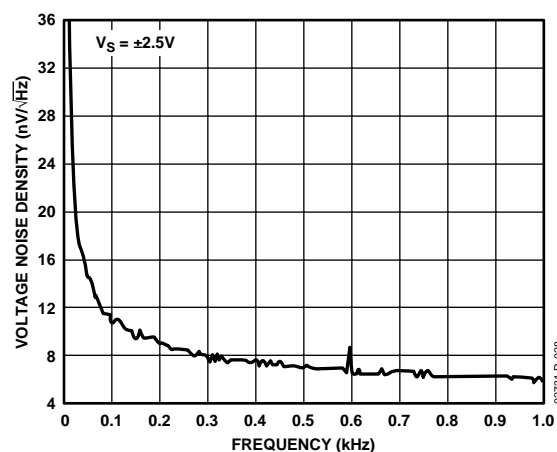
Figure 28. Voltage Noise Density
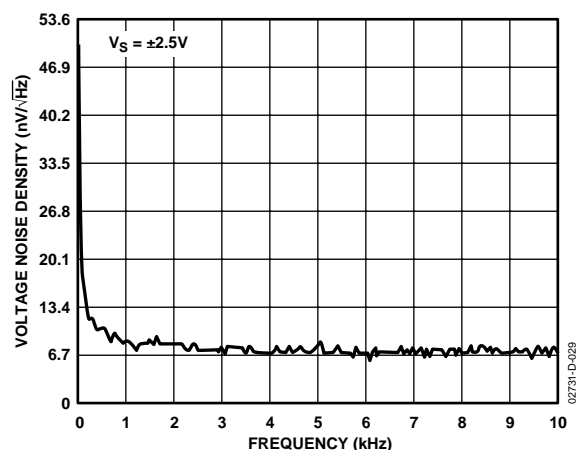
Figure 29. Voltage Noise Density
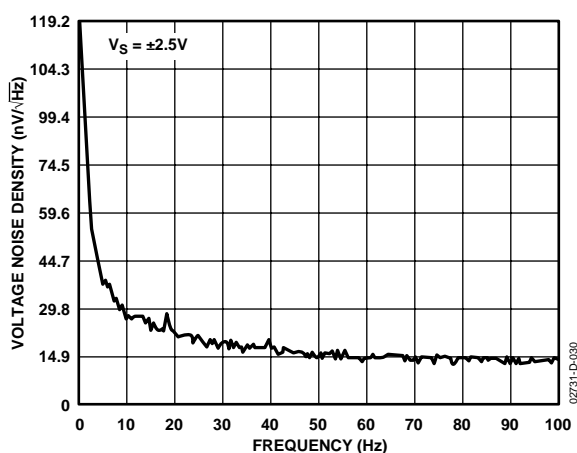
Figure 30. Voltage Noise Density
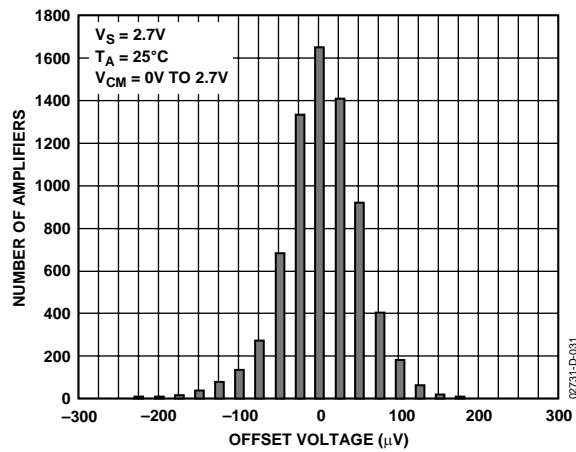
Figure 31. Input Offset Voltage Distribution
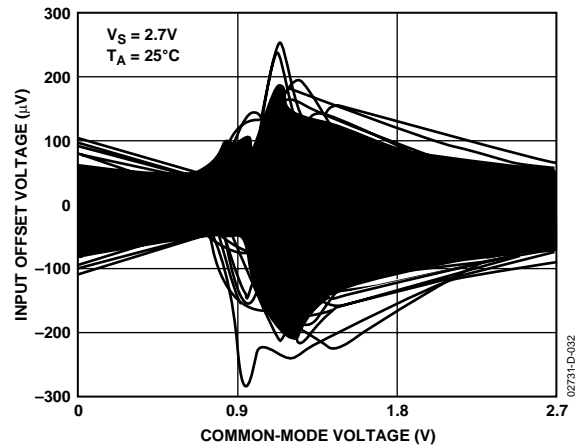
Figure 32. Input Offset Voltage vs. Common-Mode Voltage
(200 Units, 5 Wafer Lots, Including Process Skews)
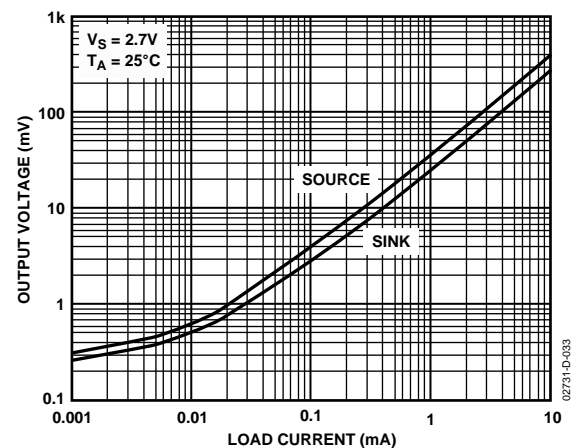
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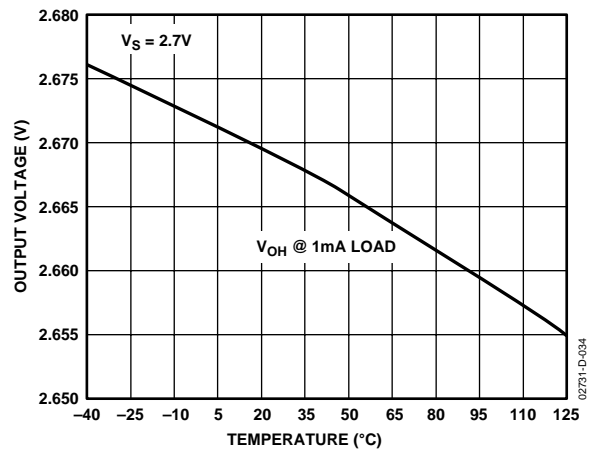
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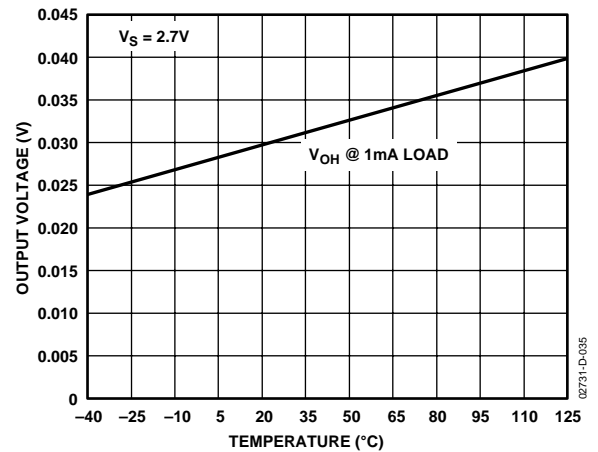
Figure 35. Output Voltage Swing vs. Temperature
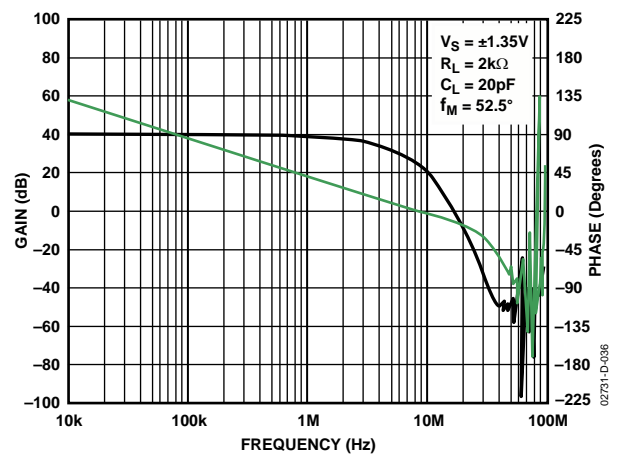
Figure 36. Open-Loop Gain and Phase vs. Frequency
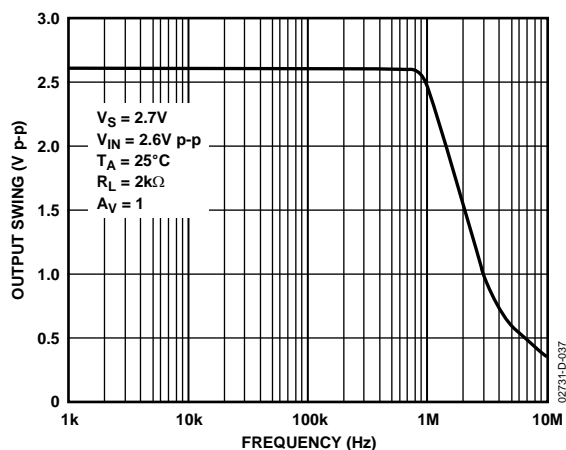
Figure 37. Closed-Loop Output Voltage Swing vs. Frequency
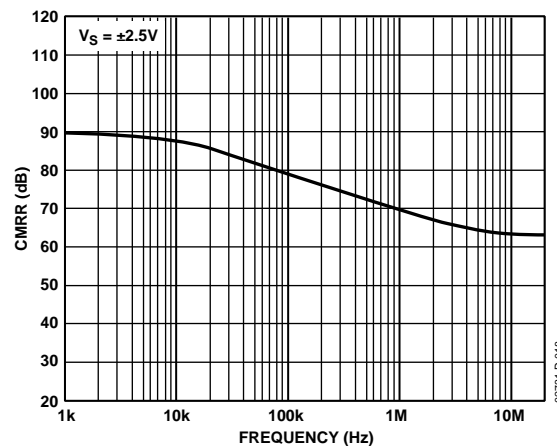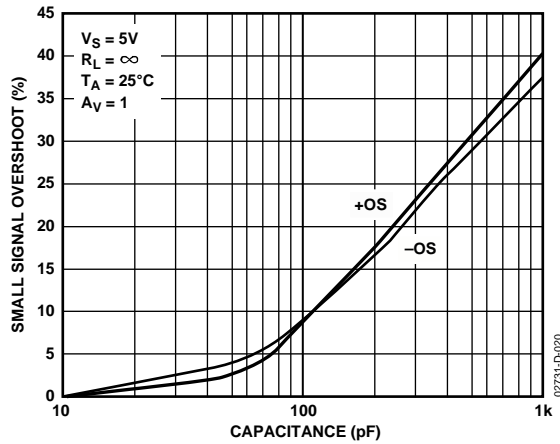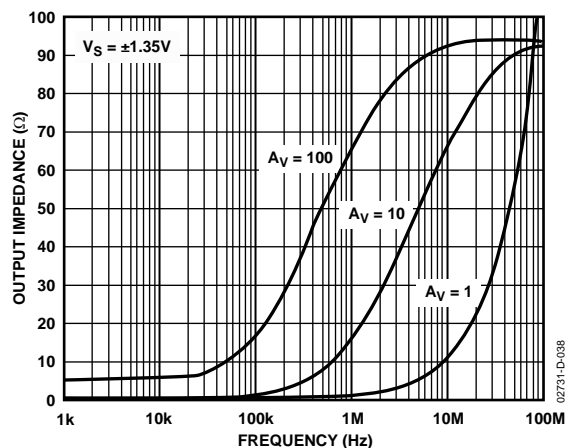
Figure 38. Output Impedance vs. Frequency
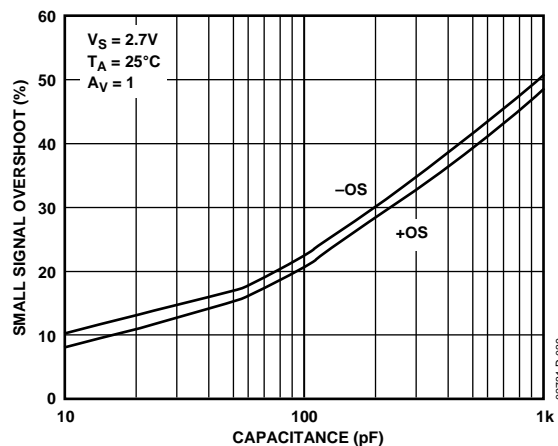
Figure 39. Small Signal Overshoot vs. Load Capacitance
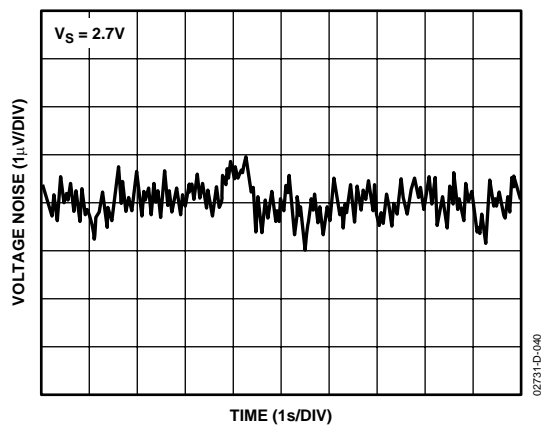
Figure 40. 0.1 Hz to 10 Hz Input Voltage Noise
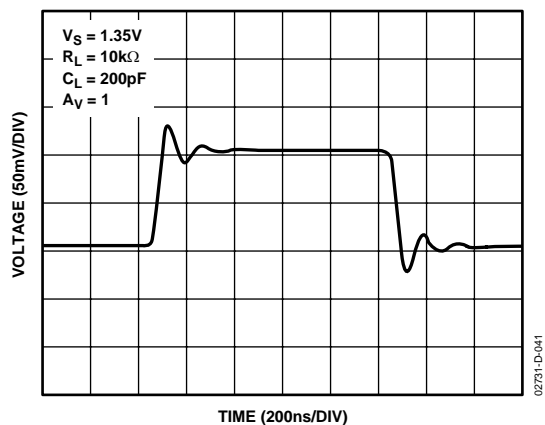
Figure 41. Small Signal Transient Response
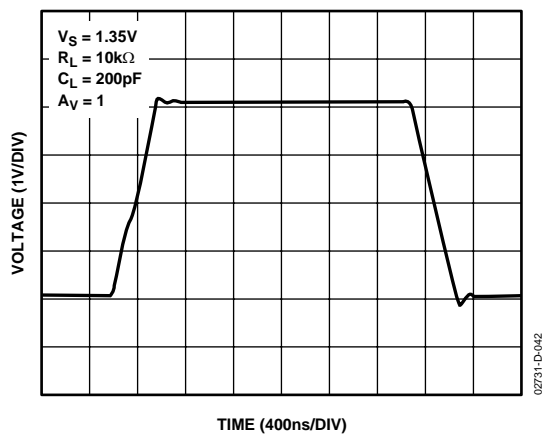
Figure 42. Large Signal Transient Response

APPLICATION INFORMATION

OUTPUT PHASE REVERSAL

Phase reversal is defined as a change in polarity at the output of the amplifier when a voltage that exceeds the maximum input common-mode voltage drives the input.

Phase reversal can cause permanent damage to the amplifier; it may also cause system lockups in feedback loops. The AD8605 does not exhibit phase reversal even for inputs exceeding the supply voltage by more than 2 V.
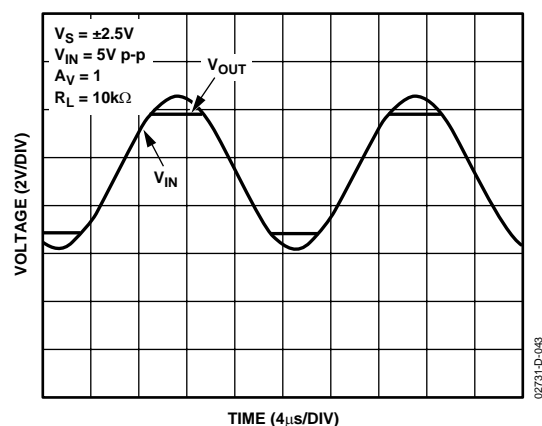
Figure 43. No Phase Reversal

MAXIMUM POWER DISSIPATION

Power dissipated in an IC causes the die temperature to increase. This can affect the behavior of the IC and the application circuit performance.

The absolute maximum junction temperature of the AD8605/ AD8606/AD8608 is 150°C. Exceeding this temperature could cause damage or destruction of the device. The maximum power dissipation of the amplifier is calculated according to the following formula:

$$P_{DISS} = \frac{T_J - T_A}{\theta_{JA}}$$

where:

T_J = junction temperature
T_A = ambient temperature
θ_{JA} = junction to-ambient-thermal resistance

Figure 44 compares the maximum power dissipation with temperature for the various AD8605 family packages.
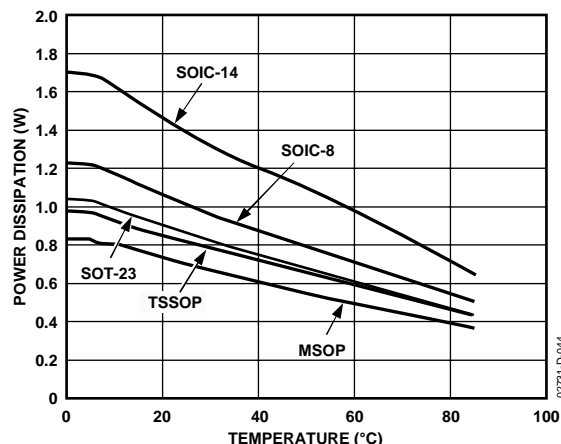
Figure 44. Maximum Power Dissipation vs. Temperature

INPUT OVERVOLTAGE PROTECTION

The AD8605 has internal protective circuitry. However, if the voltage applied at either input exceeds the supplies by more than 2.5 V, external resistors should be placed in series with the inputs. The resistor values can be determined by the formula

$$\frac{\left(V_{IN} - V_S\right)}{\left(R_S + 200\Omega\right)} \le 5mA$$

The remarkable low input offset current of the AD8605 (<1 pA) allows the use of larger value resistors. With a 10 kΩ resistor at the input, the output voltage has less than 10 nV of error voltage. A 10 kΩ resistor has less than 13 nV/$\sqrt{Hz}$ of thermal noise at room temperature.

THD + NOISE

Total harmonic distortion is the ratio of the input signal in V rms to the total harmonics in V rms throughout the spectrum. Harmonic distortion adds errors to precision measurements and adds unpleasant sonic artifacts to audio systems.

The AD8605 has a low total harmonic distortion. Figure 45 shows that the AD8605 has less than 0.005% or −86 dB of THD + N over the entire audio frequency range. The AD8605 is configured in positive unity gain, which is the worst case, and with a load of 10 kΩ.
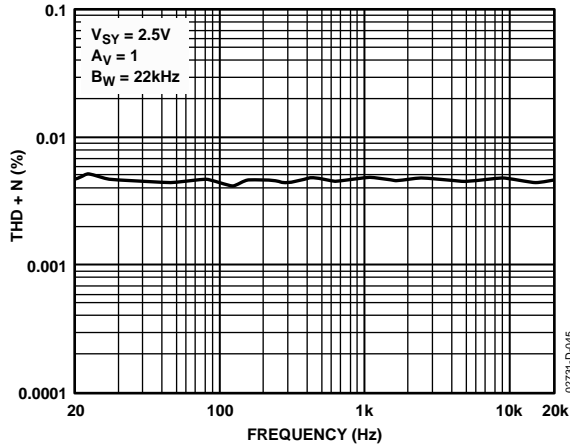
Figure 45. THD + N

TOTAL NOISE INCLUDING SOURCE RESISTORS

The low input current noise and input bias current of the AD8605 make it the ideal amplifier for circuits with substantial input source resistance such as photodiodes. Input offset voltage increases by less than 0.5 nV per 1 kΩ of source resistance at room temperature and increases to 10 nV at 85°C. The total noise density of the circuit is

$$e_{n,TOTAL} = \sqrt{e_n^2 + (i_n R_S)^2 + 4kTR_S}$$

where:

e_n is the input voltage noise density of the AD8605

i_n is the input current noise density of the AD8605

R_S is the source resistance at the noninverting terminal

k is Boltzmann's constant (1.38×10^{-23} J/K)

T is the ambient temperature in Kelvin (T = 273 + °C)

For example, with R_S = 10 kΩ, the total voltage noise density is roughly 15 nV/√Hz.

For R_S < 3.9 $k\Omega$, e_n dominates and $e_{n,TOTAL} \approx e_n$.

The current noise of the AD8605 is so low that its total density does not become a significant term unless R_S is greater than 6 MΩ. The total equivalent rms noise over a specific bandwidth is expressed as

$$E_n = (e_{n,TOTAL})\sqrt{BW}$$

where *BW* is the bandwidth in hertz.

Note that the analysis above is valid for frequencies greater than 100 Hz and assumes relatively flat noise, above 10 kHz. For lower frequencies, flicker noise (1/f) must be considered.

CHANNEL SEPARATION

Channel separation, or inverse crosstalk, is a measure of the signal feed from one amplifier (channel) to an other on the same IC.

The AD8606 has a channel separation of greater than −160 dB up to frequencies of 1 MHz, allowing the two amplifiers to amplify ac signals independently in most applications.
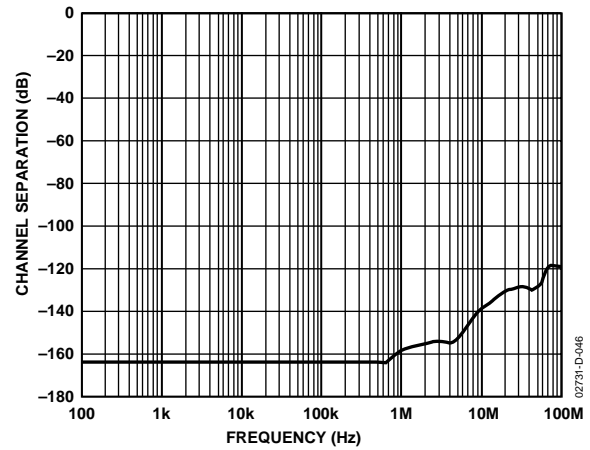
Figure 46. Channel Separation vs. Frequency

CAPACITIVE LOAD DRIVE

The AD8605 can drive large capacitive loads without oscillation. Figure 47 shows the output of the AD8606 in response to a 200 mV input signal. In this case, the amplifier was configured in positive unity gain, worst case for stability, while driving a 1,000 pF load at its output. Driving larger capacitive loads in unity gain may require the use of additional circuitry.
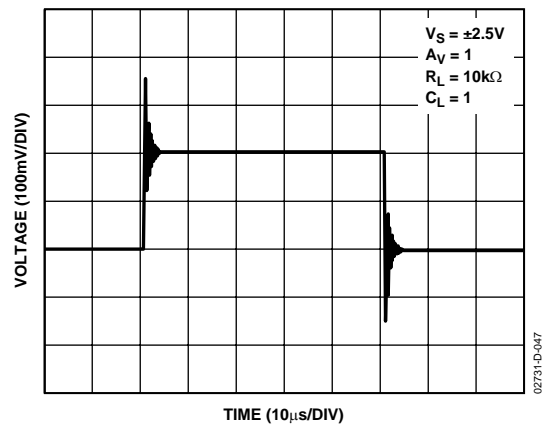
Figure 47. Capacitive Load Drive without Snubber

A snubber network, shown in Figure 48, helps reduce the signal overshoot to a minimum and maintain stability. Although this circuit does not recover the loss of bandwidth induced by large capacitive loads, it greatly reduces the overshoot and ringing. This method does not reduce the maximum output swing of the amplifier.

Figure 49 shows a scope photograph of the output at the snubber circuit. The overshoot is reduced from over 70% to less than 5%, and the ringing is eliminated by the snubber. Optimum values for R_S and C_S are determined experimentally.
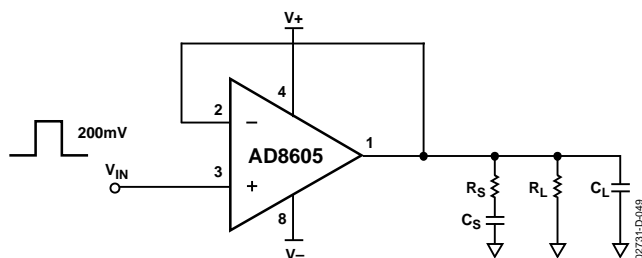
Figure 48. Snubber Network Configuration
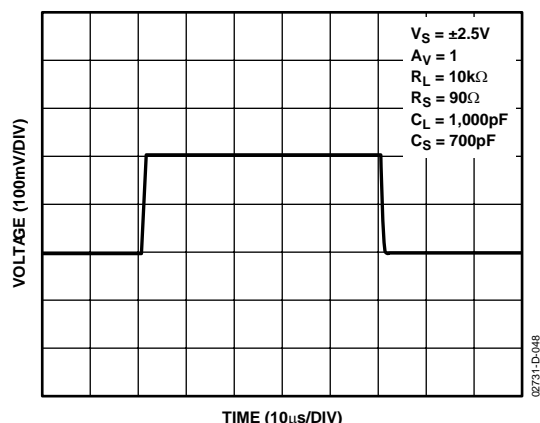
Figure 49. Capacitive Load Drive with Snubber

Table 5 summarizes a few optimum values for capacitive loads.

Table 5.

C_L (pF)	R_S (Ω)	C_S (pF)
500	100	1,000
1,000	70	1,000
2,000	60	800

An alternate technique is to insert a series resistor inside the feedback loop at the output of the amplifier. Typically, the value of this resistor is approximately 100 Ω. This method also reduces overshoot and ringing but causes a reduction in the maximum output swing.

LIGHT SENSITIVITY

The AD8605ACB (MicroCSP package option) is essentially a silicon die with additional post fabrication dielectric and intermetallic processing designed to contact solder bumps on the active side of the chip. With this package type, the die is exposed to ambient light and is subject to photoelectric effects. Light sensitivity analysis of the AD8605ACB mounted on standard PCB material reveals that only the input bias current (I_B) parameter is impacted when the package is illuminated directly by high intensity light. No degradation in electrical performance is observed due to illumination by low intensity (0.1 mW/cm^2) ambient light. Figure 50 shows that I_B increases with increasing wavelength and intensity of incident light; I_B can reach levels as high as 4500 pA at a light intensity of 3 mW/cm^2 and a wavelength of 850 nm. The light intensities

shown in Figure 50 are not normal for most applications, i.e., even though direct sunlight can have intensities of 50 mW/cm^2, office ambient light can be as low as 0.1 mW/cm^2.

When the MicroCSP package is assembled on the board with the bump-side of the die facing the PCB, reflected light from the PCB surface is incident on active silicon circuit areas and results in the increased I_B. No performance degradation occurs due to illumination of the backside (substrate) of the AD8605ACB. The AD8605ACB is particularly sensitive to incident light with wavelengths in the near infrared range (NIR, 700 nm to 1000 nm). Photons in this waveband have a longer wavelength and lower energy than photons in the visible (400 nm to 700 nm) and near ultraviolet bands (NUV, 200 nm to 400 nm); therefore, they can penetrate more deeply into the active silicon. Incident light with wavelengths greater than 1100 nm has no photo-electric effect on the AD8605ACB because silicon is trans-parent to wave lengths in this range. The spectral content of conventional light sources varies: sunlight has a broad spectral range, with peak intensity in the visible band that falls off in the NUV and NIR bands; fluorescent lamps have significant peaks in the visible but not in the NUV or NIR bands.

Efforts have been made at a product level to reduce the effect of ambient light; the under bump metal (UBM) has been designed to shield the sensitive circuit areas on the active side (bump-side) of the die. However, if an application encounters any light sensitivity with the AD8605ACB, shielding the bump side of the MicroCSP package with opaque material should eliminate this effect. Shielding can be accomplished using materials such as silica filled liquid epoxies that are used in flip chip underfill techniques.
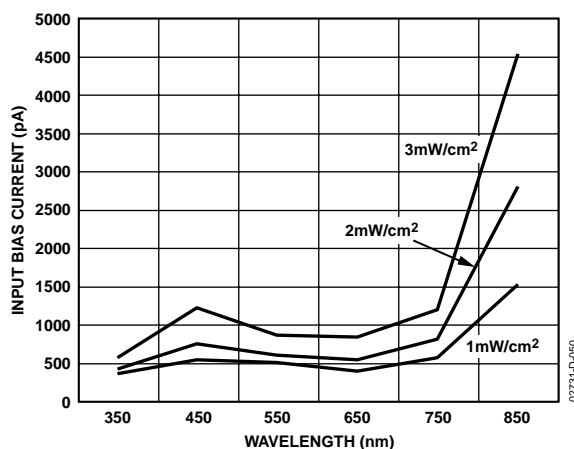

Figure 50. AD8605ACB Input Bias Current Response to Direct Illumination of Varying Intensity and Wavelength

MICROCSP ASSEMBLY CONSIDERATIONS

For detailed information on MicroCSP PCB assembly and reliability, refer to ADI Application Note AN-617 on the ADI website www.analog.com.

I-V CONVERSION APPLICATIONS

PHOTODIODE PREAMPLIFIER APPLICATIONS

The low offset voltage and input current of the AD8605 make it an excellent choice for photodiode applications. In addition, the low voltage and current noise make the amplifier ideal for application circuits with high sensitivity.
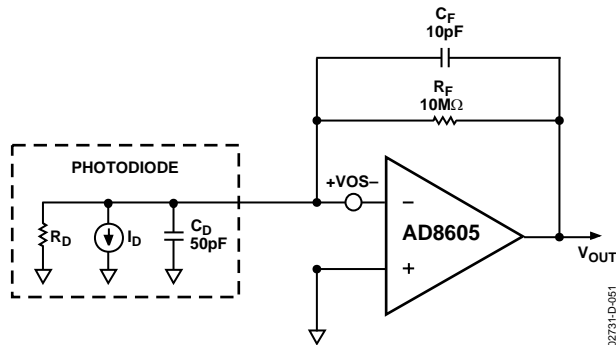
Figure 51. Equivalent Circuit for Photodiode Preamp

The input bias current of the amplifier contributes an error term that is proportional to the value of R_F.

The offset voltage causes a dark current induced by the shunt resistance of the diode R_D. These error terms are combined at the output of the amplifier. The error voltage is written as

$$E_O = V_{OS}\left(1 + \frac{R_F}{R_D}\right) + R_F I_B$$

Typically, R_F is smaller than R_D, thus R_F/R_D can be ignored.

At room temperature, the AD8605 has an input bias current of 0.2 pA and an offset voltage of 100 µV. Typical values of R_D are in the range of 1 GΩ.

For the circuit shown in Figure 9, the output error voltage is approximately 100 µV at room temperature, increasing to about 1 mV at 85°C.

Where f_t is the unity gain frequency of the amplifier, the maximum achievable signal bandwidth is

$$f_{MAX} = \sqrt{\frac{f_t}{2\pi R_F C_T}}$$

AUDIO AND PDA APPLICATIONS

The AD8605's low distortion and wide dynamic range make it a great choice for audio and PDA applications, including microphone amplification and line output buffering.

Figure 52 shows a typical application circuit for headphone/line out amplification.

R1 and R2 are used to bias the input voltage at half the supply. This maximizes the signal bandwidth range. C1 and C2 are used to ac couple the input signal. C1 and R2 form a high-pass filter whose corner frequency is 1/2πR1C1.

The high output current of the AD8605 allows it to drive heavy resistive loads.

The circuit of Figure 52 was tested to drive a 16 W headphone. The THD + N is maintained at approximately −60 dB throughout the audio range.

Figure 52. Single-Supply Headphone/Speaker Amplifier

INSTRUMENTATION AMPLIFIERS

The low offset voltage and low noise of the AD8605 make it a great amplifier for instrumentation applications.

Difference amplifiers are widely used in high accuracy circuits to improve the common-mode rejection ratio.

Figure 53 shows a simple difference amplifier. The CMRR of the circuit is plotted versus frequency. Figure 54 shows the common-mode rejection for a unity gain configuration and for a gain of 10.

Making (R4/R3) = (R2/R1) and choosing 0.01% tolerance yields a CMRR of 74 dB and minimizes the gain error at the output.
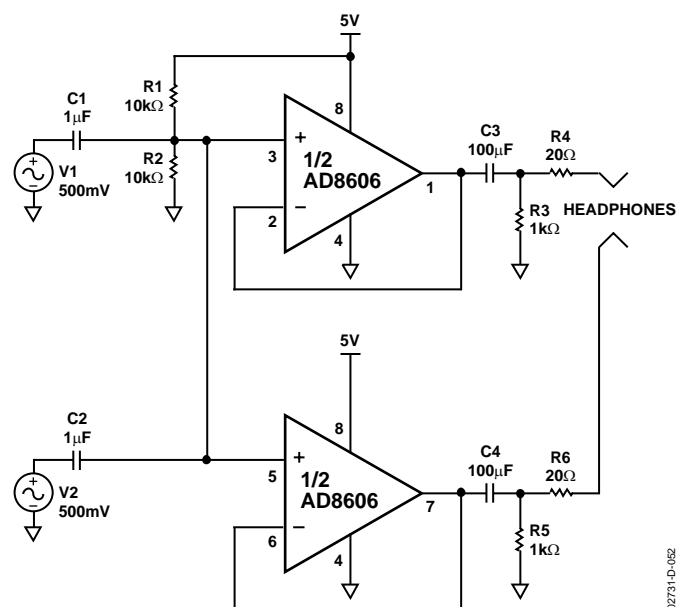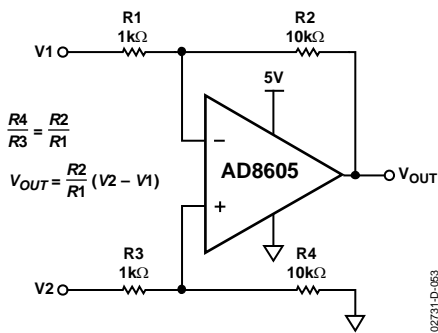

Figure 53. Difference Amplifier, $A_V = 10$
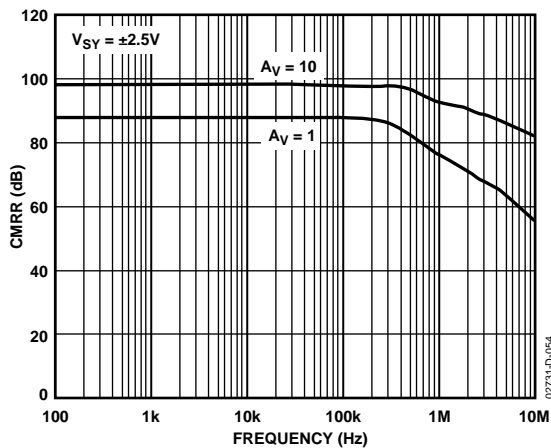
Figure 54. Difference Amplifier CMRR vs. Frequency

D/A CONVERSION

The low input bias current and offset voltage of the AD8605 make it an excellent choice for buffering the output of a current output DAC.

Figure 55 shows a typical implementation of the AD8605 at the output of a 12-bit DAC.

The DAC8143 output current is converted to a voltage by the feedback resistor. The equivalent resistance at the output of the DAC varies with the input code, as does the output capacitance.
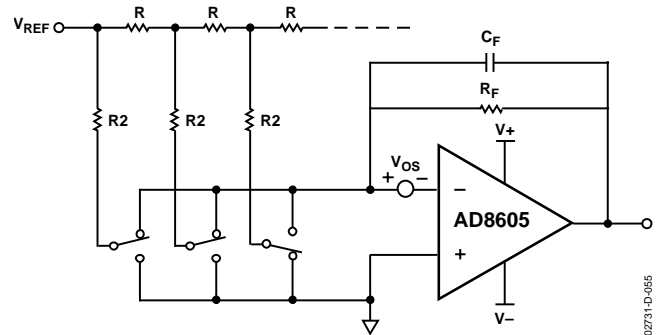
Figure 55. Simplified Circuit of the DAC8143 with AD8605 Output Buffer

To optimize the performance of the DAC, insert a capacitor in the feedback loop of the AD8605 to compensate the amplifier from the pole introduced by the output capacitance of the DAC. Typical values for C_F are in the range of 10 pF to 30 pF; it can be adjusted for the best frequency response. The total error at the output of the op amp can be computed by the formula:

$$E_O = V_{OS}\left(1 + \frac{R_F}{Re\,q}\right)$$

where Req is the equivalent resistance seen at the output of the DAC. As mentioned above, Req is code dependant and varies with the input. A typical value for Req is 15 kΩ. Choosing a feedback resistor of 10 kΩ yields an error of less than 200 µV.

Figure 56 shows the implementation of a dual-stage buffer at the output of a DAC. The first stage is used as a buffer. Capacitor C1, with Req, creates a low-pass filter and thus provides phase lead to compensate for frequency response. The second stage of the AD8606 is used to provide voltage gain at the output of the buffer.

Grounding the positive input terminals in both stages reduces errors due to the common-mode output voltage. Choosing R1, R2, and R3 to match within 0.01% yields a CMRR of 74 dB and maintains minimum gain error in the circuit.

Figure 56. Bipolar Operation

OUTLINE DIMENSIONS

2.90 BSC

1.60 BSC

2.80 BSC

5   4

1   2   3

PIN 1

0.95 BSC

**1.90
BSC**

**1.30
1.15
0.90**

1.45 MAX

0.15 MAX

**0.22
0.08**

**0.50
0.30**

**SEATING
PLANE**

**10°
5°
0°**

**0.60
0.45
0.30**

COMPLIANT TO JEDEC STANDARDS MO-178AA

Figure 57. 5-Lead Small Outline Transistor Package [SOT-23] (RT-5)

**8.75 (0.3445)
8.55 (0.3366)**

**4.00 (0.1575)
3.80 (0.1496)**

14   8

1   7

**6.20 (0.2441)
5.80 (0.2283)**

**1.27 (0.0500)
BSC**

**0.25 (0.0098)
0.10 (0.0039)**

**1.75 (0.0689)
1.35 (0.0531)**

**0.50 (0.0197)
0.25 (0.0098)** × 45°

**COPLANARITY
0.10**

**0.51 (0.0201)
0.31 (0.0122)**

**SEATING
PLANE**

**8°
0°**

**0.25 (0.0098)
0.17 (0.0067)**

**1.27 (0.0500)
0.40 (0.0157)**

**COMPLIANT TO JEDEC STANDARDS MS-012AB
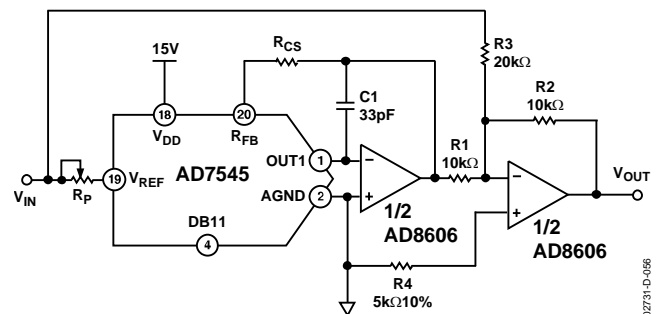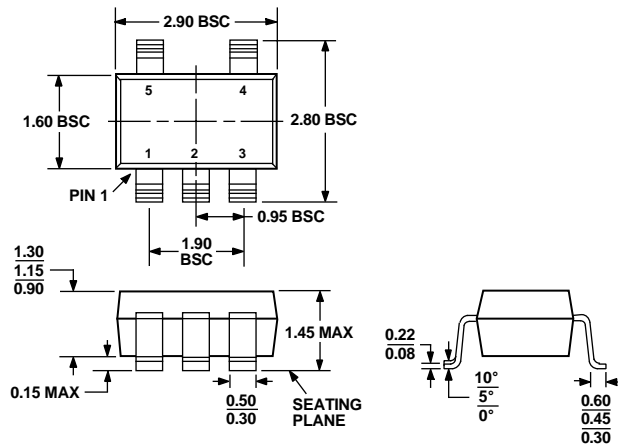CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN**

*Figure 58. 14-Lead Standard Small Outline Package [SOIC]
Narrow Body (R-14)*

**3.00
BSC**

**3.00
BSC**

8   5

4

**4.90
BSC**

PIN 1

0.65 BSC

**0.15
0.00**

1.10 MAX

**0.38
0.22**

**COPLANARITY
0.10**

**SEATING
PLANE**

**0.23
0.08**

**8°
0°**

**0.80
0.60
0.40**

COMPLIANT TO JEDEC STANDARDS MO-187AA
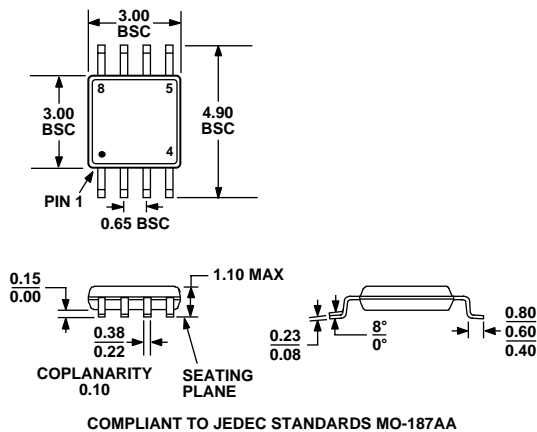
Figure 59. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

**5.00 (0.1968)
4.80 (0.1890)**

8   5

1   4

**4.00 (0.1574)
3.80 (0.1497)**

**6.20 (0.2440)
5.80 (0.2284)**

**1.27 (0.0500)
BSC**

**1.75 (0.0688)
1.35 (0.0532)**

**0.50 (0.0196)
0.25 (0.0099)** × 45°

**0.25 (0.0098)
0.10 (0.0040)**

**COPLANARITY
0.10**

**0.51 (0.0201)
0.31 (0.0122)**

**SEATING
PLANE**

**8°
0°**

**0.25 (0.0098)
0.17 (0.0067)**

**1.27 (0.0500)
0.40 (0.0157)**

**COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN**

Figure 60. 8-Lead Standard Small Outline Package [SOIC] Narrow Body (R-8)

**5.10
5.00
4.90**

**4.50
4.40
4.30**

14   8

1   7

**6.40
BSC**

PIN 1

**1.05
1.00
0.80**

**0.65
BSC**

**1.20
MAX**

**0.15
0.05**

**0.30
0.19**

**SEATING
PLANE**

**0.20
0.09**

**8°
0°**

**COPLANARITY
0.10**

**0.75
0.60
0.45**

COMPLIANT TO JEDEC STANDARDS MO-153AB-1
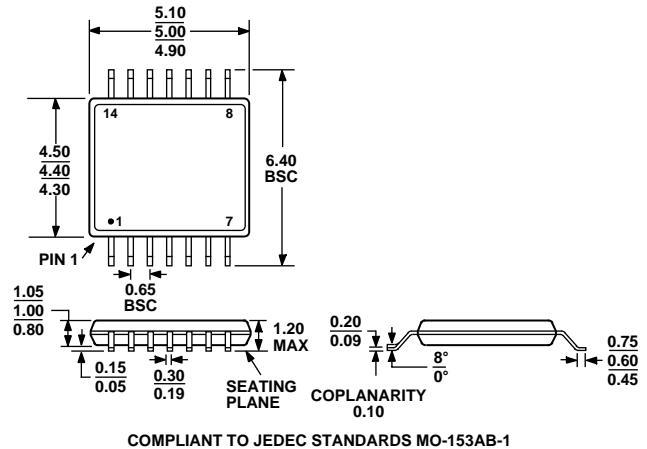
Figure 61. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)

**0.94
0.90
0.86**

**0.37
0.36
0.35**

0.50 REF

**SEATING
PLANE**

BOTTOM VIEW

**PIN 1
IDENTIFIER**

TOP VIEW
(BALL SIDE DOWN)

**1.33
1.29
1.25**

0.87

**0.23
0.18
0.14**

0.50

0.21

**0.17
0.14
0.12**

0.50

0.20

Figure 62. 5-Bump 2 × 1 × 2 Array MicroCSP [WLCSP] (CB-5)

ORDERING GUIDE

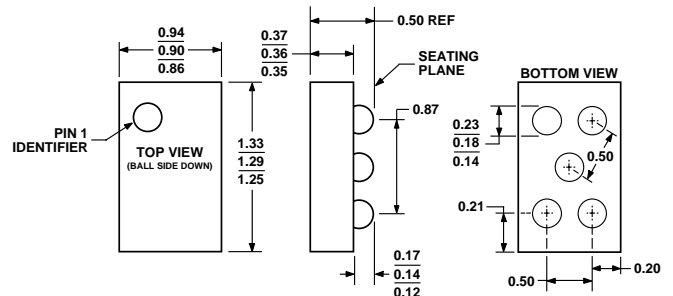| Model	Temperature Range	Package Description	Package Option	Branding
AD8605ACB-REEL	−40°C to +125°C	5-Bump MicroCSP	CB-5	B3A
AD8605ACB-REEL7	−40°C to +125°C	5-Bump MicroCSP	CB-5	B3A
AD8605ART-R2	−40°C to +125°C	5-Lead SOT-23	RT-5	B3A
AD8605ART-REEL	−40°C to +125°C	5-Lead SOT-23	RT-5	B3A
AD8605ART-REEL7	−40°C to +125°C	5-Lead SOT-23	RT-5	B3A
AD8605ARTZ-REEL[1]	−40°C to +125°C	5-Lead SOT-23	RT-5	B3A
AD8605ARTZ-REEL7[1]	−40°C to +125°C	5-Lead SOT-23	RT-5	B3A
AD8606ARM-R2	−40°C to +125°C	8-Lead MSOP	RM-8	B6A
AD8606ARM-REEL	−40°C to +125°C	8-Lead MSOP	RM-8	B6A
AD8606AR	−40°C to +125°C	8-Lead SOIC	R-8	
AD8606AR-REEL	−40°C to +125°C	8-Lead SOIC	R-8	
AD8606AR-REEL7	−40°C to +125°C	8-Lead SOIC	R-8	
AD8608AR	−40°C to +125°C	14-Lead SOIC	R-14	
AD8608AR-REEL	−40°C to +125°C	14-Lead SOIC	R-14	
AD8608AR-REEL7	−40°C to +125°C	14-Lead SOIC	R-14	
AD8608ARU	−40°C to +125°C	14-Lead TSSOP	RU-14	
AD8608ARU-REEL	−40°C to +125°C	14-Lead TSSOP	RU-14	

[1] Z = Pb-free part.

NOTES

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