UNITRODE

**UC1901**
**UC2901**
**UC3901**

# Isolated Feedback Generator

## FEATURES

- An Amplitude-Modulation System for Transformer Coupling an Isolated Feedback Error Signal
- Low-Cost Alternative to Optical Couplers
- Internal 1% Reference and Error Amplifier
- Internal Carrier Oscillator Usable to 5MHz
- Modulator Synchronizable to an External Clock
- Loop Status Monitor

## DESCRIPTION

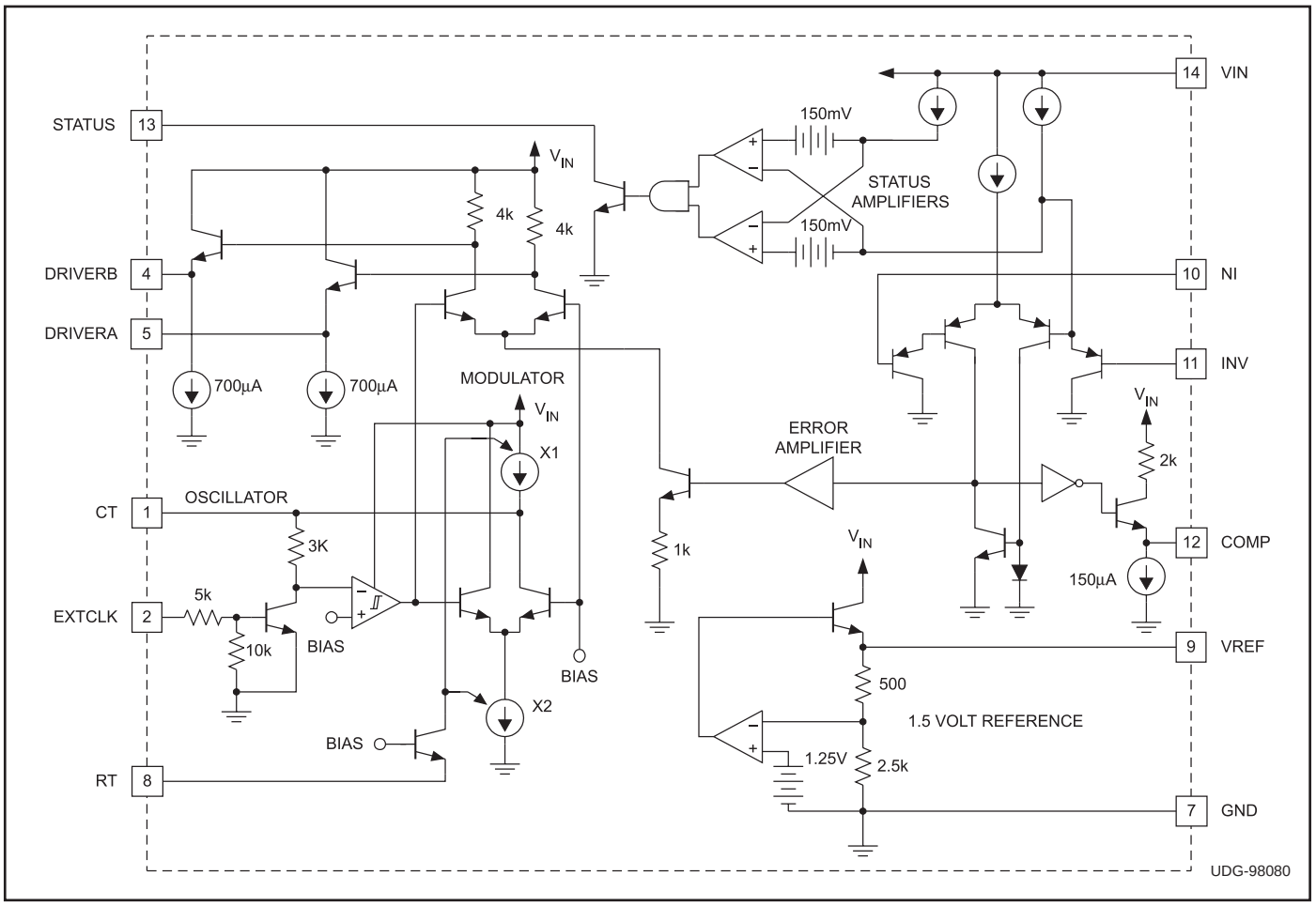
The UC1901 family is designed to solve many of the problems associated with closing a feedback control loop across a voltage isolation boundary. As a stable and reliable alternative to an optical coupler, these devices feature an amplitude modulation system which allows a loop error signal to be coupled with a small RF transformer or capacitor.

The programmable, high-frequency oscillator within the UC1901 series permits the use of smaller, less expensive transformers which can readily be built to meet the isolation requirements of today's line-operated power systems. As an alternative to RF operation, the external clock input to these devices allows synchronization to a system clock or to the switching frequency of a SMPS.

An additional feature is a status monitoring circuit which provides an active-low output when the sensed error voltage is within ±10% of the reference. The DRIVERA output, DRIVERB output, and STATUS output are disabled until the input supply has reached a sufficient level to allow proper operation of the device.

Since these devices can also be used as a DC driver for optical couplers, the benefits of 4.5 to 40V supply operation, a 1% accurate reference, and a high gain general purpose amplifier offer advantages even though an AC system may not be desired.

## UC1901 SIMPLIFIED SCHEMATICNovember S



## ABSOLUTE MAXIMUM RATINGS *(Note 1)*

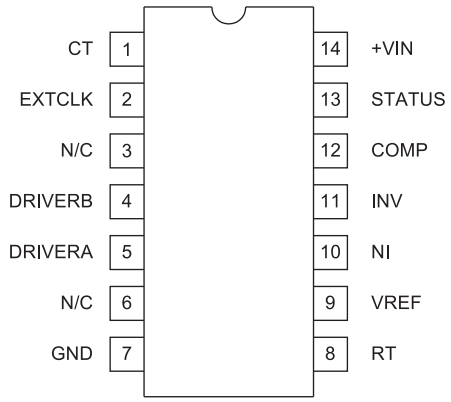
Input Supply Voltage, $V_{IN}$ . . . . . 40V
Reference Output Current . . . . . –10mA
Driver Output Currents . . . . . –35mA
Status Indicator Voltage . . . . . 40V
Status Indicator Current . . . . . 20mA
Ext. Clock Input . . . . . 40V
Error Amplifier Inputs . . . . . –0.5V to +35V
Power Dissipation at $T_A$ = 25°C . . . . . 1000mW
Power Dissipation at $T_C$ = 25°C . . . . . 2000mW
Operating Junction Temperature . . . . . –55°C to +150°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

***Note 1****: Voltages are referenced to ground, Pin 7. Currents are positive into, negative out of the specified terminal.*

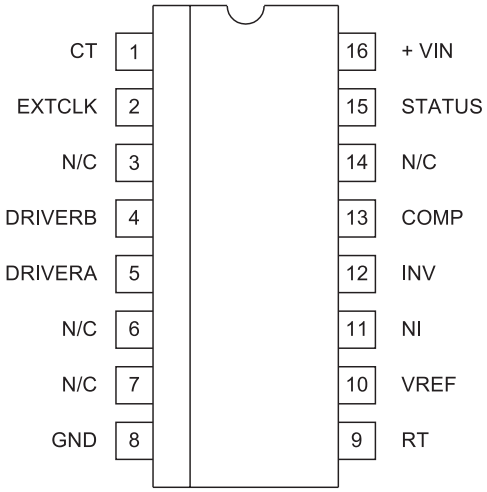
***Note 2****: Consult Packaging section of Databook for thermal limitations and considerations of package.*

## CONNECTION DIAGRAMS

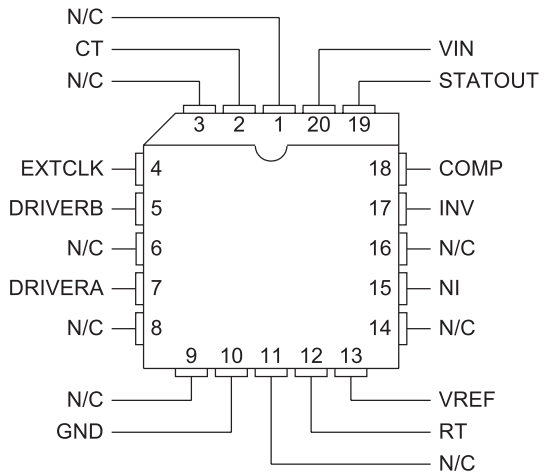
**DIL-14, SOIC-14 (TOP VIEW)**
**J or N Package, D Package**




**SOIC-16 Wide (TOP VIEW)**
**DW Package**




**PLCC-20, LCC-20 (TOP VIEW)**
**Q, L Packages**




## TEMPERATURE AND PACKAGE SELECTION GUIDE

| | TEMPERATURE RANGE | AVAILABLE PACKAGES |
|---|---|---|
| UC1901 | –55°C to +125°C | J, L |
| UC2901 | –40°C to +85°C | D, DW, J, N, Q |
| UC3901 | 0°C to +70°C | D, DW, J, N, Q |

**ELECTRICAL CHARACTERISTICS** Unless otherwise stated, these specifications apply for $V_{IN}$ = 10V, $R_T$ = 10kΩ, $C_T$ = 820pF, $T_A = T_J$.

| PARAMETER | TEST CONDITIONS | UC1901/UC2901 | | | UC3901 | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **Reference Section** | | | | | | | | |
| Output Voltage | $T_J$ = 25°C | 1.485 | 1.5 | 1.515 | 1.47 | 1.5 | 1.53 | V |
| | $T_{MIN} \le T_J \le T_{MAX}$ | 1.470 | 1.5 | 1.530 | 1.455 | 1.5 | 1.545 | |
| Line Regulation | $V_{IN}$ = 4.5 to 35V | | 2 | 10 | | 2 | 15 | mV |
| Load Regulation | $I_{OUT}$ = 0 to 5mA | | 4 | 10 | | 4 | 15 | mV |
| Short Circuit Current | $T_J$ = 25°C | | –35 | –55 | | –35 | –55 | mV |
| **Error Amplifier Section** (To Compensation Terminal) | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 1.5V | | 1 | 4 | | 1 | 8 | mV |
| Input Bias Current | $V_{CM}$ = 1.5V | | –1 | –3 | | –1 | –6 | µA |
| Input Offset Current | $V_{CM}$ = 1.5V | | 0.1 | 1 | | 0.1 | 2 | µA |
| Small Signal Open Loop Gain | | 40 | 60 | | 40 | 60 | | dB |
| CMRR | $V_{CM}$ = 0.5 to 7.5V | 60 | 80 | | 60 | 80 | | dB |
| PSRR | $V_{IN}$ = 5 to 25V | 80 | 100 | | 80 | 100 | | dB |
| Output Swing, Δ $V_O$ | | 0.4 | 0.7 | | 0.4 | 0.7 | | V |
| Maximum Sink Current | | 90 | 150 | | 90 | 150 | | µA |
| Maximum Source Current | | –2 | –3 | | –2 | –3 | | mA |
| Gain Band Width Product | | | 1 | | | 1 | | MHz |
| Slew Rate | | | 0.3 | | | 0.3 | | V/µS |
| **Modulators/Drivers Section** (From Compensation Terminal) | | | | | | | | |
| Voltage Gain | | 11 | 12 | 13 | 10 | 12 | 14 | dB |
| Output Swing | | ±1.6 | ±2.8 | | ±1.6 | ±2.8 | | V |
| Driver Sink Current | | 500 | 700 | | 500 | 700 | | µA |
| Driver Source Current | | –15 | –35 | | –15 | –35 | | mA |
| Gain Band Width Product | | | 25 | | | 25 | | MHz |
| **Oscillator Section** | | | | | | | | |
| Initial Accuracy | $T_J$ = 25°C | 140 | 150 | 160 | 130 | 150 | 170 | kHz |
| | $T_{MIN} \le T_J \le T_{MAX}$ | 130 | | 170 | 120 | | 180 | kHz |
| Line Sensitivity | $V_{IN}$ = 5 to 35V | | .15 | .35 | | .15 | .60 | %/V |
| Maximum Frequency | $R_T$ = 10k, $C_T$ = 10pF | | 5 | | | 5 | | MHz |
| Ext. Clock Low Threshold | Pin 1 ($C_T$) = $V_{IN}$ | 0.5 | | | 0.5 | | | V |
| Ext. Clock High Threshold | Pin 1 ($C_T$) = $V_{IN}$ | | | 1.6 | | | 1.6 | V |
| **Status Indicator Section** | | | | | | | | |
| Input Voltage Window | @ E/A Inputs, $V_{CM}$ = 1.5V | ±135 | ±150 | ±165 | ±130 | ±150 | ±170 | mV |
| Saturation Voltage | E/A Δ Input = 0V, $I_{SINK}$ = 1.6mA | | | 0.45 | | | 0.45 | V |
| Max. Output Current | Pin 13 = 3V, E/A Δ Input = 0.0V | 8 | 15 | | 8 | 15 | | mA |
| Leakage Current | Pin 13 = 40V, E/A ΔInput = 0.2V | | .05 | 1 | | .05 | 5 | µA |
| Supply Current | $V_{IN}$ = 35V | | 5 | 8 | | 5 | 10 | mA |
| **UVLO Section** | | | | | | | | |
| Drivers Enabled Threshold | At Input Supply $V_{IN}$ | | 3.9 | 4.5 | | 3.9 | 4.5 | V |
| Status Output Enabled Threshold | At Input Supply $V_{IN}$ | | 3.9 | 4.5 | | 3.9 | 4.5 | V |
| Change in Reference Output | When $V_{IN}$ Reaches UVLO Threshold | | –2 | –30 | | –2 | –30 | mV |

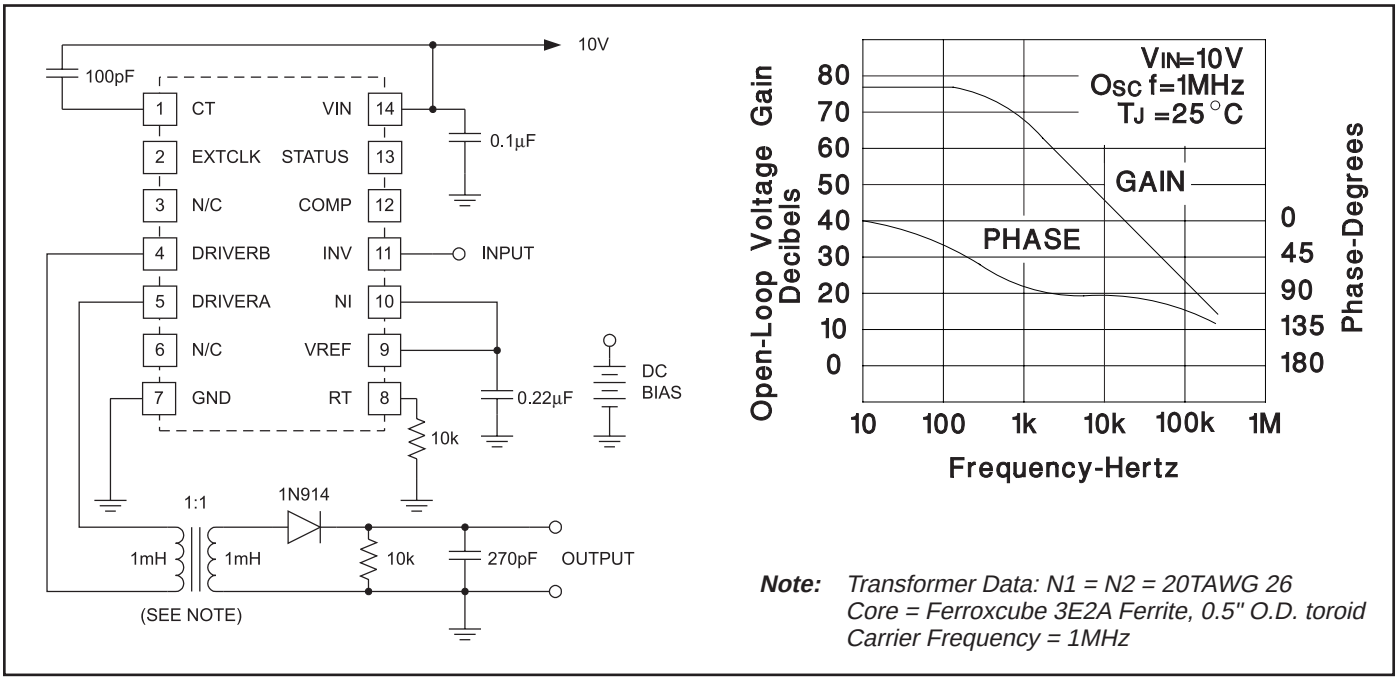



***Figure 1. Transformer Coupled Open Loop Transfer Function***

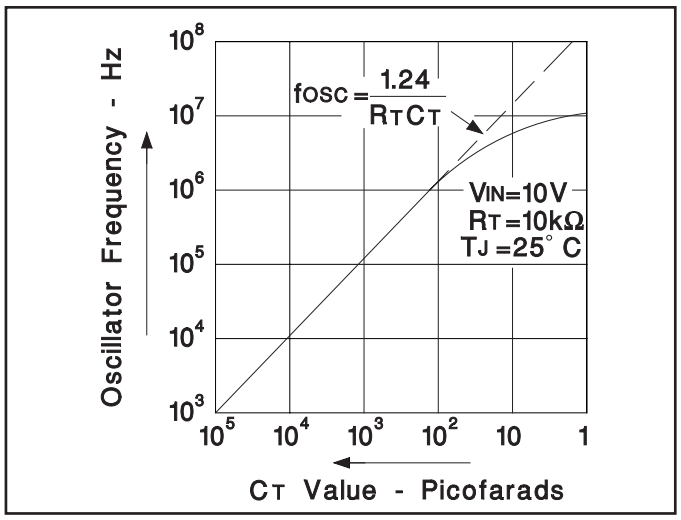



***Figure 2. Oscillator Frequency***

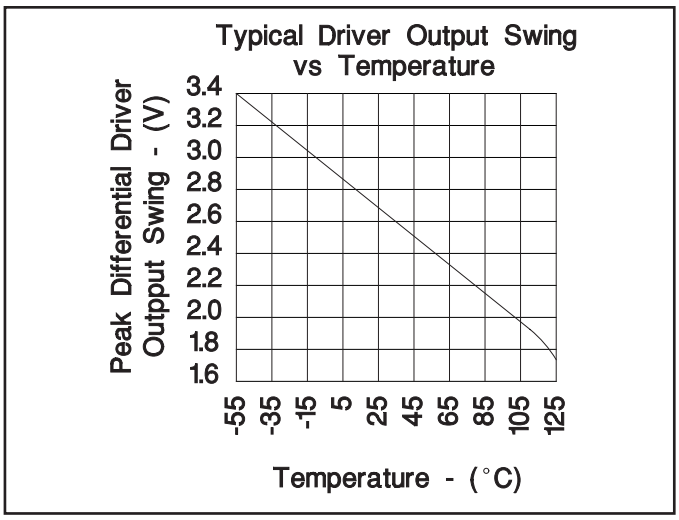



***Figure 3. Typical Driver Output Swing vs Temperature***

## APPLICATION INFORMATION

The error amplifier compensation terminal, Pin 12, is intended as a source of feedback to the amplifier's inverting input at Pin 11. For most applications, a series DC blocking capacitor should be part of the feedback network. The amplifier is internally compensated for unity feedback.

The waveform at the driver outputs is a squarewave with an amplitude that is proportional to the error amplifier input signal. There is a fixed 12dB of gain from the error amplifier compensation pin to the modulator driver outputs. The frequency of the output waveform is controlled by either the internal oscillator or an external clock signal. With the internal oscillator the squarewave will have a fixed 50% duty cycle. If the internal oscillator is disabled by connecting Pin 1, $C_R$, to $V_{IN}$ then the frequency and duty cycle of the output will be determined by the input clock waveform at Pin 2. If the oscillator remains disabled and there is not clock input at Pin 2, there will be a linear 12dB of signal gain to one or the other of the driver outputs depending on the DC state of Pin 2.

The driver outputs are emitter followers which will source a minimum of 15mA of current. The sink current, internally limited at 700µA, can be increased by adding resistors to ground at the driver outputs.

## APPLICATION INFORMATION (continued)

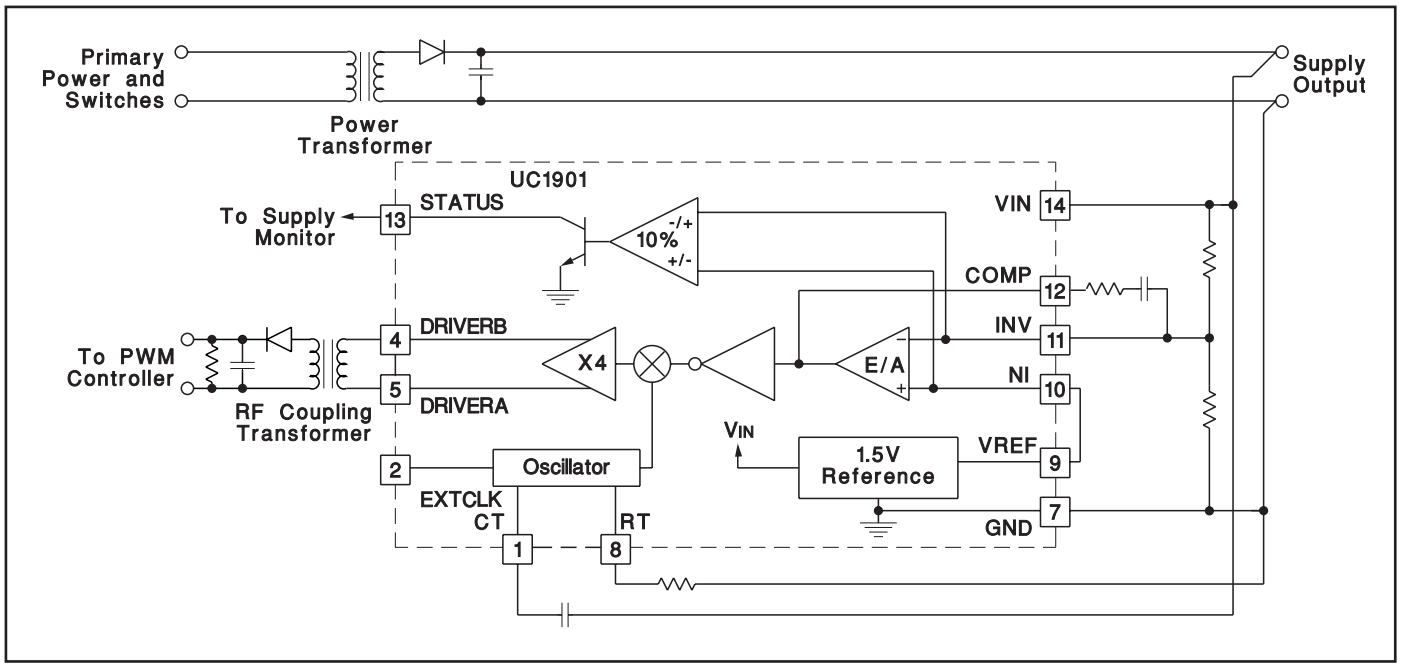



*Figure 4. R.F. Transformer Coupled Feedback*

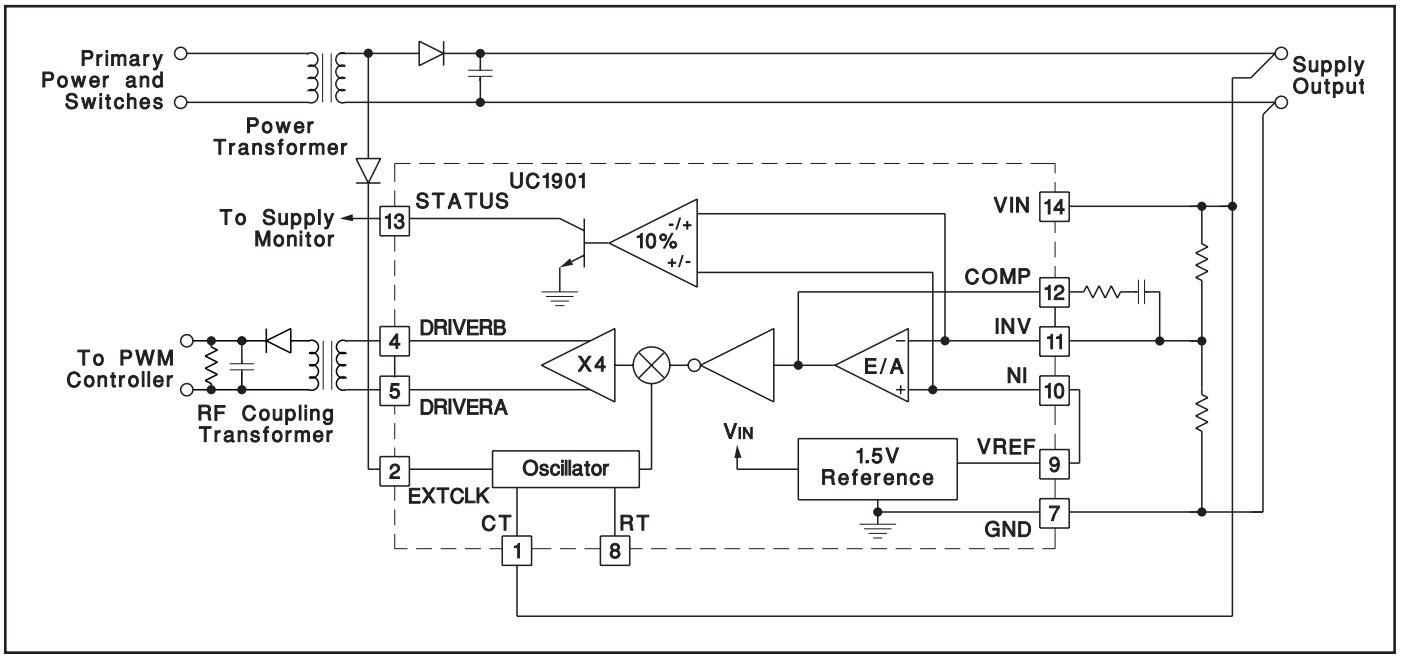
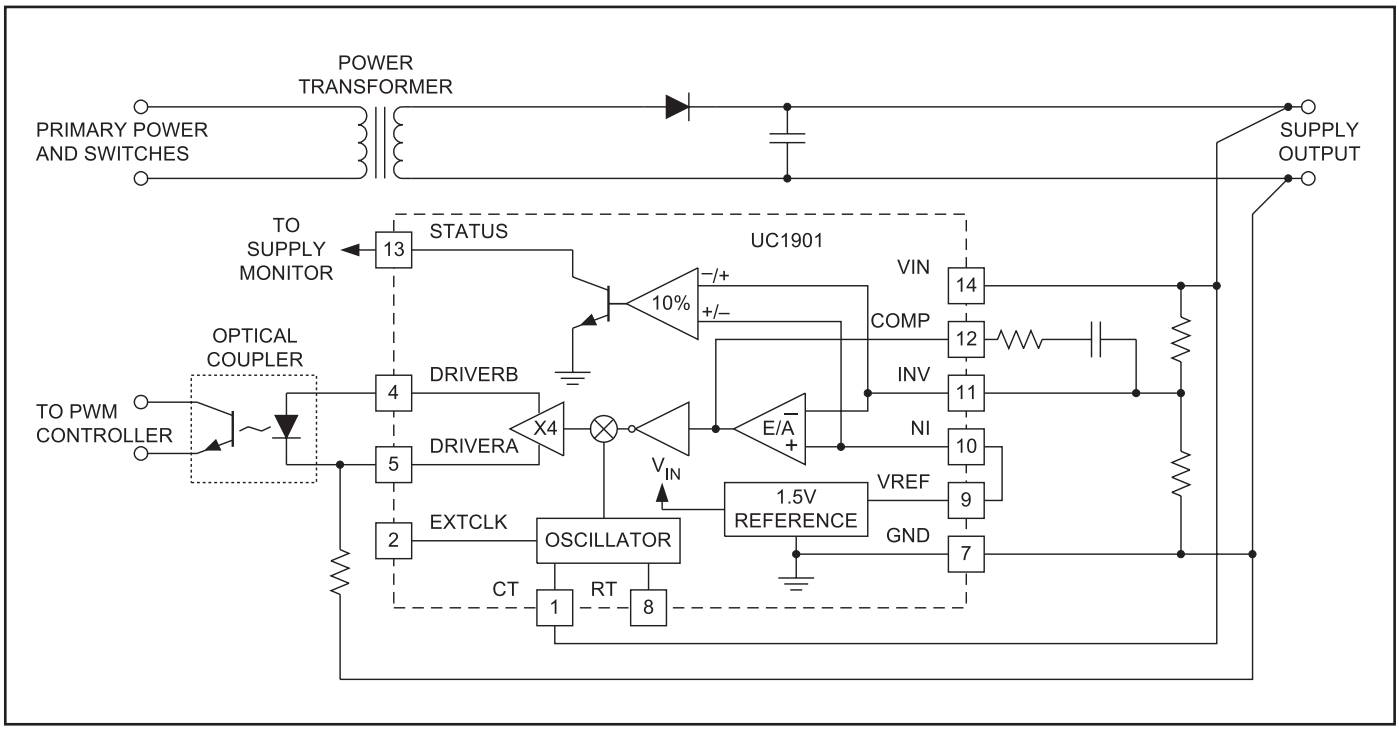



*Figure 5. Feedback Coupled at Switching Frequency*


POWER
TRANSFORMER
PRIMARY POWER
AND SWITCHES
SUPPLY
OUTPUT
TO
SUPPLY
MONITOR
13
STATUS
UC1901
VIN
14
–/+
10%
+/–
COMP
12
OPTICAL
COUPLER
DRIVERB
4
INV
11
TO PWM
CONTROLLER
X4
E/A
NI
10
DRIVERA
5
V
IN
VREF
1.5V
REFERENCE
9
EXTCLK
2
OSCILLATOR
GND
7
CT
RT
1
8

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-89441012A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-89441012A UC1901L/ 883B |
| 5962-8944101CA | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8944101CA UC1901J/883B |
| 5962-8944101VCA | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8944101VCA UC1901JQMLV |
| 5962-8944101VCA.A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8944101VCA UC1901JQMLV |
| UC1901J | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | UC1901J |
| UC1901J.A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | UC1901J |
| UC1901J883B | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8944101CA UC1901J/883B |
| UC1901J883B.A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8944101CA UC1901J/883B |
| UC1901L | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | UC1901L |
| UC1901L.A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | UC1901L |
| UC1901L883B | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-89441012A UC1901L/ 883B |
| UC1901L883B.A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-89441012A UC1901L/ 883B |
| UC2901D | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2901D |
| UC2901D.A | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2901D |
| UC2901DTR | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2901D |
| UC2901DTR.A | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2901D |
| UC2901J | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -40 to 85 | UC2901J |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| UC2901J.A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -40 to 85 | UC2901J |
| UC2901N | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | UC2901N |
| UC2901N.A | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | UC2901N |
| UC3901D | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3901D |
| UC3901D.A | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3901D |
| UC3901DTR | Obsolete | Production | SOIC (D) \| 14 | - | - | Call TI | Call TI | 0 to 70 | UC3901D |
| UC3901DW | Obsolete | Production | SOIC (DW) \| 16 | - | - | Call TI | Call TI | 0 to 70 | UC3901DW |
| UC3901N | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | UC3901N |
| UC3901N.A | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | UC3901N |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF UC1901, UC1901-SP, UC2901, UC2901-MIL, UC3901 :**

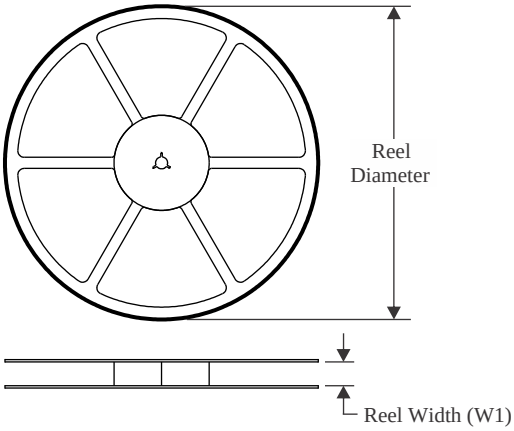
- Catalog : UC3901, UC1901
- Enhanced Product : UC2901-EP, UC2901-EP
- Military : UC1901
- Space : UC1901-SP, UC1901-SP

NOTE: Qualified Version Definitions:

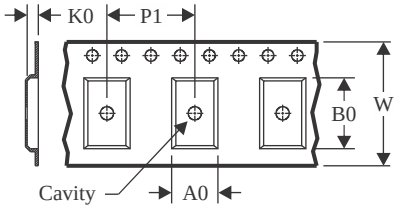
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

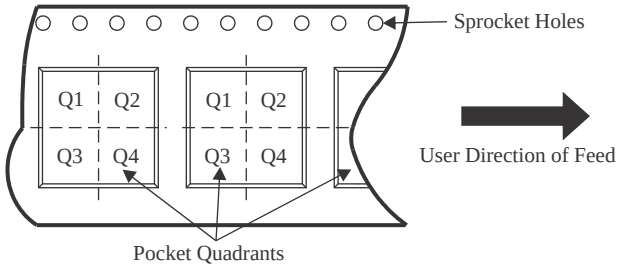



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

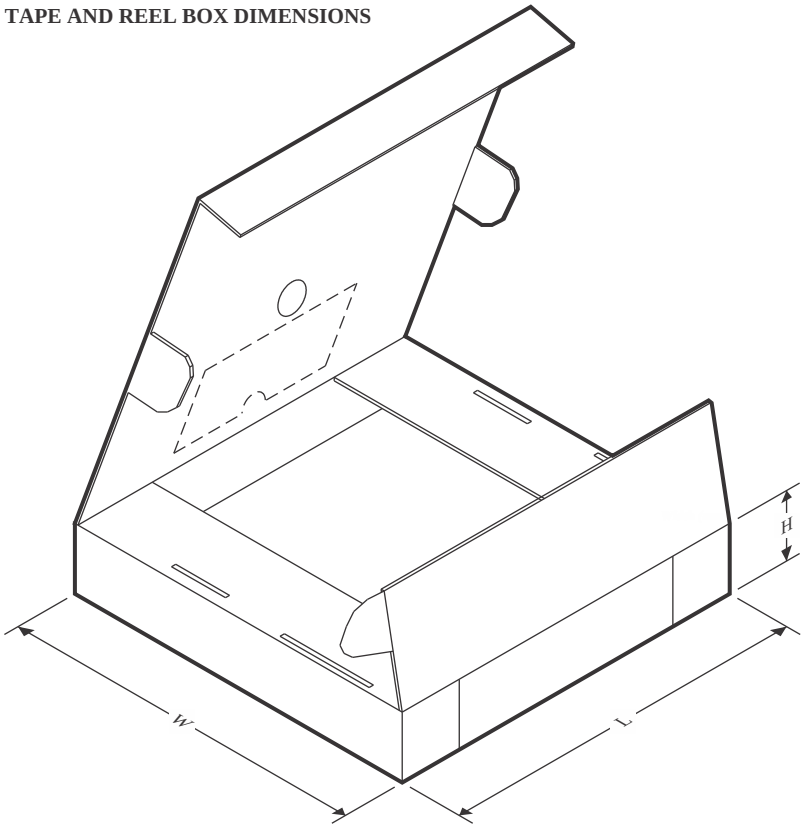
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UC2901DTR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

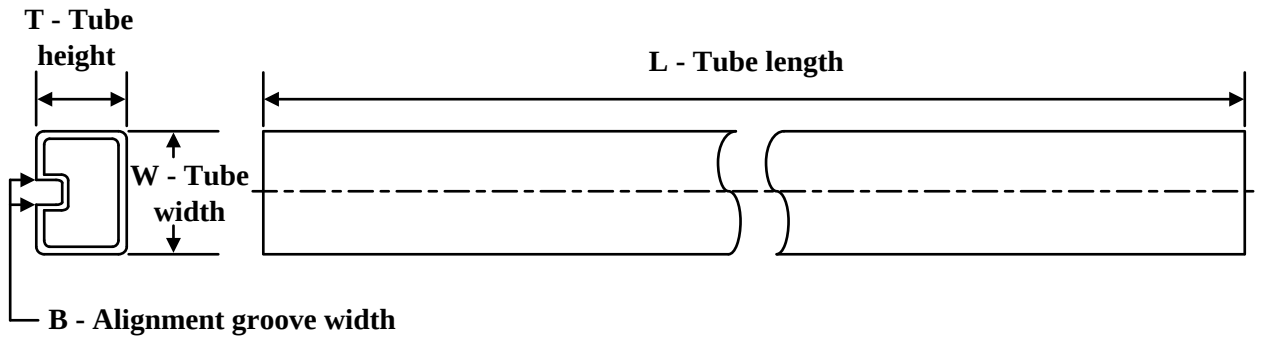
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UC2901DTR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-89441012A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| UC1901L | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| UC1901L.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| UC1901L883B | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| UC1901L883B.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| UC2901D | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| UC2901D.A | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| UC2901N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| UC2901N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| UC3901D | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| UC3901D.A | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| UC3901N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| UC3901N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |

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