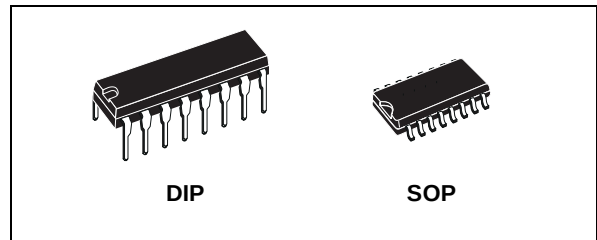


TRIPLE SERIAL ADDER

- INVERT INPUTS ON ALL ADDERS FOR SUM COMPLEMENTING APPLICATIONS
- FULLY STATIC OPERATION...DC TO 10MHz (Typ.) at $V_{DD} = 10V$
- BUFFERED INPUTS AND OUTPUTS
- SINGLE PHASE CLOCKING
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- INPUT LEAKAGE CURRENT
 $I_l = 100nA$ (MAX) AT $V_{DD} = 18V$ $T_A = 25^\circ C$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"

DESCRIPTION

The HCF4032B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. The HCF4032B consists of three serial adder circuits with common CLOCK and CARRY-RESET inputs. Each adder has two provisions for two serial DATA INPUT signals and an INVERT command signal. When the command signal is a logical "1", the sum is complemented.

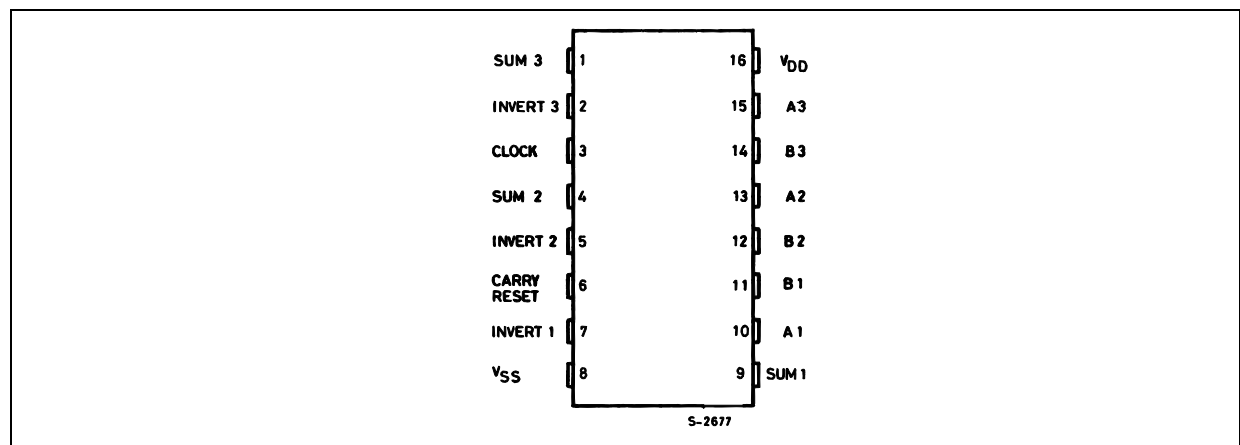


ORDER CODES

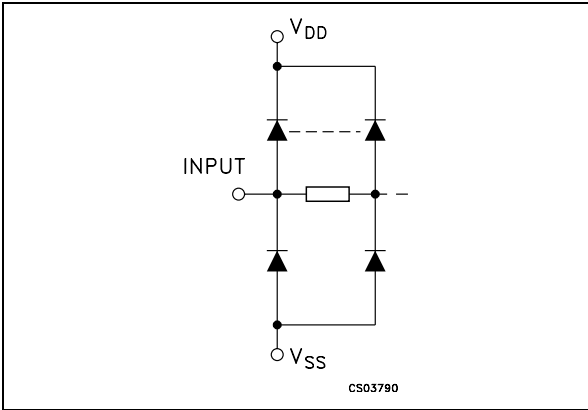
PACKAGE	TUBE	T & R
DIP	HCF4032BEY	
SOP	HCF4032BM1	HCF4032M013TR

Data words enter the adder with the least significant bit first; the sign bit trails. The output is the MOD 2 sum of the input bits plus the carry from the previous bit position. The carry is only added at the positive going clock transition, thus, for spike-free operation the input data transitions should occur as soon as possible after the triggering edge. The CARRY is reset to a logical "0" at the end of each word by applying a logical "1" signal to a CARRY-RESET input one bit position before the application of the first bit of the next word.

PIN CONNECTION



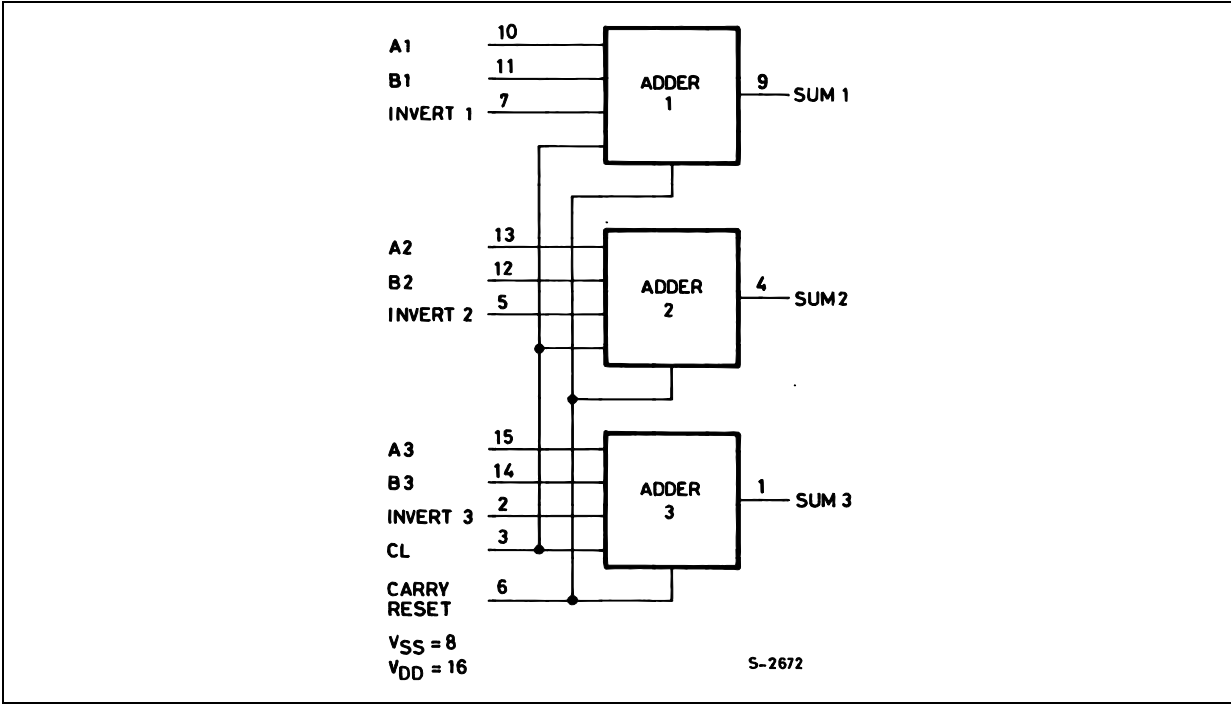
IINPUT EQUIVALENT CIRCUIT



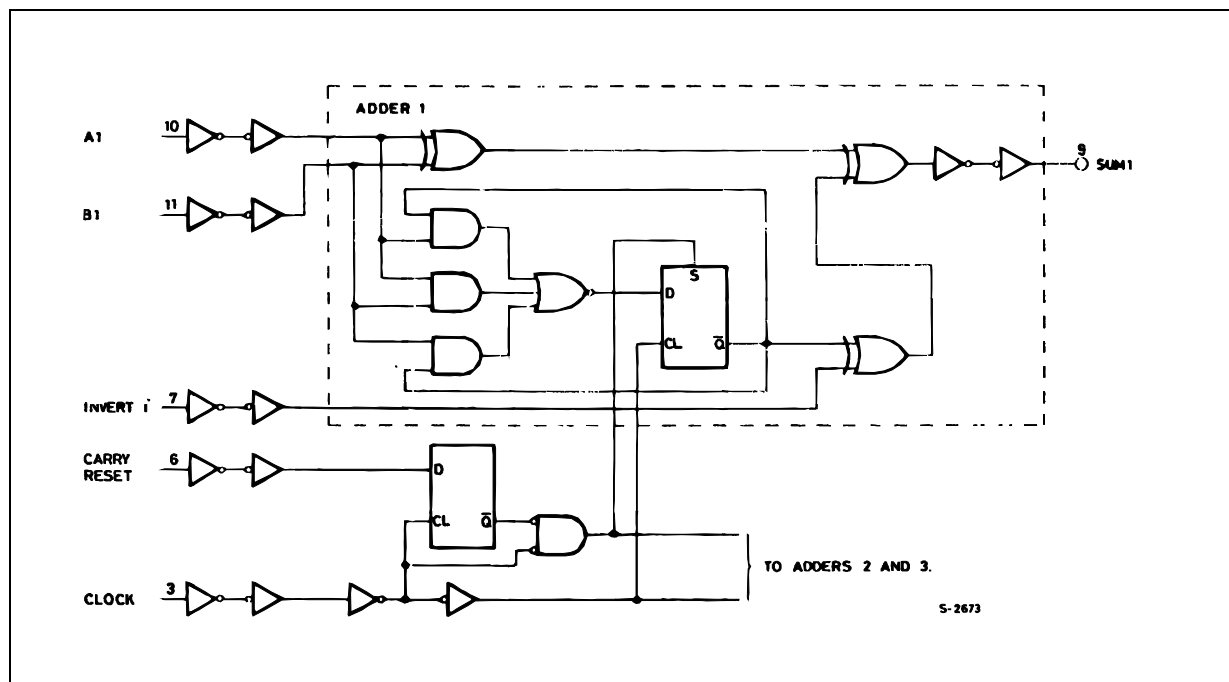
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
10, 13, 15	A1 to A3	Data Inputs
11, 12, 14	B1 to B3	Data Inputs
7, 5, 2	INVERT1 to INVERT3	Invert Command Inputs
9, 4, 1	SUM1 to SUM3	Data Outputs
3	CLOCK	Clock Input
6	CARRY-RESET	Carry Reset Input
8	V _{SS}	Negative Supply Voltage
16	V _{DD}	Positive Supply Voltage

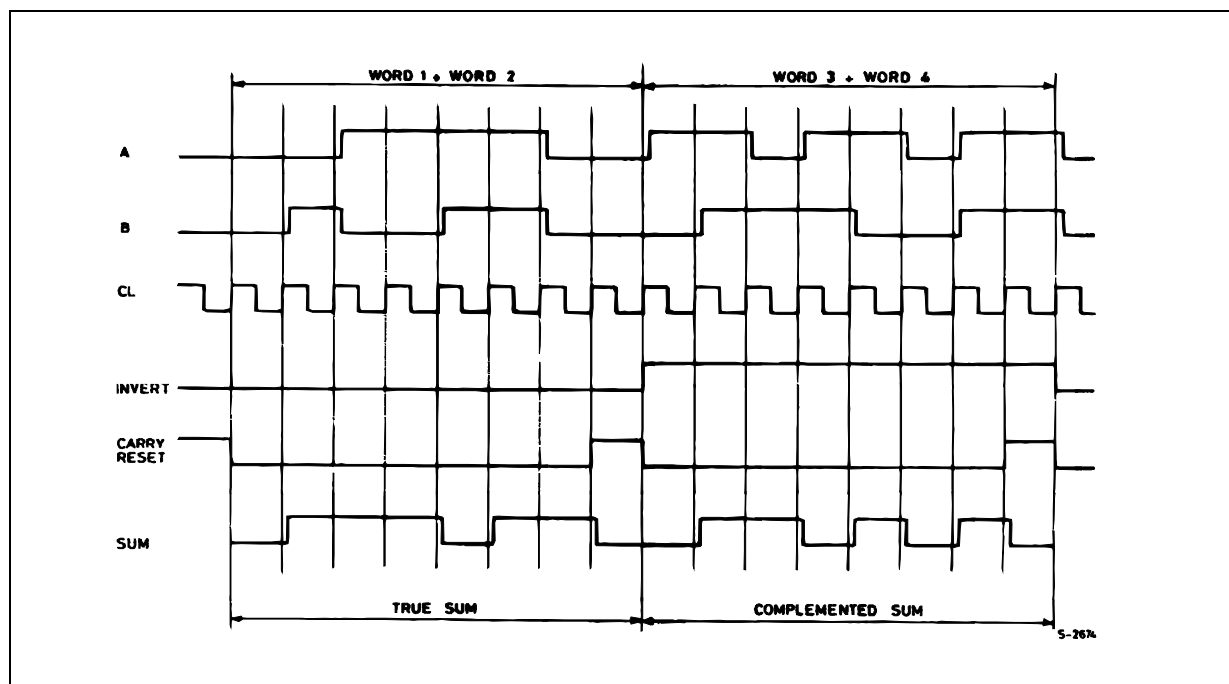
FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

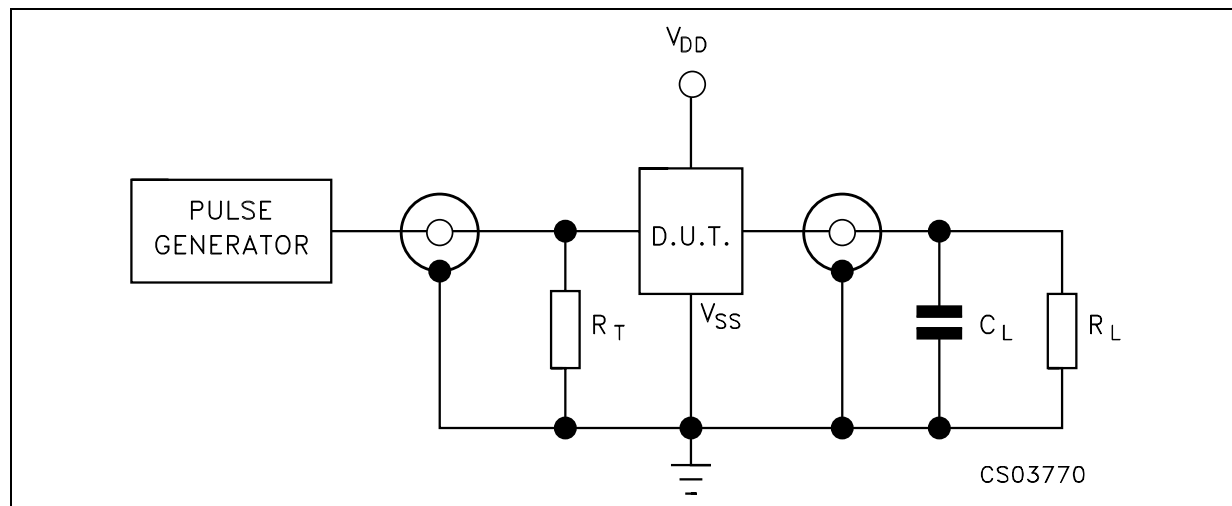
DC SPECIFICATIONS

Symbol	Parameter	Test Conditions				Value							Unit
		V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I _L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V _{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V _{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V _{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/18.5	<1	15	11			11		11		
V _{IL}	Low Level Input Voltage		0.5/4.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			1.5/18.5	<1	15			4		4		4	
I _{OH}	Output Drive Current	0/5	2.5		5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6		5	-0.44	-1		-0.36		-0.36		
		0/10	9.5		10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5		15	-3.0	-6.8		-2.4		-2.4		
I _{OL}	Output Sink Current	0/5	0.4		5	0.44	1		0.36		0.36		mA
		0/10	0.5		10	1.1	2.6		0.9		0.9		
		0/15	1.5		15	3.0	6.8		2.4		2.4		
I _I	Input Leakage Current	0/18	any input		18		±10 ⁻⁵	±0.1		±1		±1	μA
C _I	Input Capacitance		any input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

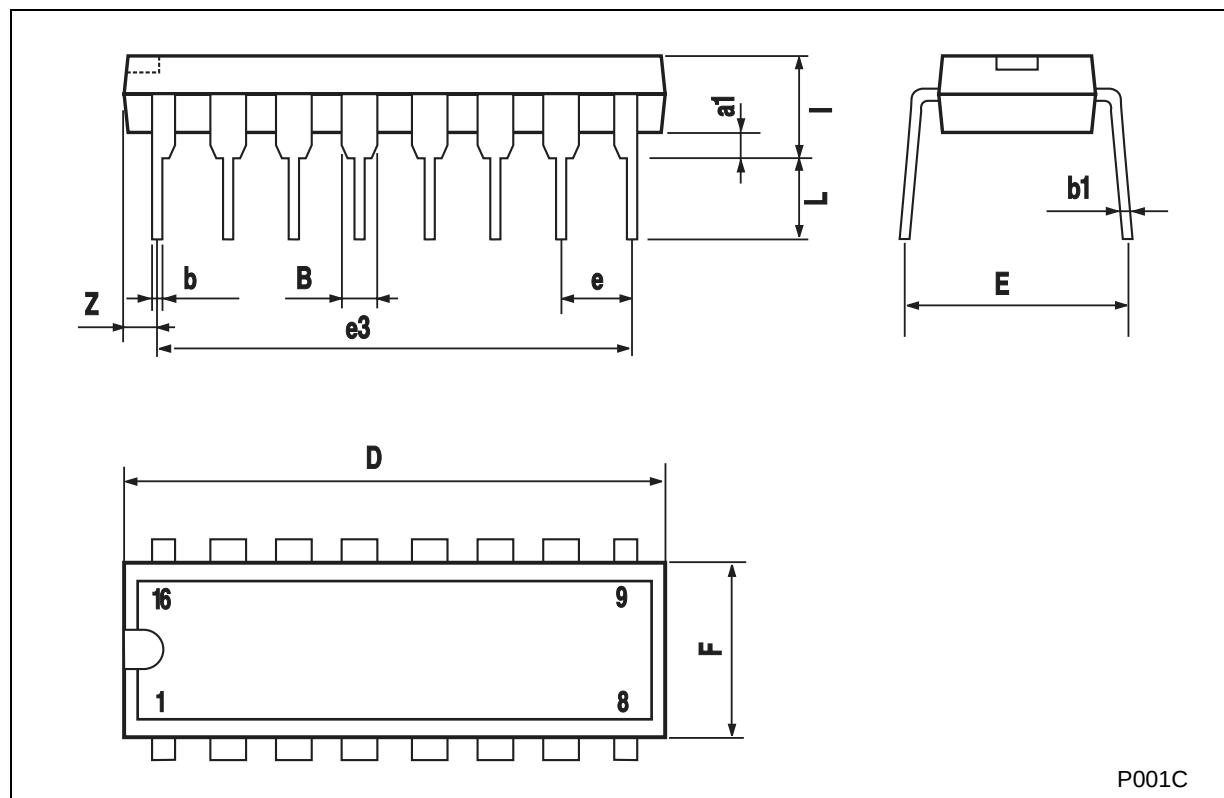
DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $C_L = 50\text{pF}$, $R_L = 200\text{K}\Omega$, $t_r = t_f = 20\text{ ns}$)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PHL} t_{PLH}	Propagation Delay Time (A, B or Inverter Inputs to Sum Outputs)	5			260	520	ns
		10			120	240	
		15			90	180	
t_{PHL} t_{PLH}	Propagation Delay Time (Clock Inputs to Sum Outputs)	5			325	650	ns
		10			175	350	
		15			150	300	
t_{THL} t_{TLH}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
t_{hold}	Data Input Hold Time (clock edge to A, B, or reset inputs)	5			120	200	ns
		10			50	80	
		15			40	60	
f_{MAX}	Maximum Clock Input Frequency	5		2.5	4.5		MHz
		10		5	10		
		15		7.5	15		
t_r , t_f ⁽¹⁾	Clock Input Rise or Fall Time	5				500	μs
		10				500	
		15				500	

(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.(1) If more than one unit is cascaded t_r should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving state for the estimated capacitive load.**TEST CIRCUIT** $C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance) $R_L = 200\text{K}\Omega$ $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

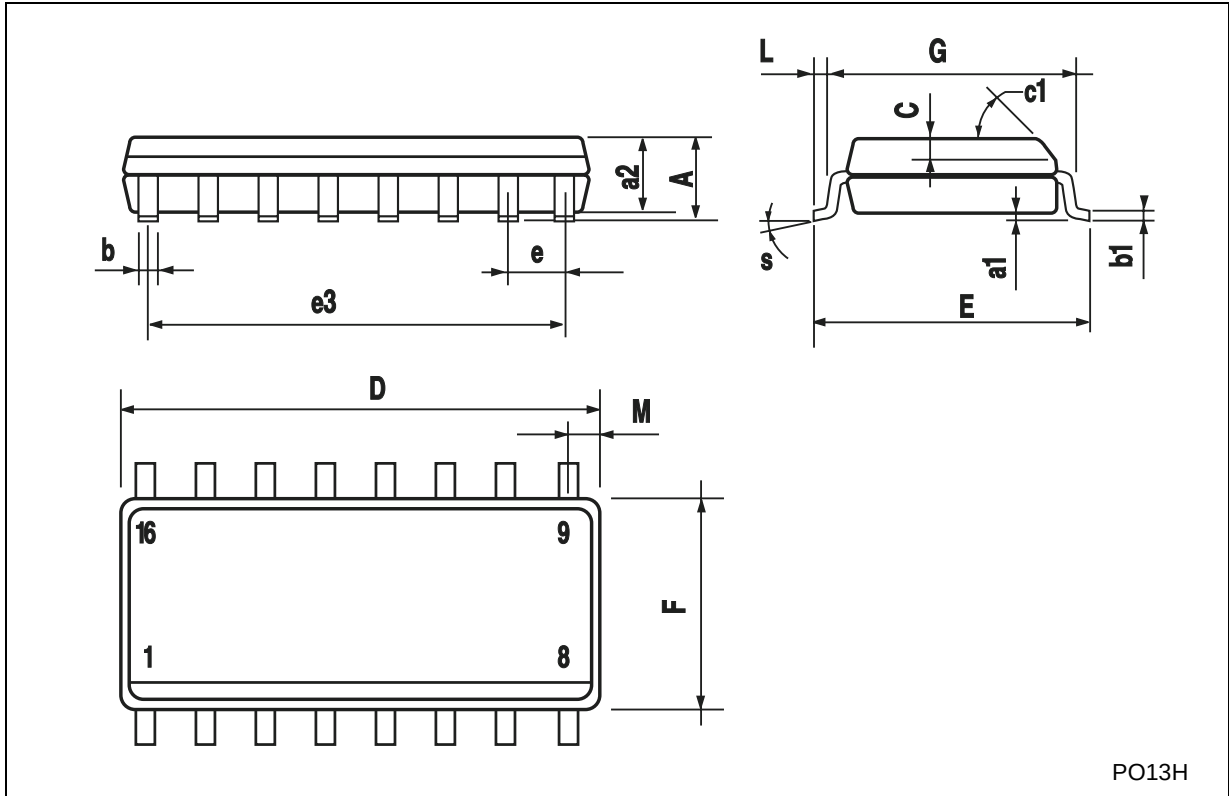
Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>

