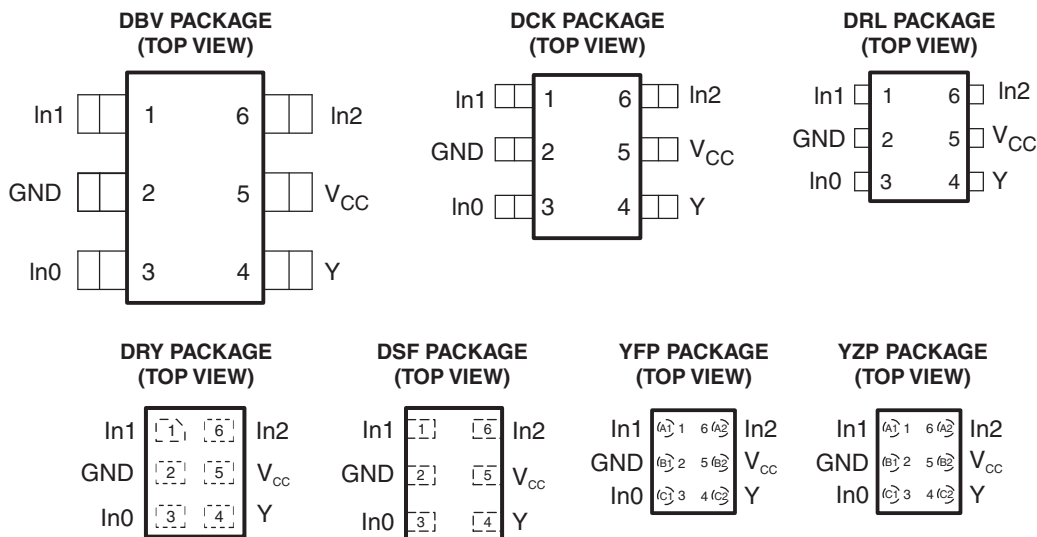


## LOW-POWER CONFIGURABLE MULTIPLE-FUNCTION GATE

Check for Samples: [SN74AUP1G58](#)

### FEATURES

- Available in the Texas Instruments NanoStar™ Packages
- Low Static-Power Consumption ( $I_{CC} = 0.9 \mu A$  Max)
- Low Dynamic-Power Consumption ( $C_{pd} = 4.6$  pF Typ at 3.3 V)
- Low Input Capacitance ( $C_i = 1.5$  pF Typ)
- Low Noise – Overshoot and Undershoot <10% of  $V_{CC}$
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Includes Schmitt-Trigger Inputs
- Wide Operating  $V_{CC}$  Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 5.5$  ns Max at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

### DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire  $V_{CC}$  range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity, which produces very low undershoot and overshoot characteristics.

The SN74AUP1G58 features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions AND, OR, NAND, NOR, XNOR, inverter, and noninverter. All inputs can be connected to  $V_{CC}$  or GND.

The device functions as an independent gate with Schmitt-trigger inputs, which allow for slow input transition and better switching noise immunity at the input.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**ORDERING INFORMATION<sup>(1)</sup>**

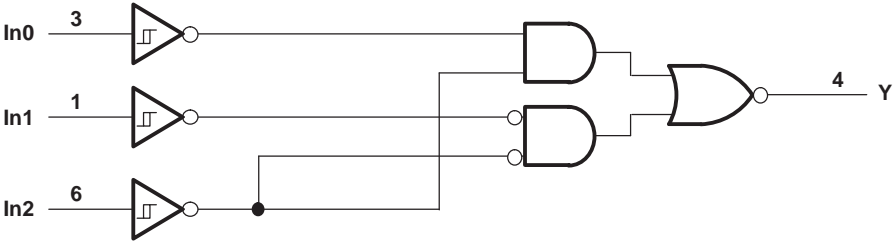
$T_A$	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(3)</sup>
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YFP (Pb-free)	Reel of 3000	SN74AUP1G58YFPR	_ _ _HJ_
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUP1G58YZPR	_ _ _HJ_
	QFN – DRY	Reel of 5000	SN74AUP1G58DRYR	HJ
	uQFN – DSF	Reel of 5000	SN74AUP1G58DSFR	HJ
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1G58DBVR	H58_
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1G58DCKR	HJ_
	SOT (SOT-553) – DRL	Reel of 4000	SN74AUP1G58DRLR	HJ_

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).
- (3) DBV/DCK/DRL: The actual top-side marking has one additional character that designates the wafer fab/assembly site.  
YFP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

**FUNCTION TABLE**

INPUTS			OUTPUT Y
In2	In1	In0	
L	L	L	L
L	L	H	H
L	H	L	L
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	L
H	H	H	L

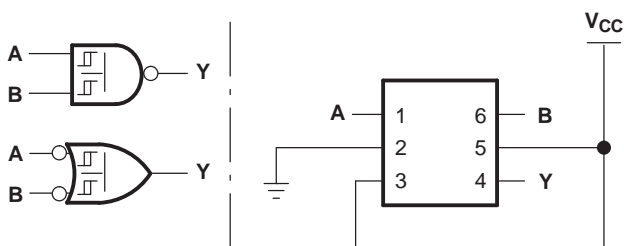
**LOGIC DIAGRAM (POSITIVE LOGIC)**



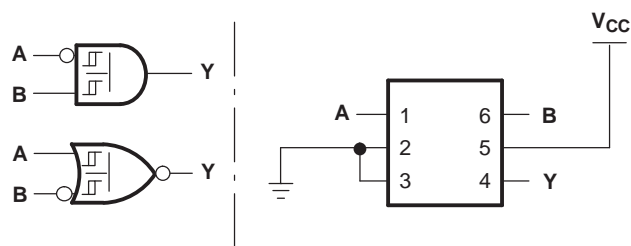
### FUNCTION SELECTION TABLE

LOGIC FUNCTION	FIGURE NO.
2-input AND with inverted input	2, 3
2-input NAND	1
2-input NAND with both inputs inverted	4
2-input OR	4
2-input OR with both inputs inverted	1
2-input NOR with inverted input	2, 3
2-input XOR	5

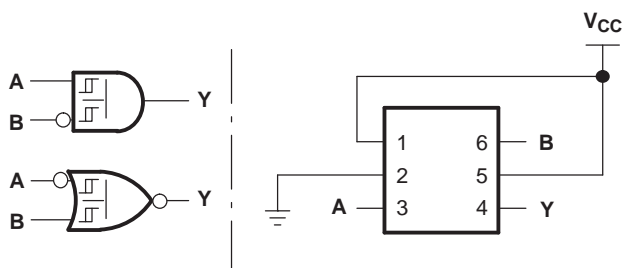
### LOGIC CONFIGURATIONS



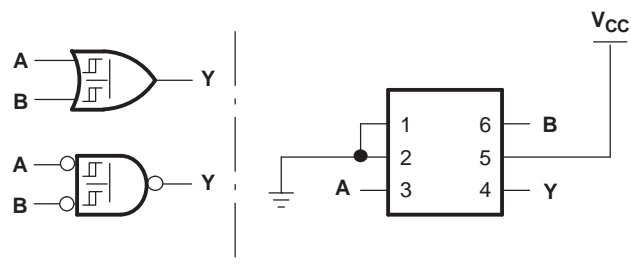
**Figure 1. 2-Input NAND Gate**



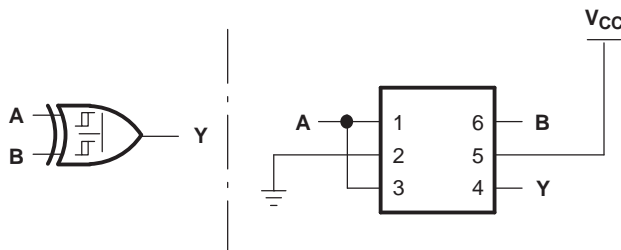
**Figure 2. 2-Input AND Gate With Inverted A Input**



**Figure 3. 2-Input AND Gate With Inverted B Input**



**Figure 4. 2-Input OR Gate**



**Figure 5. 2-Input XOR Gate**

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		–0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>		–0.5	4.6	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>		–0.5	4.6	V
$V_O$	Output voltage range in the high or low state <sup>(2)</sup>		–0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$		–50	mA
$I_{OK}$	Output clamp current	$V_O < 0$		–50	mA
$I_O$	Continuous output current			±20	mA
	Continuous current through $V_{CC}$ or GND			±50	mA
$\theta_{JA}$	Package thermal impedance <sup>(3)</sup>	DBV package		165	°C/W
		DCK package		259	
		DRL package		142	
		DSF package		300	
		DRY package		234	
		YFP/YZP package		123	
$T_{stg}$	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		0.8	3.6	V
$V_I$	Input voltage		0	3.6	V
$V_O$	Output voltage		0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 0.8\text{ V}$		–20	μA
		$V_{CC} = 1.1\text{ V}$		–1.1	mA
		$V_{CC} = 1.4\text{ V}$		–1.7	
		$V_{CC} = 1.65\text{ V}$		–1.9	
		$V_{CC} = 2.3\text{ V}$		–3.1	
		$V_{CC} = 3\text{ V}$		–4	
$I_{OL}$	Low-level output current	$V_{CC} = 0.8\text{ V}$		20	μA
		$V_{CC} = 1.1\text{ V}$		1.1	mA
		$V_{CC} = 1.4\text{ V}$		1.7	
		$V_{CC} = 1.65\text{ V}$		1.9	
		$V_{CC} = 2.3\text{ V}$		3.1	
		$V_{CC} = 3\text{ V}$		4	
$T_A$	Operating free-air temperature		–40	85	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARMETER		TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C		T <sub>A</sub> = –40°C to 85°C		UNIT	
				MIN	TYP	MAX	MIN		MAX
V <sub>T+</sub>  Positive-going input threshold voltage			0.8 V	0.3		0.6	0.3	0.6	V
			1.1 V	0.53		0.9	0.53	0.9	
			1.4 V	0.74		1.11	0.74	1.11	
			1.65 V	0.91		1.29	0.91	1.29	
			2.3 V	1.37		1.77	1.37	1.77	
			3 V	1.88		2.29	1.88	2.29	
V <sub>T–</sub>  Negative-going input threshold voltage			0.8 V	0.1		0.6	0.1	0.6	V
			1.1 V	0.26		0.65	0.26	0.65	
			1.4 V	0.39		0.75	0.39	0.75	
			1.65 V	0.47		0.84	0.47	0.84	
			2.3 V	0.69		1.04	0.69	1.04	
			3 V	0.88		1.24	0.88	1.24	
ΔV <sub>T</sub>  Hysteresis (V <sub>T+</sub> – V <sub>T–</sub> )			0.8 V	0.07		0.5	0.07	0.5	V
			1.1 V	0.08		0.46	0.08	0.46	
			1.4 V	0.18		0.56	0.18	0.56	
			1.65 V	0.27		0.66	0.27	0.66	
			2.3 V	0.53		0.92	0.53	0.92	
			3 V	0.79		1.31	0.79	1.31	
V <sub>OH</sub>	I <sub>OH</sub> = –20 μA I <sub>OH</sub> = –1.1 mA I <sub>OH</sub> = –1.7 mA I <sub>OH</sub> = –1.9 mA I <sub>OH</sub> = –2.3 mA I <sub>OH</sub> = –3.1 mA I <sub>OH</sub> = –2.7 mA I <sub>OH</sub> = –4 mA	0.8 V to 3.6 V	V <sub>CC</sub> – 0.1		V <sub>CC</sub> – 0.1		V		
		1.1 V	0.75 × V <sub>CC</sub>		0.7 × V <sub>CC</sub>				
		1.4 V	1.11		1.03				
		1.65 V	1.32		1.3				
		2.3 V	2.05		1.97				
			1.9		1.85				
		3 V	2.72		2.67				
			2.6		2.55				
V <sub>OL</sub>	I <sub>OL</sub> = 20 μA I <sub>OL</sub> = 1.1 mA I <sub>OL</sub> = 1.7 mA I <sub>OL</sub> = 1.9 mA I <sub>OL</sub> = 2.3 mA I <sub>OL</sub> = 3.1 mA I <sub>OL</sub> = 2.7 mA I <sub>OL</sub> = 4 mA	0.8 V to 3.6 V	0.1		0.1		V		
		1.1 V	0.3 × V <sub>CC</sub>		0.3 × V <sub>CC</sub>				
		1.4 V	0.31		0.37				
		1.65 V	0.31		0.35				
		2.3 V	0.31		0.33				
			0.44		0.45				
		3 V	0.31		0.33				
			0.44		0.45				
I <sub>I</sub>	All inputs	V <sub>I</sub> = GND to 3.6 V	0 V to 3.6 V	0.1		0.5	μA		
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	0 V	0.2		0.6	μA		
ΔI <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	0 V to 0.2 V	0.2		0.6	μA		
I <sub>CC</sub>		V <sub>I</sub> = GND or (V <sub>CC</sub> to 3.6 V), I <sub>O</sub> = 0	0.8 V to 3.6 V	0.5		0.9	μA		
ΔI <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> – 0.6 V <sup>(1)</sup> , I <sub>O</sub> = 0	3.3 V	40		50	μA		
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V	1.5				pF		
		3.6 V	1.5						
C <sub>o</sub>	V <sub>O</sub> = GND	0 V	3				pF		

(1) One input at V<sub>CC</sub> – 0.6 V, other inputs at V<sub>CC</sub> or GND.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $C_L = 5$  pF (unless otherwise noted) (see [Figure 6](#) and [Figure 7](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	In0, In1, or In2	Y	0.8 V		23.6				ns
			1.2 V $\pm$ 0.1 V	2.8	9.4	13.8	2.3	17.4	
			1.5 V $\pm$ 0.1 V	2.1	6.5	9.2	1.6	11.3	
			1.8 V $\pm$ 0.15 V	1.5	5.4	7.4	1	9	
			2.5 V $\pm$ 0.2 V	1.1	4	5.6	0.6	6.6	
			3.3 V $\pm$ 0.3 V	1	3.2	4.6	0.5	5.5	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $C_L = 10$  pF (unless otherwise noted) (see [Figure 6](#) and [Figure 7](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	In0, In1, or In2	Y	0.8 V		26.4				ns
			1.2 V $\pm$ 0.1 V	3.2	10.7	15.2	2.7	19	
			1.5 V $\pm$ 0.1 V	2	7.5	10.5	1.5	12.5	
			1.8 V $\pm$ 0.15 V	1.1	6.2	8.4	0.6	10.2	
			2.5 V $\pm$ 0.2 V	1	4.6	6.4	0.5	7.6	
			3.3 V $\pm$ 0.3 V	1	3.7	5.3	0.5	6.3	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $C_L = 15$  pF (unless otherwise noted) (see [Figure 6](#) and [Figure 7](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	In0, In1, or In2	Y	0.8 V		29.6				ns
			1.2 V $\pm$ 0.1 V	3.8	11.8	16.8	3.3	21.1	
			1.5 V $\pm$ 0.1 V	2.9	8.3	11.6	2.4	13.8	
			1.8 V $\pm$ 0.15 V	2.2	6.8	9.3	1.7	11.3	
			2.5 V $\pm$ 0.2 V	1.7	5.1	7	1.2	8.4	
			3.3 V $\pm$ 0.3 V	1.4	4.2	5.9	0.9	7	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $C_L = 30$  pF (unless otherwise noted) (see [Figure 6](#) and [Figure 7](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	In0, In1, or In2	Y	0.8 V		38.1				ns
			1.2 V $\pm$ 0.1 V	5.1	15	21.4	4.6	26.6	
			1.5 V $\pm$ 0.1 V	4	10.6	14.6	3.5	17.4	
			1.8 V $\pm$ 0.15 V	3.2	8.7	11.7	2.7	14.2	
			2.5 V $\pm$ 0.2 V	2.5	6.5	8.7	2	10.5	
			3.3 V $\pm$ 0.3 V	2.1	5.4	7.3	1.6	8.7	

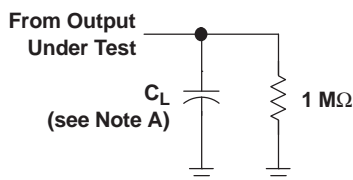
## OPERATING CHARACTERISTICS

 $T_A = 25^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$f = 10\text{ MHz}$	0.8 V	4	pF
			$1.2\text{ V} \pm 0.1\text{ V}$	4	
			$1.5\text{ V} \pm 0.1\text{ V}$	4	
			$1.8\text{ V} \pm 0.15\text{ V}$	4	
			$2.5\text{ V} \pm 0.2\text{ V}$	4.3	
			$3.3\text{ V} \pm 0.3\text{ V}$	4.6	

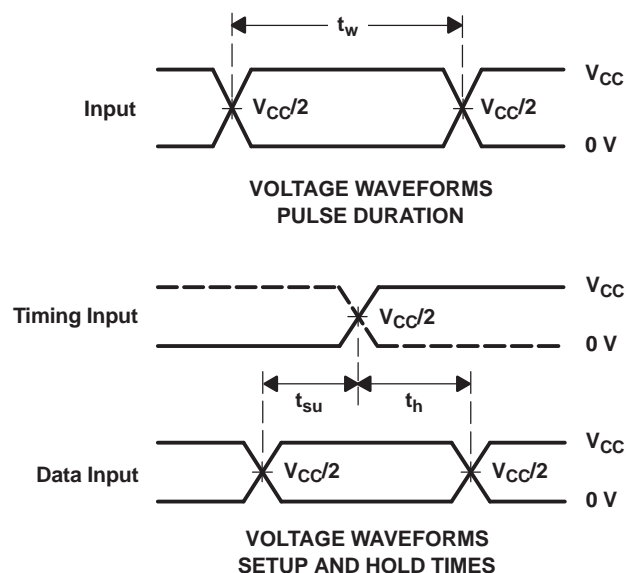
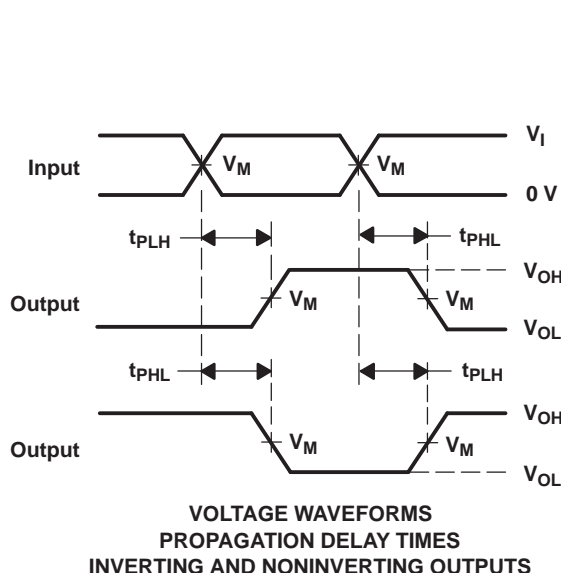
## PARAMETER MEASUREMENT INFORMATION

### (Propagation Delays, Setup-and-Hold Times, and Pulse Duration)



LOAD CIRCUIT

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_M$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
$V_I$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$

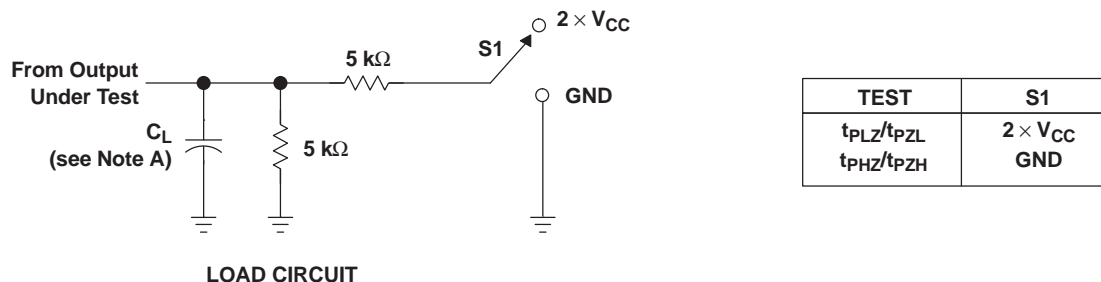


- NOTES:
- $C_L$  includes probe and jig capacitance.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10$  MHz,  $Z_O = 50 \Omega$ , slew rate  $\geq 1$  V/ns.
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

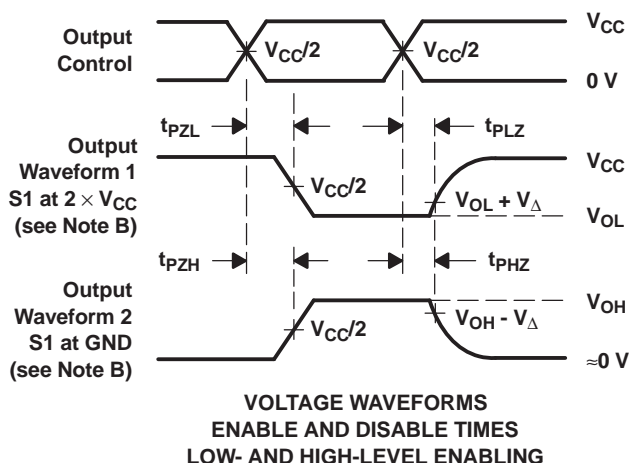
Figure 6. Load Circuit and Voltage Waveforms



## PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_M$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
$V_I$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$
$V_{\Delta}$	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ , slew rate  $\geq 1 \text{ V/ns}$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 7. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1G58DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H58R	<a href="#">Samples</a>
SN74AUP1G58DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H58R	<a href="#">Samples</a>
SN74AUP1G58DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HJR	<a href="#">Samples</a>
SN74AUP1G58DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HJR	<a href="#">Samples</a>
SN74AUP1G58DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HJR	<a href="#">Samples</a>
SN74AUP1G58DRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HJ7 ~ HJR)	<a href="#">Samples</a>
SN74AUP1G58DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HJ	<a href="#">Samples</a>
SN74AUP1G58DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HJ	<a href="#">Samples</a>
SN74AUP1G58YFPR	ACTIVE	DSBGA	YFP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		(HJ2 ~ HJ7 ~ HJN)	<a href="#">Samples</a>
SN74AUP1G58YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(HJ2 ~ HJ7 ~ HJN)	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G58DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G58DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G58DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AUP1G58DCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AUP1G58DRLR	SOT	DRL	6	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74AUP1G58DRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G58DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G58DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G58YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1G58YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

## TAPE AND REEL BOX DIMENSIONS

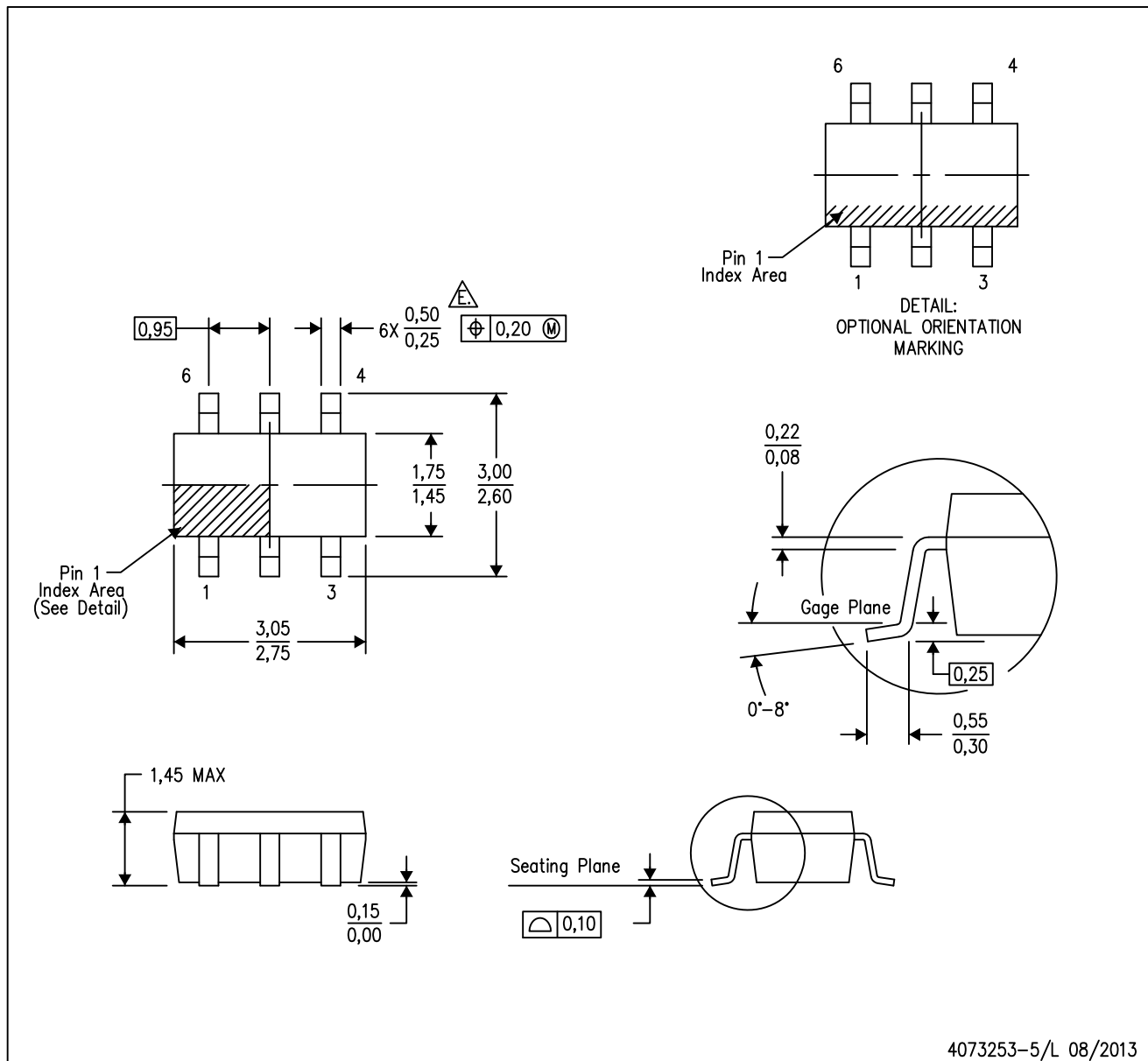


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G58DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74AUP1G58DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74AUP1G58DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74AUP1G58DCKT	SC70	DCK	6	250	202.0	201.0	28.0
SN74AUP1G58DRLR	SOT	DRL	6	4000	184.0	184.0	19.0
SN74AUP1G58DRLR	SOT	DRL	6	4000	202.0	201.0	28.0
SN74AUP1G58DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G58DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP1G58YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1G58YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

DBV (R-PDSO-G6)

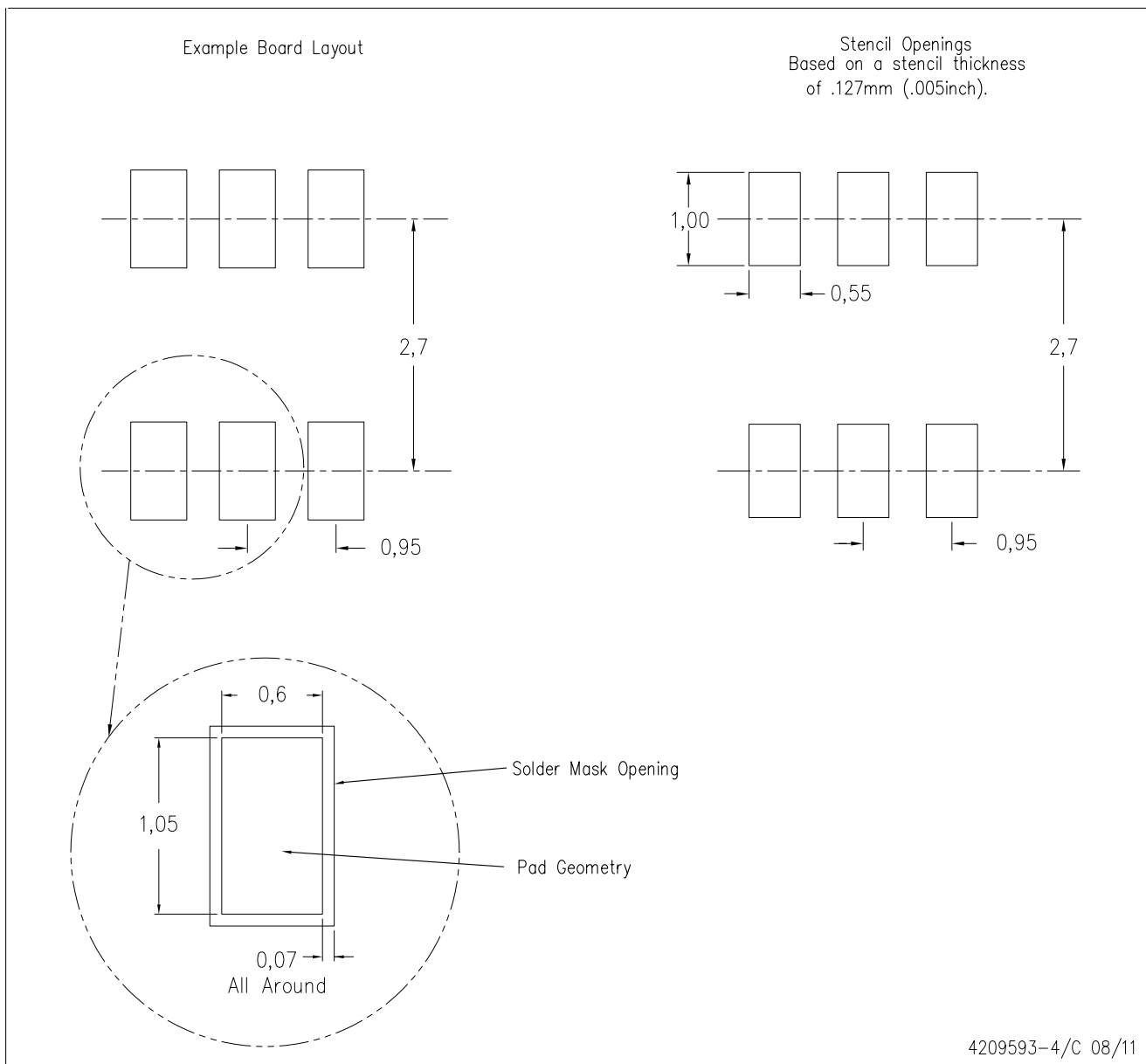
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
  - $\Delta$  Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

## DCK (R-PDSO-G6)

## PLASTIC SMALL-OUTLINE PACKAGE

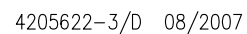


4093553-4/G 01/2007


- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - Falls within JEDEC MO-203 variation AB.



## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
-  C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
- D. JEDEC package registration is pending.

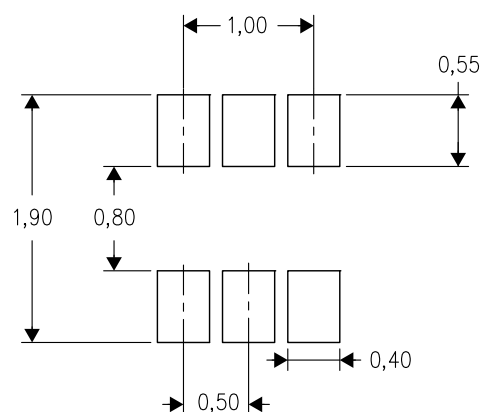
DRL (R-PDSO-N6)

PLASTIC SMALL OUTLINE

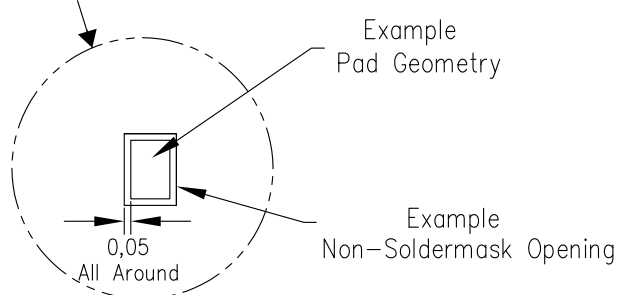
Example Board Layout



Example Stencil Design  
(Note E)



Example  
Non-Soldermask Defined Pad



Example  
Pad Geometry



Example  
Non-Soldermask Opening

4208207-3/E 06/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



4207181/F 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. SON (Small Outline No-Lead) package configuration.
  -  D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
  - E. This package complies to JEDEC MO-287 variation UFAD.
  -  F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R-PUSON-N6)

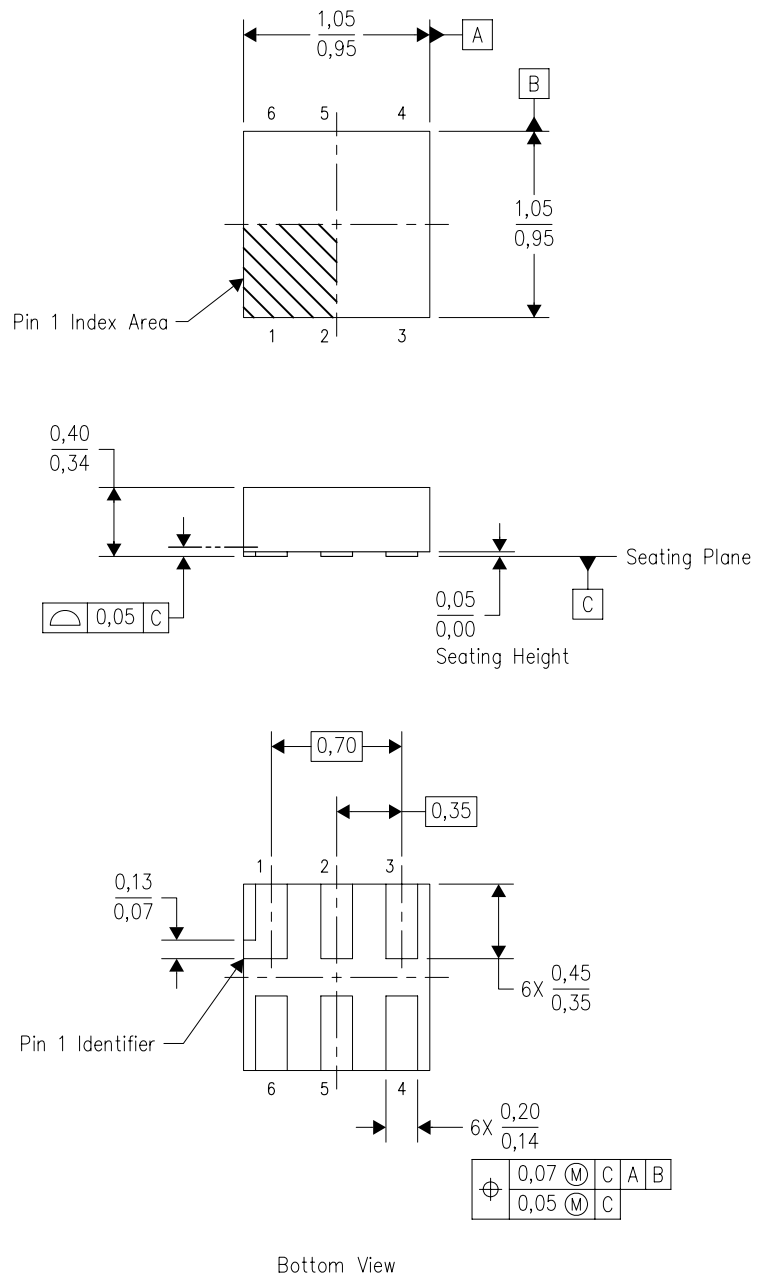
PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4208186/E 03/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - SON (Small Outline No-Lead) package configuration.
  - This package complies to JEDEC MO-287 variation X2AAF.

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

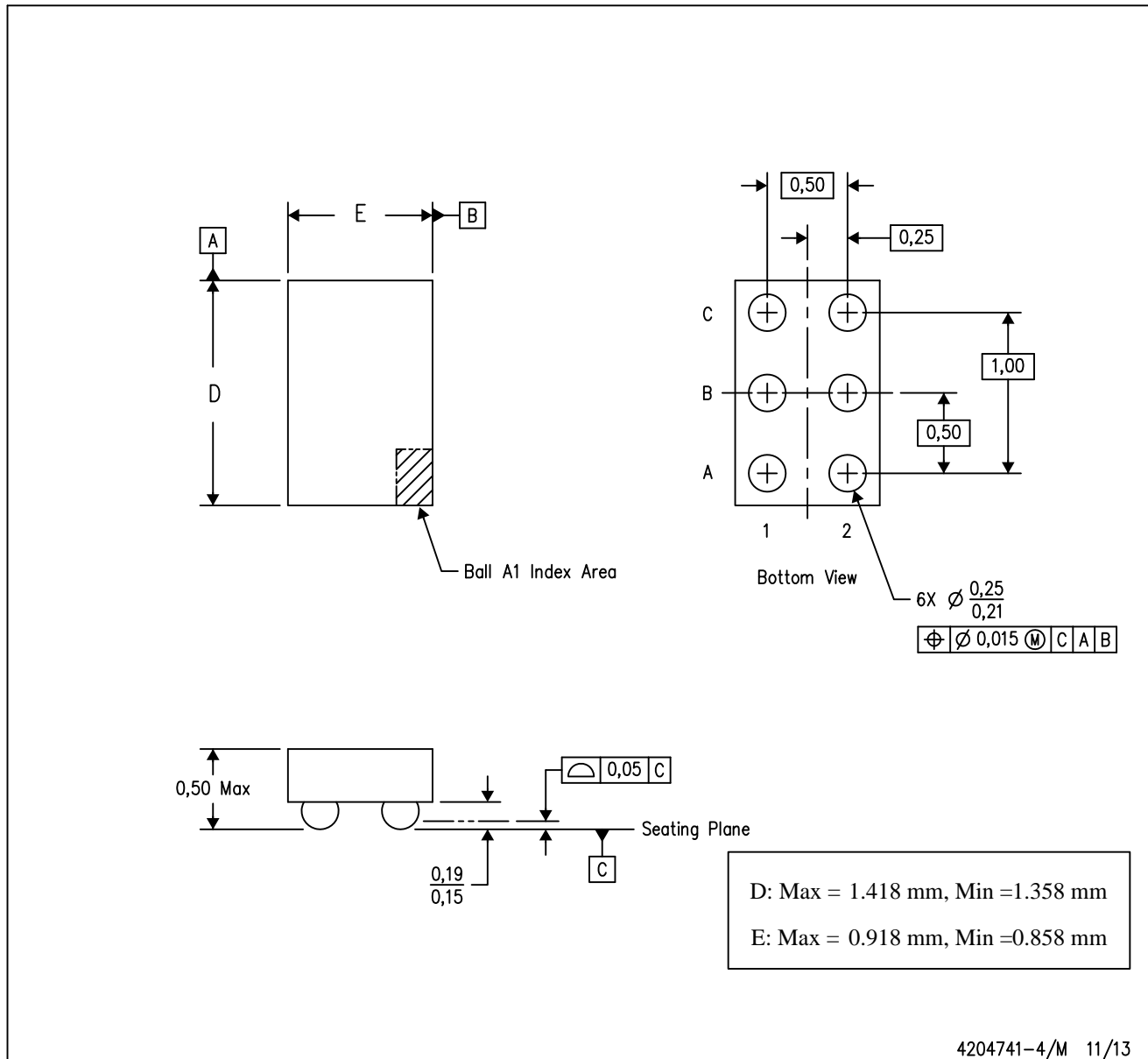


4210277/D 05/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
  - E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
  - H. Component placement force should be minimized to prevent excessive paste block deformation.

YZP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY

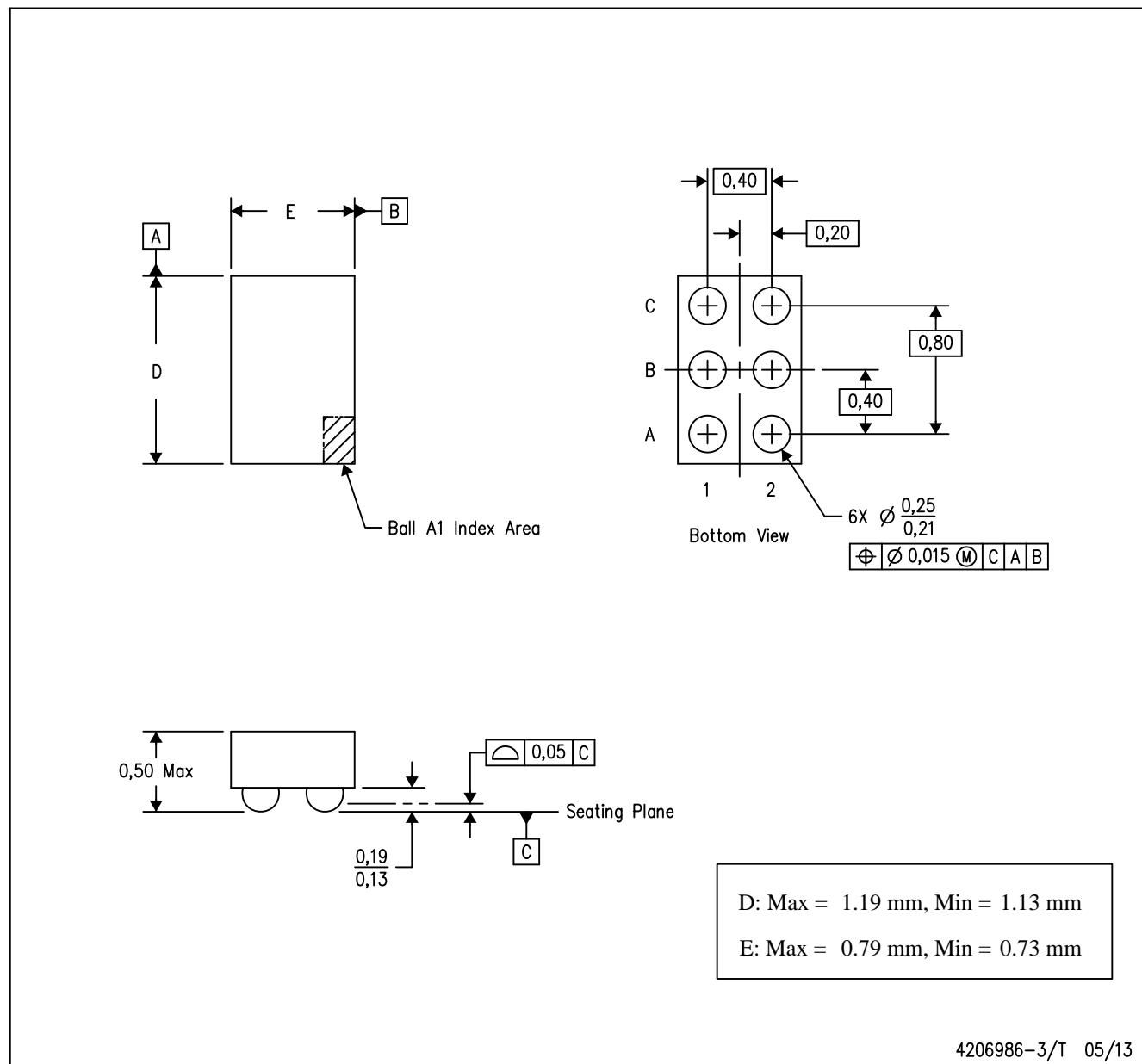


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

YFP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.



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