

AD9520-x Evaluation Board

FEATURES

- Simple power connection using 6 V wall adapter and on-board LDO voltage regulators
- LDOs are easily bypassed for power measurements
- 5 ac-coupled differential LVPECL SMA connectors
- 7 LVPECL differential headers for additional outputs
- SMA connectors for
 - 2 reference inputs
 - Charge pump output
 - Clock distribution input
- USB connection to PC
- Microsoft Windows-based evaluation software with simple graphical user interface
- On-board PLL loop filter
- Easy access to digital I/O and diagnostic signals via I/O header
- Status LEDs for diagnostic signals

APPLICATIONS

- Clocking of analog-to-digital and digital-to-analog converters up to 2.9 GHz
- Networking and communications line cards
- Test and measurement equipment
- Wireless base stations, controllers
- Clock cleanup/jitter attenuation
- Clock distribution

GENERAL DESCRIPTION

The AD9520-x (hereafter referred to as [AD9520](#)) is a very low noise PLL clock synthesizer featuring an integrated VCO, clock dividers, and up to 24 outputs. The AD9520 features automatic holdover and a flexible reference input circuit allowing for very smooth reference clock switching. The AD9520 family also features the necessary provisions for an external VCXO.

The AD9520 evaluation board is a compact, easy-to-use platform for evaluating all features of the AD9520. This user guide covers all six versions of the AD9520 family.

Although the Quick Start Guide to the AD9520 PLL section applies specifically to the AD9520-4, increasing the N (feedback) divider and channel divider increases the VCO frequency to the allowable frequency range of other AD9520 versions.

For the AD9520-5, which lacks the internal VCO, certain portions of this user guide that apply to the internal VCO (such as VCO calibration) can be ignored.

This document covers the AD9520 family. The [AD9522](#) family, which is identical to the AD9520 except that it has LVDS outputs, is covered in UG-077.

For convenience, detailed information from the AD9520 data sheet has been included here. Use this user guide in conjunction with the AD9520 and AD9522 data sheet and software documentation available at www.analog.com.

AD9520 EVALUATION BOARD

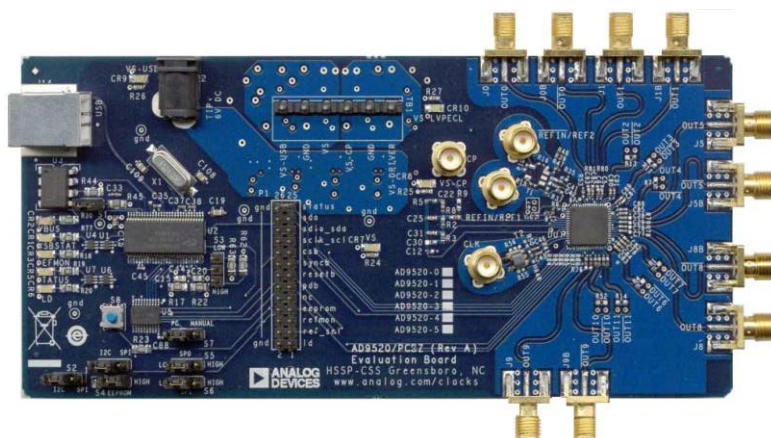


Figure 1.

08746-001

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REVISION HISTORY

1/10—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The following instructions are for setting up the physical connections to the AD9520 evaluation board.

When connecting the evaluation board to a PC for the first time, the user must install the evaluation software prior to connecting the evaluation board.

POWER AND PC CONNECTIONS

1. Install AD9520 evaluation software. Administrative privileges are required for installation. The 64-bit versions of Windows® are not supported.
2. Connect the wall power supply to the main power connector labeled P2. The following five LEDs should be on: CR1 (USBSTAT), CR7 (VS), CR8 (VS-CP), CR9 (VS_USB), and CR10 (VS_LVPECL).
3. Connect the USB cables to the evaluation board and the computer. The red LED labeled CR2 (VBUS) on the AD9520 evaluation board should illuminate and the CR1 (USBSTAT) LED should start blinking.
4. If the **Found New Hardware Wizard** window automatically appears when the evaluation board is connected, select **Install the software automatically** and click **Next**.
The **Found New Hardware Wizard** window may appear twice, and a system restart may be required.

Refer to the Evaluation Board Software section for details on running the AD9520 evaluation board software.

If the USBSTAT LED is not blinking, ensure that:

- Jumpers are installed on Position S1 and on the SPI position of S2.
- The jumper on S4 is across the center pin and the minus symbol.
- The USB port on the PC is operational and that the USB cable is not damaged.

SIGNAL CONNECTIONS

To connect signals, connect a signal generator to the J10 SMA connector. By default, the reference inputs on this evaluation board are ac-coupled and terminated 50 Ω to ground. An amplitude setting of 0 dBm to 6 dBm is fine.

If the user wishes to connect a signal to REF2, connect that signal to the J13 SMA connector. DC-coupling is recommended in applications requiring automatic hitless reference switching. There is a possibility that the AD9520 receive buffer can chatter when an ac-coupled clock stops toggling.

Connect an oscilloscope, spectrum analyzer, or other lab equipment to any of the J0 to J9 SMA connectors on the right side of the board.

OUT0 through OUT8 are ac-coupled LVPECL outputs. OUT9 through OUT11 are dc-coupled and have no output termination. These are intended to allow the user to evaluate the AD9520 output driver in CMOS mode. To use OUT9 through OUT11 in LVPECL mode, replace the 0 Ω resistors with 0.1 μ F capacitors, and install 200 Ω pull-down resistors.

BYPASSING THE WALL POWER SUPPLY

To bypass the wall power supply, remove the following ferrite beads (on the backside of the board) : F7, F4, F2, and F6. Next, connect a bench power supply to TB1 on the evaluation board. This is useful for making AD9520 power consumption measurements.

BYPASSING THE PLL (CLOCK DISTRIBUTION ONLY)

To bypass the PLL, connect a signal generator to the SMA connector labeled CLK. By default, this connection is ac-coupled to the CLK pin, and terminated with 50 Ω to ground. Refer to the Evaluation Software Components section for details on running the AD9520 evaluation board software.

USING AN EXTERNAL VCXO

To use an external VCXO,

1. Install a 0 Ω resistor at R9 and remove R8.
2. Connect a loop filter and external VCO/VCXO input to J12.
3. Connect the external VCO/VCXO output to the J11 SMA connector (CLK input).

USING I²C SERIAL PORT MODE

To use I²C serial port mode,

1. Move Jumper S2 to the center and left (I²C) pins.
2. Move Jumper W1 to the center and left (I²C) pins.
3. Select the desired I²C address using Jumper S5 and Jumper S6. Note that S5 = S6 = high is reserved for SPI mode.
4. On the evaluation software, select **Configure Serial Port** from the **I/O** menu (see Figure 24).
5. Click **Reset Serial Port**, and then click **Detect Current Configuration**. A dialog box appears and acknowledges the I²C mode and address.

EVALUATION BOARD SOFTWARE

Use the following instructions to set up the AD9520 evaluation board software.

SOFTWARE INSTALLATION

Do not connect the evaluation board until the software installation is complete.

1. The latest evaluation software and documentation can be downloaded from www.analog.com.
2. If the software was downloaded, skip to Step 3. If using the CD, insert the AD9520 evaluation software CD. Double-click **My Computer**, and then double-click the **AD9520EV CD** icon. A window opens showing the contents of the CD divided into four sections: **Datasheet**, **Layout**, **Schematic**, and **Software**. The file named **readme.txt** contains a description of the CD contents and may contain additional as well as any last minute instructions or information. Double-click the **Software** folder.
3. Double-click **AD9520Eval_Setup1.1.0.exe**. (Note that the website may have a newer version.) Follow the installation instructions. The default installation location for the evaluation software is: **C:\Program Files\Analog Devices\AD9520 Eval Software**.

RUNNING THE SOFTWARE

Power up and connect the evaluation board to the PC. See the Evaluation Board Hardware section for details on the various connectors on the evaluation board.

1. Double-click **AD9520 Eval Software** to run the AD9520 evaluation software. Depending on whether the evaluation board was found by the software, either light blue text appears in a pop-up window indicating that the evaluation board was found, or red text appears indicating that the evaluation board was not found.
2. If the evaluation board is found, click anywhere in the pop-up window with the **Evaluation Software Ready**, and the main window for the software appears. Proceed to the Evaluation Software Components section for details about running the software.
If the evaluation board is not found, a dialog box appears allowing you to select which AD9520 evaluation board is connected while the software runs in standalone mode. Standalone mode is useful for viewing and generating register setup files.

See the Evaluation Board Hardware section for connecting the evaluation board. Alternatively, you can use the software in standalone mode, and specify which version of the AD9520 will be used. The standalone mode is useful for verifying register settings for a given PLL setup.

If the evaluation board is connected while the evaluation software is running, the window in Figure 2 appears to prompt you to load the evaluation board with the evaluation software settings or read the evaluation board with the evaluation software settings.

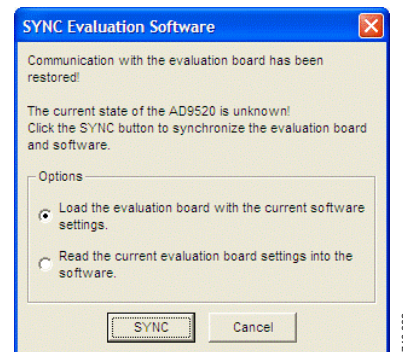


Figure 2. SYNC Evaluation Software Window

If the evaluation board was not automatically detected when it was connected, you can also select the **Select Evaluation Board** option from the **I/O** menu (see Figure 24), and select **Ezssp-0**, **Ezssp-1**, or **Ezssp-2**.

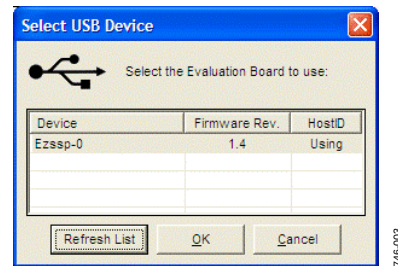


Figure 3. Select USB Device Window

See the Evaluation Software Components section for a description of the evaluation software features, or the Quick Start Guide to the AD9520 PLL section for details on the individual blocks of the AD9520.

QUICK START GUIDE TO THE AD9520 PLL

When the evaluation software is installed, the evaluation board is connected, and the software is loaded, use the following steps to configure and lock the PLL. These steps assume that the input signal is present, the evaluation board has not been modified, and that the PLL loop filter is suitable for the user's application.

This quick start guide covers only simple PLL operation to start the PLL. See the AD9520 data sheet and Evaluation Software Components section for a detailed explanation of the various AD9520 features.

The following case is an example for the AD9520-4 using the values in Table 1.

Table 1.

Parameter	Value
Input Frequency	19.44 MHz on REF1
Output Frequency	148.5 MHz
Reference Divider	72
Phase Detector Frequency	270 kHz
Feedback Divider	5500
VCO Frequency	1485 MHz
VCO Divider	2
Channel Divider	5

1. Turn the PLL on by selecting **Normal Op** from the **PLL MODE** box found at the top of the main window (see Figure 8).
2. Enter the intended reference input frequency (in megahertz) in the **REF 1 (MHz)** box at the upper left corner of the main window.
3. Click the triangular buffer symbol immediately to the right of the input reference frequency (see Figure 4) text boxes to load the **Reference Input Control** window shown in Figure 5. Turn the REF1 reference input buffer on by selecting the **Enable REF 1** check box, and then click **OK**.

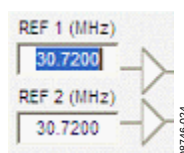


Figure 4. Buffer Symbol

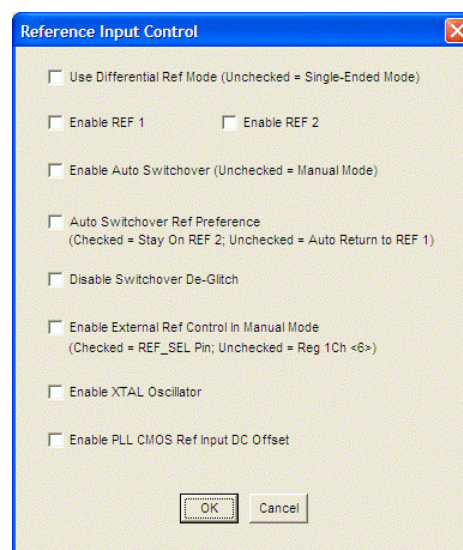


Figure 5. Reference Input Control Window

4. When the window closes, the **WRITE** button under the **REGISTER W/R** section in Figure 8 blinks red. This indicates that there are settings that have not been loaded to the AD9520 evaluation board. Click the blinking red **WRITE** button to load these settings to the evaluation board.
5. Select the VCO as the input to the clock distribution circuitry by clicking the mux symbol that is located immediately to the right of the **VCO (MHz)** box (see Figure 6).

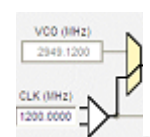


Figure 6. Buffer Symbol

When the VCO is selected, the border of the **VCO (MHz)** box changes from gray to black. The current VCO frequency is shown in the **VCO (MHz)** box.

6. Program the R (reference) divider by clicking the **R DIVIDER** box at the top of the main window. Set the desired value and click **OK** (see Figure 13).
7. Program the N (feedback) divider by clicking the **N DIVIDER** box at the top of the main window. Set the desired value and click **OK**. For this example, N = 5500 can use 8/9 dual modulus mode with A = 4 and B = 687.
8. Set the charge pump current (1.2 mA in this case) by clicking the **CHARGE PUMP** box in the upper right corner of the main window, and click **OK**.
9. Note that if the desired configuration has the phase detector frequency above 50 MHz, an antibacklash pulse width of 1.3 ns may work better. This setting is accessed by clicking the **PFD** box to the left of the **CHARGE PUMP** box. However, this setting normally does not need to be modified.
10. Set the VCO divider by clicking the green **VCO** box in the center of the main window immediately to the left of the **Cal VCO** button.

11. Power down unused drivers by clicking the numbered triangular symbol (see Figure 7) on the right side of the main window, and then clicking **Safe Power Down**.

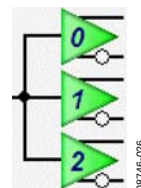


Figure 7. Driver Symbol

12. Set the channel dividers by clicking **DIVIDER 0** through **DIVIDER 3**, and entering the divider ratio.
13. Click the flashing red **WRITE** button under the **REGISTER W/R** section. This loads the desired settings to the AD9520 evaluation board.
14. Click the blinking yellow **Cal VCO** button to load the VCO calibration window. The default VCO divide ratio (16) works for all applications. Click the **Cal VCO** button in the **Calibrate VCO** window to begin calibration (see Figure 19). The PLL should now be locked and the lock detect (LD) LED on the left side of the board should be on.

EVALUATION SOFTWARE COMPONENTS

MAIN WINDOW

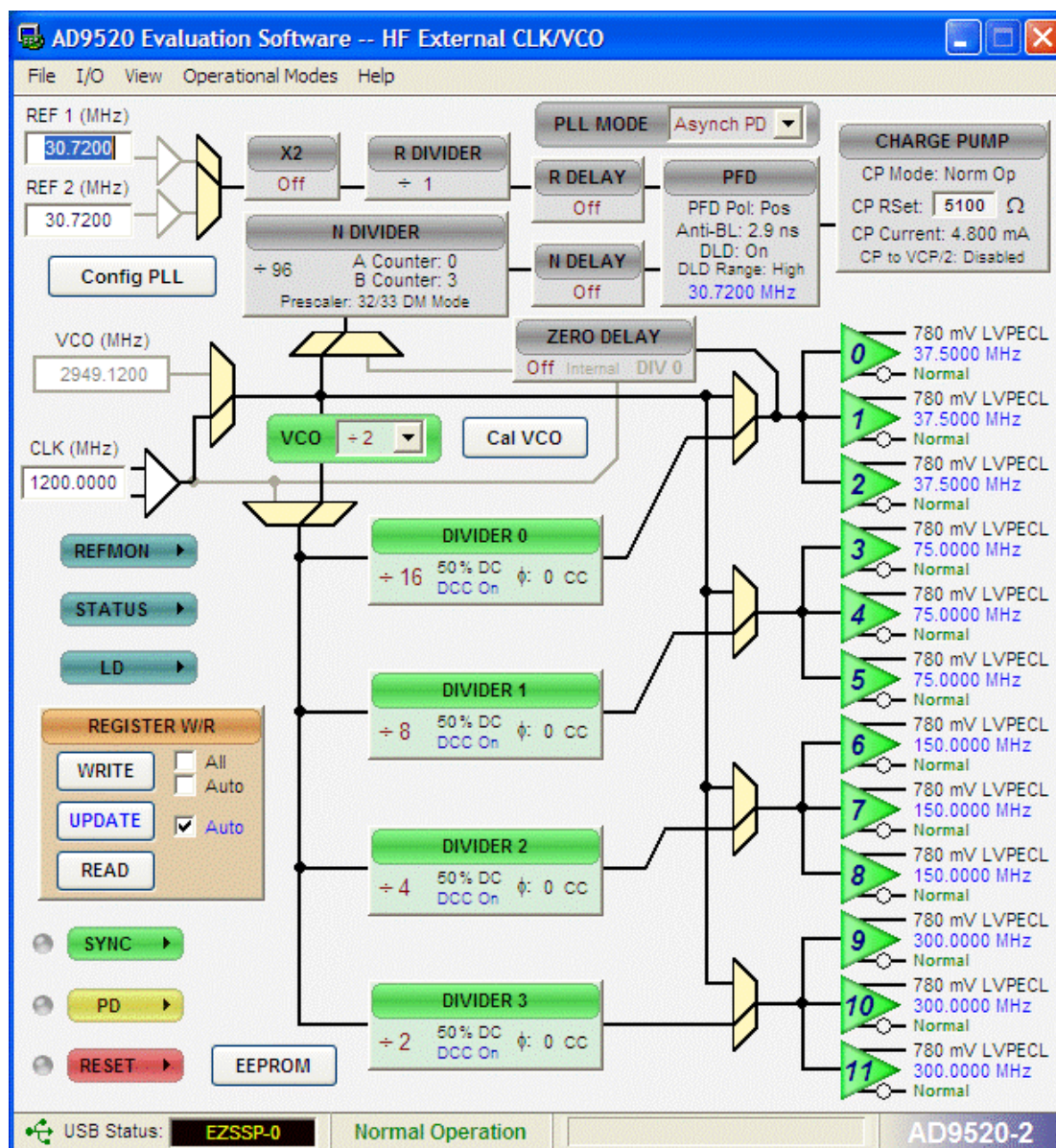


Figure 8. Evaluation Software Main Window

The AD9520 evaluation software is composed of subsections that correspond to the major functional blocks of the AD9520. These subsections are listed in the following sections, and each of these has its own window. From the main window, each functional block can be accessed by clicking that block in the main window.

When a subwindow closes after clicking **OK**, the **WRITE** box on the main window (under the **REGISTER W/R** section) may blink red. This indicates that there are settings that have not been loaded to the AD9520 evaluation board. Clicking the blinking red **WRITE** box loads these settings to the evaluation board.

PLL REFERENCE INPUT WINDOW

The **Reference Input Control** window is shown in Figure 10 and is accessed by clicking either of the triangular buffer symbols immediately to the right of the **REF 1 (MHz)** and **REF 2 (MHz)** input reference frequency boxes (see Figure 9).

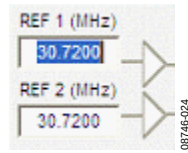


Figure 9. Buffer Symbol

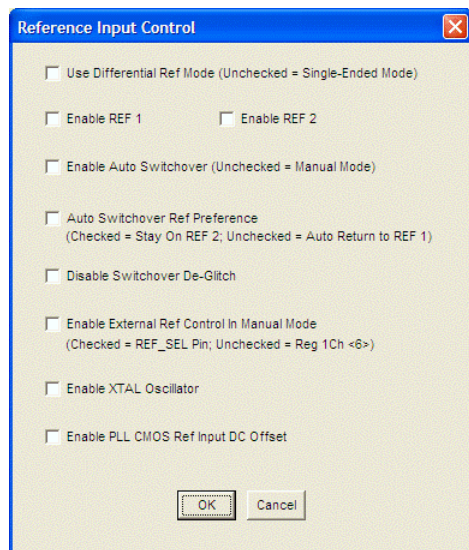


Figure 10. Reference Input Control Window

This window is used to enable the PLL reference inputs, which are powered down by default.

Select **Enable REF 1**, or **Enable REF 2**, or both to enable the appropriate reference input and click **OK** when finished. If a differential input is used, select the **Use Differential Ref Mode (Unchecked = Single-Ended Mode)** check box. Note that this mode should not be used simultaneously with **Enable REF 1** or **Enable REF 2**.

The remaining six check boxes control the reference switchover modes. If **Disable Switchover De-Glitch** is activated, the AD9520 maintains the phase relationship between the active input and PLL output during a reference switchover. Otherwise, the AD9520 minimizes the phase disturbance at the output during a reference switchover.

Check **Enable XTAL Oscillator** if you intend to connect a crystal to the reference input.

Enable PLL CMOS Ref Input DC Offset forces the dc bias point of the single-ended reference input to be different from the switching point, and is useful for preventing an ac-coupled input from chattering when the reference input is lost.

PLL CONFIGURATION WINDOW

The **PLL Configuration** window shown in Figure 11 is opened by clicking the **Config PLL** button on the main screen. The window has three sections: **SyncB Counter Reset Mode**, **PLL Status Registers**, and **Settings**.

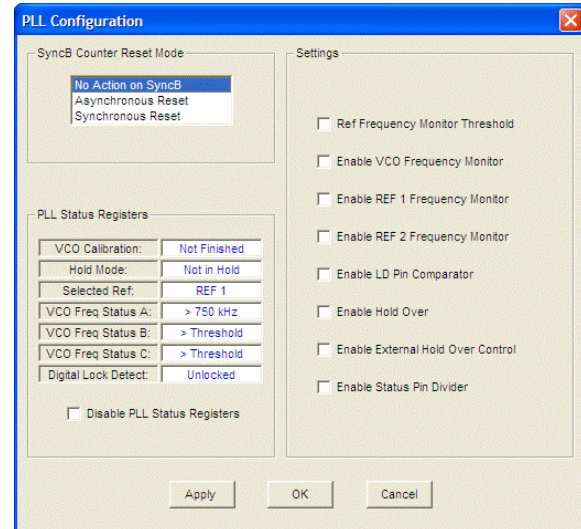


Figure 11. PLL Configuration Window

The **SyncB Counter Reset Mode** section indicates whether the R, A, and B counters are reset when the **SYNC** pin is activated, and controls R0x019[7:6]. See the AD9520 data sheet for more details.

The **PLL Status Registers** section allows you to see the current value of the read-only PLL status register, Address 0x01F. This function is very useful for ensuring that the AD9520 VCO has finished VCO calibration, and that the PLL is locked.

The **Settings** section controls the various PLL settings such as holdover. The AD9520 data sheet describes these functions in detail.

REFMON, STATUS, AND LD BUTTONS

These three blue buttons (**REFMON**, **STATUS**, and **LD**) allow you to select which signals appear at the REFMON, STATUS, and LD pins at Connector P1. Connector P1 is located in the center of the evaluation board. The pins in the left column of Connector P1 are ground pins, and the ones in the right column are signal pins.

There are many useful diagnostic signals available at these pins. The R divider output is particularly useful. In the example used in the Quick Start Guide to the AD9520 PLL section, the 80 kHz signal is visible on the STATUS pin to ensure that the reference inputs and R divider are working properly.

Dynamic signals (such as the R divider output) are primarily intended for diagnostics. These diagnostic signals may adversely affect PLL performance in critical applications if left on in normal operation.

REGISTER W/R BOX

The **REGISTER W/R** (write/read) box has three buttons and three check boxes.

The **WRITE** button transfers the values stored in the evaluation software to the evaluation board. It blinks red when register values have changed.

The **READ** button transfers the values stored in the evaluation board to the evaluation software.

The **UPDATE** button issues an I/O update command by writing 0x01 to Register 0x232.

Selecting the **All** check box transfers all of the registers when the **WRITE** button is clicked. When this box is cleared, only the registers whose value has changed are written.

Selecting the **Auto** check box adjacent to the **WRITE** box forces the evaluation software to write the register changes to the evaluation board automatically when they occur.

Selecting the **Auto** check box adjacent to the **UPDATE** box forces the evaluation software to issue an I/O update command whenever registers are written to the AD9520.

SYNC, PD (POWER DOWN), AND RESET BUTTONS

The **SYNC**, **PD**, and **RESET** buttons allow you to control the **SYNC**, **PD**, and **RESET** pins on the AD9520.

Each button has three options: **Strobe**, **Latch**, and **Release**. **Strobe** activates the pin, and then releases it. **Latch** holds the pin active until the **Release** command is issued.

EEPROM CONTROL WINDOW

The **EEPROM Control** window shown in Figure 12 is accessed by clicking the **EEPROM** button near the lower left corner of the main window.

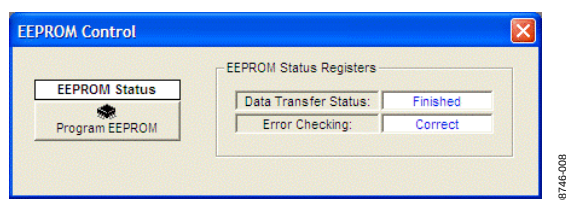


Figure 12. EEPROM Control Window

To store the current register settings of the AD9520 to the EEPROM, click the **Program EEPROM** button (see Figure 12). Check the **EEPROM Status Registers** section on the right side of the window to verify that the operation is successful.

To load the values stored in the EEPROM, ensure that the EEPROM pin is pulled high and reset the AD9520.

The EEPROM pin is pulled high by placing the S4 EEPROM jumper (located in the lower left corner of the evaluation board) across the center and right (high) pin.

You can reset the AD9520 by clicking the red **RESET** button in the lower left corner of the main window, and selecting **Strobe ResetB**.

REFERENCE (R) DIVIDER WINDOW

The R divider window shown in Figure 13 is accessed by clicking the **R DIVIDER** box in the main window. It allows you to set the reference divider. If this box is colored gray, the PLL is off. To turn the PLL on, click the **PLL MODE** box at the top of the main window, and select **Norm Op**.

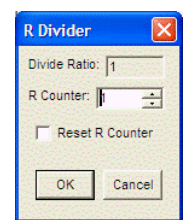


Figure 13. Reference Divider Window

This window has a check box for holding the R divider in reset. When the R divider is held in reset, the PLL loop is opened. Therefore, this feature is seldom used.

The reference input path also has a reference multiply-by-2 (labeled **X2** in the main window) check box that controls the reference clock doubler. This frequency doubler can be used to double the phase detector frequency of the PLL, and is described in detail in the AD9520 data sheet.

FEEDBACK (N) DIVIDER WINDOW

The **N Divider** window shown in Figure 14 is accessed by clicking the **N DIVIDER** box. It allows you to set the feedback divider. If this box is colored gray, the PLL is off. To turn the PLL on, click the **PLL MODE** box at the top of the main window and select **Norm Op**.

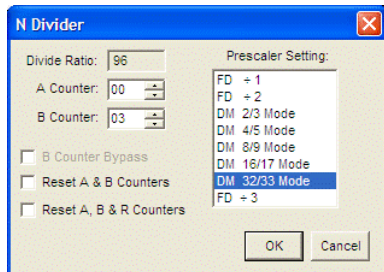


Figure 14. Reference Divider Window

The various modes of the N divider are described in detail in the AD9520 data sheet. For most applications, the 8/9 or 16/17 dual modulus modes are used. For applications requiring a divider value larger than 131119, the 32/33 mode is provided. Different applications require different settings, and you can experiment with the different settings.

The evaluation software has internal checking to ensure that invalid settings are not programmed. For example, the B counter must always be larger than the A counter. Another restriction is that 8/9 dual modulus mode cannot be used for VCO frequencies greater than 2400 MHz. In cases where a feedback divider restriction cannot be resolved, you may need to adjust the R (reference) divider to allow a different feedback divider value. For example, it is not possible to use the internal VCO, and a feedback divider of 30. However, the R divider can be doubled, which allows a feedback divider of 60.

The feedback divider window has a check box for holding the N divider in reset. When the N divider is held in reset, the PLL is open. Therefore, this feature is seldom used.

R AND N DELAY WINDOW

The N delay window shown in Figure 15 is accessed by clicking the **N DELAY** box on the main window. The **R DELAY** box is identical to the **N DELAY** box. These delay settings, which are most often used in zero delay mode, allow you to vary the static phase offset of the PLL.

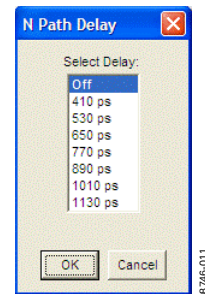


Figure 15. N Delay Window

PHASE FREQUENCY DETECTOR (PFD) WINDOW

The **Phase Frequency Detector (PFD)** window shown in Figure 16 is accessed by clicking the **PFD** box on the main screen.

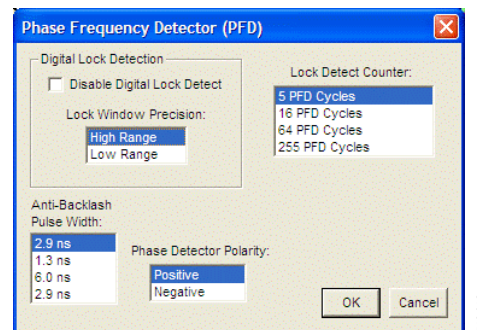


Figure 16. Phase Frequency Detector Window

The features accessible in this window are described in detail in the AD9520 data sheet. The most commonly used settings are **Anti-Backlash Pulse Width** and **Lock Detect Counter**.

For phase detector frequencies greater than 50 MHz, the PLL may work better with the 1.3 ns antbacklash pulse width setting.

Setting the **Lock Detect Counter** to values greater than 5 PFD cycles can be useful in applications where the loop bandwidth is low and the lock detect counter chatters during acquisition.

CHARGE PUMP SETUP WINDOW

The **Charge Pump Setup** window shown in Figure 17 is accessed by clicking the **CHARGE PUMP** box on the main window.

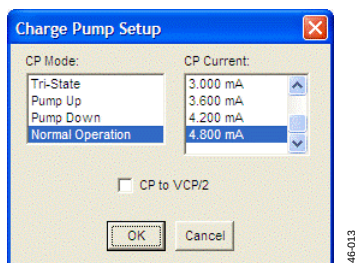


Figure 17. Charge Pump Setup Window

This window is most often used to vary the charge pump current.

The window also has a check box for setting the charge pump voltage to $V_{CP}/2$, which is very useful for debugging the PLL and isolating the output driver section of the AD9520 from the PLL section.

ZERO DELAY WINDOW

The **Zero Delay** window shown in Figure 18 is accessed by clicking the **ZERO DELAY** box on the main window.

When internal zero delay mode is selected, the window shrinks because only Divider 0 can operate in the internal zero delay mode.

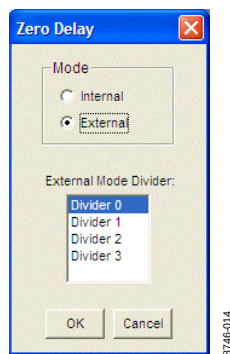


Figure 18. Zero Delay Window

VCO CALIBRATION WINDOW

The **Calibrate VCO** window shown in Figure 19 is accessed by clicking the **Cal VCO** button on the main window.

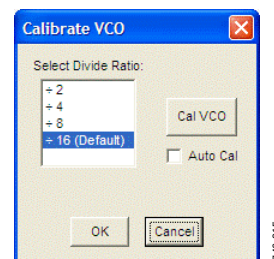


Figure 19. Calibrate VCO Window

A valid reference input signal must be present to complete VCO calibration, and the VCO must be recalibrated any time the VCO frequency changes by more than 40 MHz.

A VCO divider of 16 is suitable for all applications. However, for applications where the phase detector frequency is <12 MHz, using a smaller VCO calibration divider reduces calibration time. Refer to the AD9520 data sheet for more details.

CHANNEL DIVIDER WINDOW

The channel divider window shown in Figure 20 is accessed by clicking the appropriate channel divider. It is usually sufficient to change only the divide ratio because the evaluation software and the AD9520 duty cycle correction feature ensure that the output duty cycle remains very close to 50%.

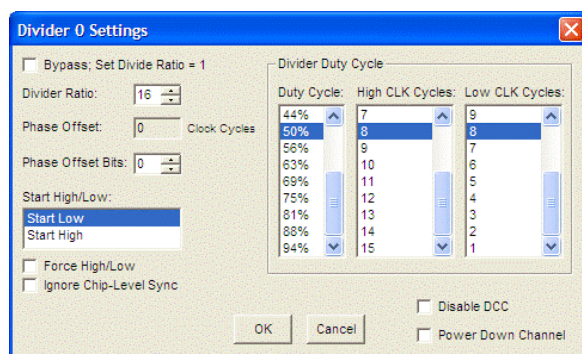


Figure 20. Channel Divider Window

You can also vary the phase offset by changing the **Phase Offset Bits** setting. However, for the new phase to take effect, the **SYNC** signal must be toggled via the **SYNC** button in the lower left corner of the main window.

OUTPUT DRIVER WINDOW

The output driver window shown in Figure 22 is accessed by clicking any of the numbered triangular output driver symbols on the right side of the main window (see Figure 21).

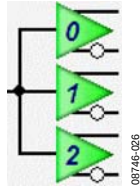


Figure 21. Driver Symbol

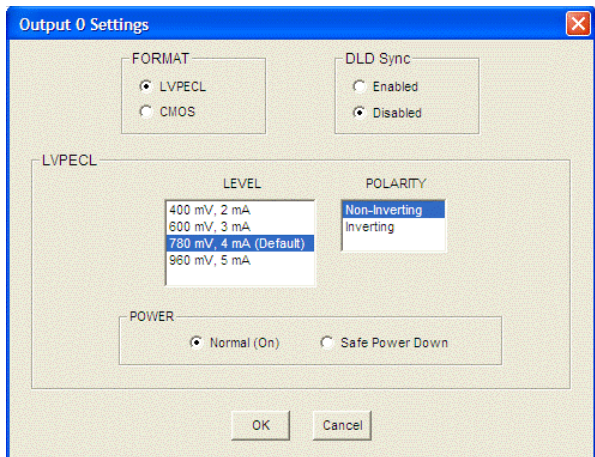


Figure 22. Output Driver Window

It is important to power down unused outputs on the evaluation board because they can be a major source of unwanted spurs.

LVPECL and CMOS outputs have different termination requirements, and OUT9 through OUT11 have been terminated differently from OUT0 through OUT8.

OUT 0 through OUT8 are ac-coupled with 200 Ω pull-down resistors on each output. This termination scheme is ideal for LVPECL drivers. However, this scheme degrades the CMOS driver performance. Improved CMOS driver performance is achieved by removing the 200 Ω pull-down resistors.

OUT9 through OUT11 have no termination resistors, and are ideally configured for CMOS operation. If you want to use these drivers in LVPECL mode, pull-down resistors must be added to the board. If you want to put 50 Ω termination at the SMA connectors of OUT9 through OUT11, add series decoupling capacitors so that the termination on OUT9 through OUT11 is identical to OUT0 through OUT8.

DEBUG WINDOW

The **Debug** window shown in Figure 23 is accessed by clicking the **Debug** option from the **View** menu.

The **Serial I/O** section of this window is a convenient way to read and write registers directly.

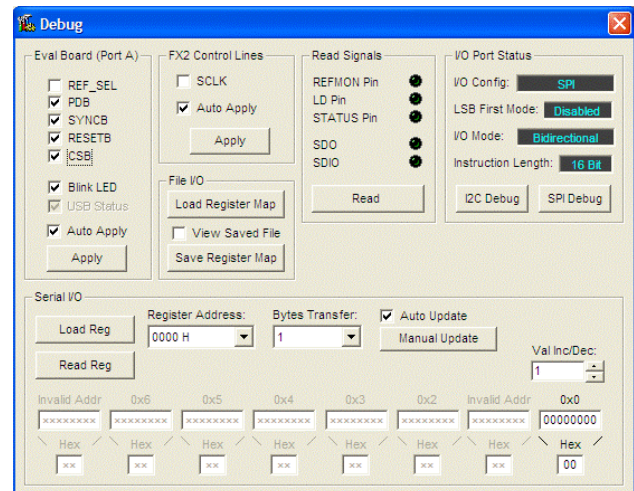


Figure 23. Debug Window

EVALUATION SOFTWARE MENU ITEMS

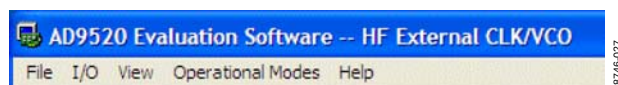


Figure 24. Menu Bar

MENU BAR

File Menu

The file menu has the following options:

Load Setup

Selecting Load Setup loads a previously saved AD9520 setup file (.stp). A setup file is a text file that contains the AD9520 register setup file, plus any evaluation board settings. Note that you must still perform a VCO calibration.

Save Setup

Selecting Save Setup saves an AD9520 setup file (.stp). A setup file is a text file that contains the AD9520 register setup file, plus any evaluation board settings.

Generate Binary File

Select this menu option to generate binary setup files that can be used by EEPROM programmers.

Exit

Exits the evaluation software. No checking is performed to ensure that the existing setup is saved.

I/O Menu

The I/O menu includes the following options:

Select Evaluation Board

The AD9520 evaluation system allows one PC to control multiple evaluation boards. This window allows you to select which evaluation board the software is controlling. Click **Refresh List** to detect a recently connected evaluation board (see Figure 25).

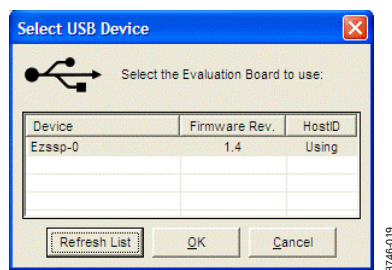


Figure 25. Select USB Device Window

Configure Serial Port

The **I/O Interface** window allows you to control how the USB controller interacts with the AD9520 serial port (see Figure 26).

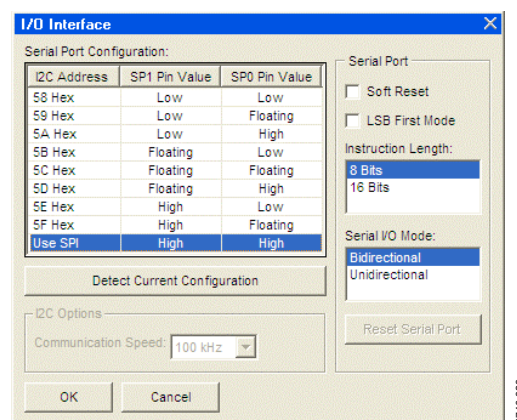


Figure 26. I/O Interface Window

If you are using I²C mode, this window allows you to select which address to use. Note that it should correspond to the S5 and S6 jumper settings on the evaluation board. You can also click **Detect Current Configuration** to discover which I²C address is active (see Figure 26).

However, if you are attempting to program an AD9520 on a remote board via a header cable from Connector P1, then the I²C address of the on-board AD9520 must not match the I²C address of the remote AD9520 that you are attempting to program.

View Menu

The **View** menu includes the following options:

Debug

This window (see Figure 23) allows you to write and read registers directly, as well as force the various configuration pins high and low.

Options

This window allows you to select Windows® XP visual styles.

Operational Modes Menu

This menu allows you to select any of the three operational modes in the AD9520 data sheet.

Help Menu

Selecting **Help** opens the **About AD9520** window, which contains information such as revision number, region information, and contact information.

AD9520 PLL LOOP FILTER

The AD9520 PLL requires an external loop filter whose components are tailored for different applications. The third-order passive configuration shown in Figure 27 usually offers the best performance for many applications and is the one found on the evaluation board.

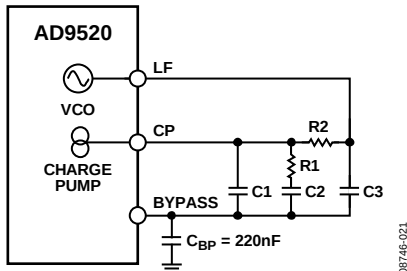


Figure 27. PLL Loop Filter

The default loop filter on the AD9520 evaluation board is optimized for reference clock cleanup. It has a flat transfer function with peaking <0.1 dB and loop bandwidths from 0.5 kHz to 10 kHz. In most of these applications, the phase detector is run at 1 MHz or less.

In the example in the Quick Start Guide to the AD9520 PLL section, the default loop filter shown in Table 2 results in a PLL with a loop bandwidth of 2.2 kHz, 80° of phase margin, and 0.05 dB of peaking. The charge pump current for this example is 1.2 mA.

For clock generation applications in which the reference clock is relatively low jitter, the high loop bandwidth (BW) loop filter shown in Table 2 is a better choice. Typical phase detector frequencies for these applications are 10 MHz to 100 MHz, and typical loop bandwidths for this loop filter are 50 kHz to 500 kHz, depending on the configuration.

The user should not consider these recommendations as a substitute for using ADIsimCLK™ to determine the best loop filter for a given application. ADIsimCLK is a free program that can help with the design and exploration of the capabilities and features of the AD9520, including the design of the PLL loop filter. The Analog Devices website has a sample ADIsimCLK file that includes the AD9520 default loop filter titled: **AD9520EvalBoardExample_148p5MHz.clk**.

ADIsimCLK Version 1.3 includes specific support for the AD9520. However, the AD9516, AD9520, and AD9522 share the same loop dynamics. Therefore, ADIsimCLK Version 1.2 can also be used for modeling the AD9520 loop filter by selecting the corresponding version of the AD9516. ADIsimCLK is available at www.analog.com/clocks.

Table 2 shows the correspondence between the components shown in Figure 27 and those on the evaluation board, as well as the default values.

Table 2. AD9520 Evaluation Board Default Loop Filter Values

ADIsimCLK	Evaluation Board Location	Clock Cleanup (Default)	High Loop BW
C1	C25	1500 pF	62 pF
R1	R5	2.1 kΩ	820 Ω
C2	C22	4.7 μF	240 nF
R2	R2	3 kΩ	390 Ω
C3	C31	2200 pF	33 pF

USING THE EVALUATION BOARD TO PROGRAM AN AD9520 ON A CUSTOMER BOARD

This guide shows how to use an AD9520 evaluation board to program an AD9520 on a customer board via the I²C interface. It assumes that the user has access to the I²C pins via a header on the target board, and knows the assigned address of the target I²C device.

1. Move Jumper S2 to the center and left (I²C) pins.
2. Move Jumper W1 to the center and left (I²C) pins.
3. Select the desired I²C address for the AD9520 evaluation board using Jumper S5 and Jumper S6. Note that the S5 = S6 = high setting is reserved for SPI mode. Also, this I²C address should not conflict with the I²C address of the target AD9520.
4. Attach a jumper cable from SDIO_SDA pin of Header P1 of the evaluation board to the SDA pin on the target board.
5. Repeat Step 4 for both the SCLK_SCL pin and GND pin of the AD9520 evaluation board to the SCL pin and ground pin of the target board, respectively. On the evaluation software, select **Configure Serial Port** from the I/O menu. This window is shown in Figure 28.

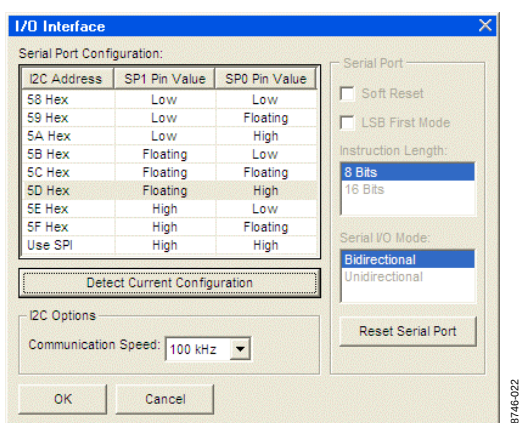


Figure 28. Evaluation Software Serial Port Configuration

6. Click **Reset Serial Port** and then click **Detect Current Configuration**. A dialog box appears and acknowledges the I²C mode and address. The evaluation software starts at I²C Address 0x058 and stops at the first valid I²C address that it finds. If the target I²C address is different from the one automatically selected, select the I²C address of the target AD9520 from the list, and click **OK**.
7. From the **View** menu on the menu bar (see Figure 24), and select **Debug**. Click the **I2C Debug** button. The window shown in Figure 29 appears.

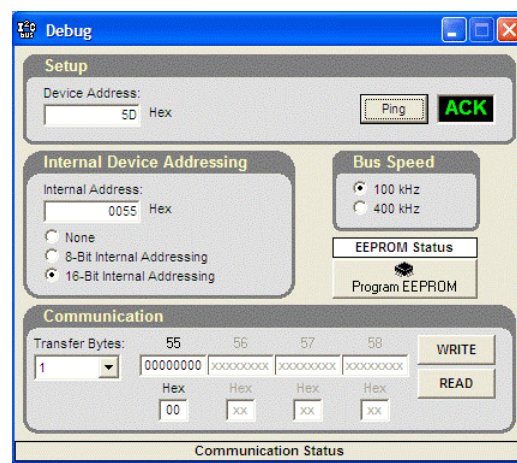


Figure 29. Evaluation Software I²C Debug Window

8. Enter the I²C address set by Jumper S5 and Jumper S6 on the AD9520 evaluation board, and click **Ping**. The user should see a green **ACK** message as shown in Figure 29. Repeat this step for the I²C address of the target AD9520. If **ACK** is returned for both addresses, the remote AD9520 is ready to be programmed. If the ping test fails, double-check the cabling between the boards, as well as the I²C address of the target AD9520. Ensure that the I²C address of the AD9520 on the evaluation board is different from the target AD9520. Also, disconnect the jumper cable, and make sure that I²C mode is working properly on the AD9520 evaluation board.
9. Proceed to program the target AD9520 with the desired settings. When finished, click the **EEPROM** button on the main window to access the EEPROM window, and then click **Program EEPROM** to write the settings to the EEPROM.

AD9520 BINARY FILE GENERATION

The AD9520 evaluation software can be used to generate binary setup files that can be used by EEPROM programmers, such as those made by BPM Microsystems.

Clicking **Generate Binary File** from the **File** menu prompts the user to enter a filename. The .bin extension is assumed. There is no facility for loading a .bin file into the software.

The binary file format is such that Byte Offset 0 in the binary file contains the value for Register 0x000.

CHECKSUM GENERATION

Both 8-bit and 16-bit checksums are supported. The device checksum is calculated using Address 0x00 through Address 0x232. The data pattern checksum uses Address 0x00 through Address 0xB03.

The 8-bit checksum is an 8-bit sum of the byte range described previously, whereas the 16-bit checksum forms a 16-bit word in which the MSB is the odd register addresses, and the LSB is the even-numbered registers. For example, Register 0x000 and Register 0x001 are paired together prior to the summation process.

The checksum values are also stored in the .stp files generated by the evaluation software.

AVOIDING CHECKSUM MISMATCHES

It is possible to have differences in the setup and binary files that may cause checksum mismatches. These scenarios are outlined as follows.

The evaluation software automatically sets the VCO calibration now bit (Register 0x018[0]) in the .bin file if the PLL is turned on. If the VCO calibration now bit is not set, the AD9520 will be unable to lock the PLL after automatically loading the register values from the EEPROM without further user intervention. Register 0x018[0] is not normally set in the register setup (.stp) file because the user normally initiates VCO calibration manually while running the evaluation software. To avoid a checksum mismatch, it is recommended that the user manually set the VCO calibration now bit in the setup file if the PLL is enabled.

Register 0x01F is a read-only status register whose value can change in between the writing of the setup (.stp) file and the binary (.bin) file. This situation is likely to occur if the reference input frequency monitors are enabled and the reference inputs are left floating. To prevent this, the user should avoid leaving the reference inputs floating, or disconnect the evaluation board while saving the setup and corresponding binary file.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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