

IR20153S & (PbF)

HIGH SIDE DRIVER WITH RECHARGE

Features

- Floating channel designed for bootstrap operation
Fully operational up to 150V
Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 5V to 20V
- Undervoltage lockout
- Internal recharge FET for bootstrap refresh
- Internal deadtime of 11 μ s and 0.8 μ s
- CMOS Schmitt-triggered input logic
- Output out of phase with input
- Reset input
- Split pull-up and pull-down gate drive pins
- Also available LEAD-FREE (PbF)

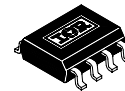
Product Summary

V_{OFFSET}	150V max.
$I_{\text{O+/-}}$	400mA @ $V_{\text{BS}}=7\text{V}$, 1.5A @ $V_{\text{BS}}=16\text{V}$
V_{OUT}	5-20V
$t_{\text{on/off}}$	1.0 and 0.3 μ s

Description

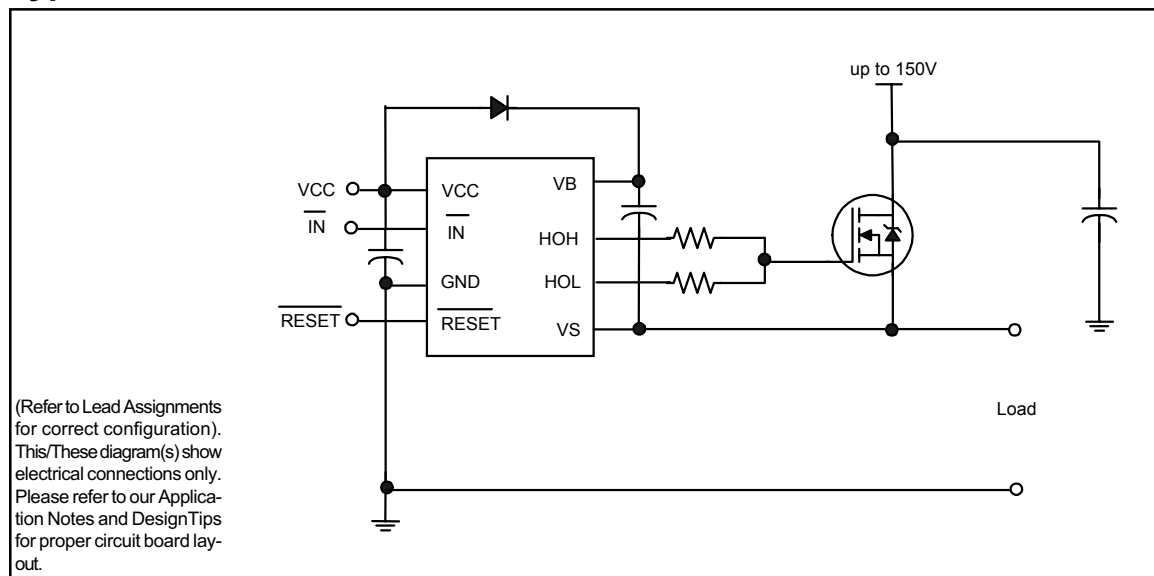
The IR20153S is a high voltage, high speed power MOSFET driver. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS output down to 3.3V. The output driver features a high pulse current buffer stage designed for minimum cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high or low side configuration which operates up to 150 volts.

Package



8-Lead SOIC

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND, all currents are defined positive into any lead. This is a stress only rating and operation of the device at these or any conditions exceeding those indicated in the operational sections of this specifications is not implied.

Symbol	Definition	Min.	Max.	Units
V_B	High side driver output stage voltage	-5.0	170	V
V_S	High side floating supply offset voltage	- 8.0	150	
V_{HO}	Output voltage gate high connection	$V_S - 0.3$	$V_B + 0.3$	
V_{CC}	Low side fixed supply voltage	-0.3	25	
V_{IN}	Input voltage (IN and RESET)		-0.3	$V_{CC} + 0.3$
dV/dt	Allowable offset voltage slew rate	—	50	V/nsec
T_J	Junction temperature	-55	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 2. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to GND. The V_S offset rating is tested with all suppliers biased at $V_{CC}=5V$ and $V_{BS}=7V$.

Symbol	Definition	Min.	Max.	Units
V_B	High side driver output stage voltage	$V_S + 5$	$V_S + 20$	V
V_S	High side floating supply offset voltage	-1.6	150	
V_{HO}	Output voltage gate high connection	V_S	V_B	
V_{CC}	Supply voltage	5	20	
V_{IN}	Input voltage (IN and RESET)	0	V_{CC}	
T_A	Ambient temperature	-55	150	°C

Electrical Characteristics

Unless otherwise specified, $V_{CC} = 5V$, $V_{BS} = 7V$, $V_S = 0V$, $I_N = 0V$, $R_{ES} = 5V$, load $R = 50\Omega$, $C = 6.8nF$ (see Figure 3).

Unless otherwise noted, these specifications apply for an operating ambient temperature of $T_A = 25^\circ C$.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
VCC Supply Characteristics						
V_{CCUV+}	VCC supply undervoltage positive going threshold	—	—	4.3	V	V_{CC} rising from 0V
V_{CCUV-}	VCC supply undervoltage negative going threshold	2.5	—	—		V_{CC} dropping from 5V
$V_{CCUVHYS}$	VCC supply undervoltage lockout hysteresis	0.01	0.3	0.60		
I_{QCC}	VCC supply current	—	—	400	μA	$V_{CC} = 3.6V$ & $6.5V$
VBS Supply Characteristics						
V_{BSUV+}	VBS supply undervoltage positive going threshold	—	—	4.3	V	VBS rising from 0V
V_{BSUV-}	VBS supply undervoltage negative going threshold	2.5	—	—		VBS dropping from 5V
$V_{BSUVHYS}$	VBS supply undervoltage lockout hysteresis	0.01	0.3	0.60		
I_{QBS1}	VBS supply current	—	—	100	μA	static mode, $V_{BS} = 7V$, $I_N = 0V$ or $5V$
I_{QBS2}	VBS supply current	—	—	200	μA	static mode, $V_{BS} = 16V$, $I_N = 0V$ or $5V$
VB. VS Supply Characteristics						
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 150V$
Gate Driver Characteristics						
I_{O+1}	Peak output source current	250	400	—	mA	
I_{O+2}	Peak output source current	800	1500	—	mA	$V_{BS} = 16V$
t_{r1}	Output rise time	—	0.2	0.4	μsec	
t_{r2}	Output rise time	—	0.1	0.2	μsec	$V_{BS} = 16V$
I_{O-1}	Peak output sink current	250	400	—	mA	$I_N = 5V$
I_{O-2}	Peak output sink current	800	1500	—	mA	$V_{BS} = 16V$, $I_N = 5V$
t_{f1}	Output fall time	—	0.2	0.4	μsec	$I_N = 5V$
t_{f2}	Output fall time	—	0.1	0.2	μsec	$V_{BS} = 16V$, $I_N = 5V$
t_{on}	Input-to-Output Turn-on propagation delay (50% input level to 10% output level)	—	1.0	2.0	μsec	
t_{off}	Input-to-Output Turn-off propagation delay (50% input level to 90% output level)	—	0.3	0.9	μsec	
$t_{res,off}$	RES-to-Output Turn-off propagation delay (50% input level to 90% $[t_{phl}]$ output levels)	—	0.3	0.9	μsec	

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Electrical Characteristics

Unless otherwise specified, $V_{CC} = 5V$, $V_{BS} = 7V$, $V_S = 0V$, $I_N = 0V$, $R_{ES} = 5V$, load $R = 50\Omega$, $C = 6.8nF$ (see Figure 3).

Unless otherwise noted, these specifications apply for an operating ambient temperature of $T_A = 25^\circ C$.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Gate Driver Characteristics cont.						
$t_{res,on}$	RES-to-Output Turn-On Propagation Delay (50% input level to 10% [t _{plh}] output levels)	-	1.0	2.0	μsec	
Input Characteristics						
V_{INH}	High Logic Level Input Threshold	3	-	-	V	
V_{INL}	Low Logic Level Input Threshold	-	-	1.4	V	
R_{IN}	High Logic Level Input Resistance	40	100	220	$k\Omega$	
V_{H_RES}	High Logic Level RES Input Threshold	3	-	-	V	
V_{L_RES}	Low Logic Level RES Input Threshold	-	-	1.4	V	
R_{RES}	High Logic Level RES Input Resistance	40	100	220	$k\Omega$	
Recharge Characteristics (see Figure 3a)						
t_{on_rech}	Recharge Transistor Turn-On Propagation Delay	7	11	15	μsec	$V_S = 5V$
t_{off_rech}	Recharge Transistor Turn-Off Propagation Delay	-	0.3	0.9	μsec	
V_{RECH}	Recharge Output Transistor On-State Voltage Drop	-	-	1.2	V	$I_S = 1mA$, $I_N = 5V$
Deadtime Characteristics						
DT_{HOFF}	High Side Turn-Off to Recharge gate Turn-On	7	11	15	μsec	
DT_{HON}	Recharge gate Turn-Off to High Side Turn-On.	0.4	0.8	1.5	μsec	

A True table for V_{CC}, V_{BS}, RESET, IN, H_O and RechFET is shown as follows. This truth table is for ACTIVE LOW IN.

V _{CC}	V _{BS}	RESET-	IN-	H _O	RechFET
<V _{CC} UVLO-	<V _{BS} UVLO-	HIGH	HIGH	OFF	ON
<V _{CC} UVLO-	<V _{BS} UVLO-	HIGH	LOW	OFF	ON
<V _{CC} UVLO-	<V _{BS} UVLO-	LOW	HIGH	OFF	ON
<V _{CC} UVLO-	<V _{BS} UVLO-	LOW	LOW	OFF	ON
<V _{CC} UVLO-	>V _{BS} UVLO+	HIGH	HIGH	OFF	ON
<V _{CC} UVLO-	>V _{BS} UVLO+	HIGH	LOW	OFF	ON
<V _{CC} UVLO-	>V _{BS} UVLO+	LOW	HIGH	OFF	ON
<V _{CC} UVLO-	>V _{BS} UVLO+	LOW	LOW	OFF	ON
>V _{CC} UVLO+	<V _{BS} UVLO-	HIGH	HIGH	OFF	ON
>V _{CC} UVLO+	<V _{BS} UVLO-	HIGH	LOW	OFF	OFF
>V _{CC} UVLO+	<V _{BS} UVLO-	LOW	HIGH	OFF	ON
>V _{CC} UVLO+	<V _{BS} UVLO-	LOW	LOW	OFF	ON
>V _{CC} UVLO+	>V _{BS} UVLO+	HIGH	HIGH	OFF	ON ¹
>V _{CC} UVLO+	>V _{BS} UVLO+	HIGH	LOW	ON	OFF ¹
>V _{CC} UVLO+	>V _{BS} UVLO+	LOW	HIGH	OFF	ON ¹
>V _{CC} UVLO+	>V _{BS} UVLO+	LOW	LOW	OFF	ON ¹

RESET = HIGH indicates that high side MOSFET is allowed to be turned on.

RESET = LOW indicates that high side MOSFET is OFF.

IN = LOW indicates that high side MOSFET is on.

IN = HIGH indicates that high side MOSFET is off.

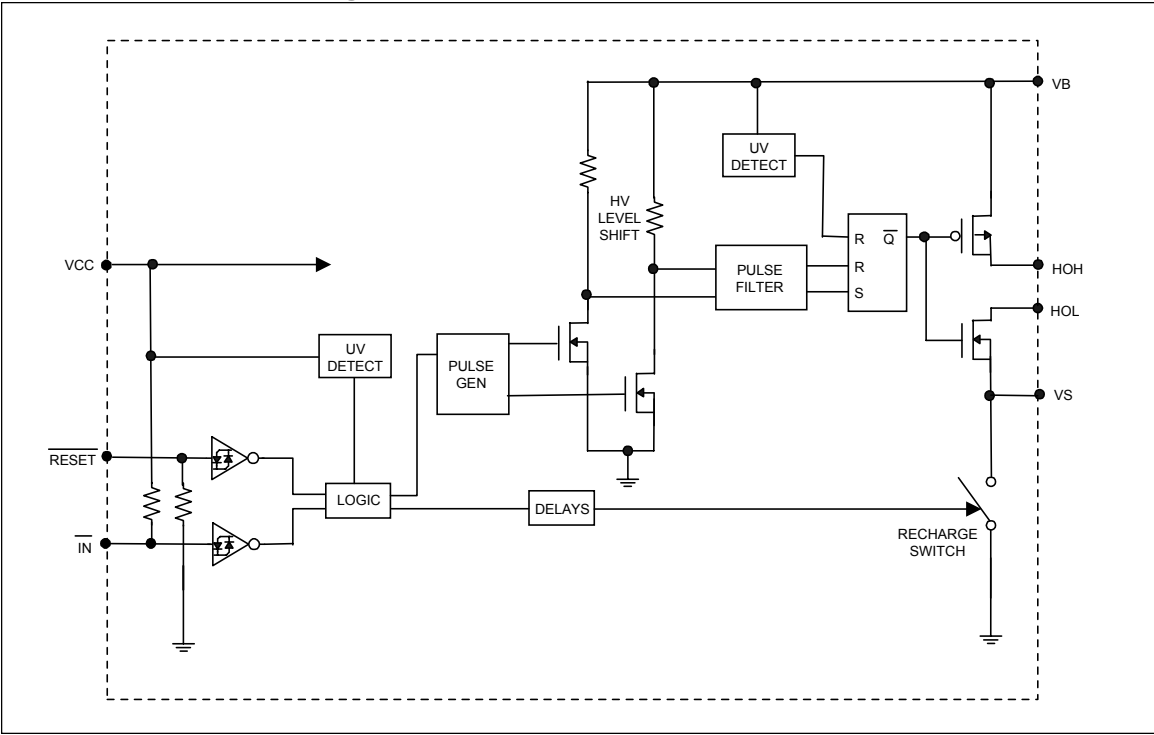
RechFET = ON indicates that the recharge MOSFET is on.

RechFET = OFF indicates that the recharge MOSFET is off.

¹Note: Refer to the RESET functionality graph of Figure 7, for V_{CC} and V_{BS} voltage ranges under which the functionality is normal.

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Functional Block Diagram



Lead Definitions and Assignments

Symbol	Description	
VCC	Driver Supply	8-Lead SOIC
IN-	Driver Control Signal Input	
GND	Ground	
RESET	Driver Enable Signal Input	
VS	MOSFET Source Connection	
H _{OL}	MOSFET Gate Low Connection	
H _{OH}	MOSFET Gate High Connection	
VB	Driver Output Stage Supply	

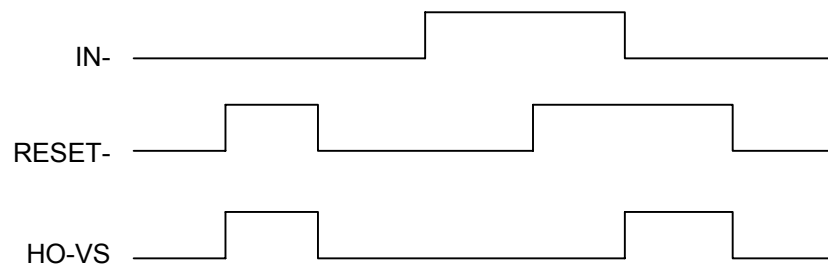


Figure 1. Input/Output Functional Diagram

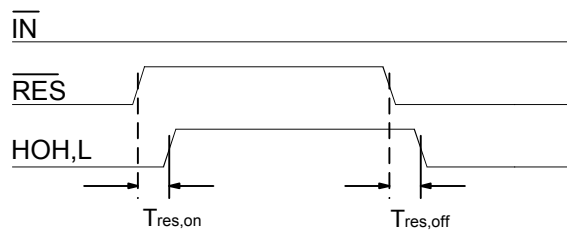


Figure 1a. Reset Timing Diagram

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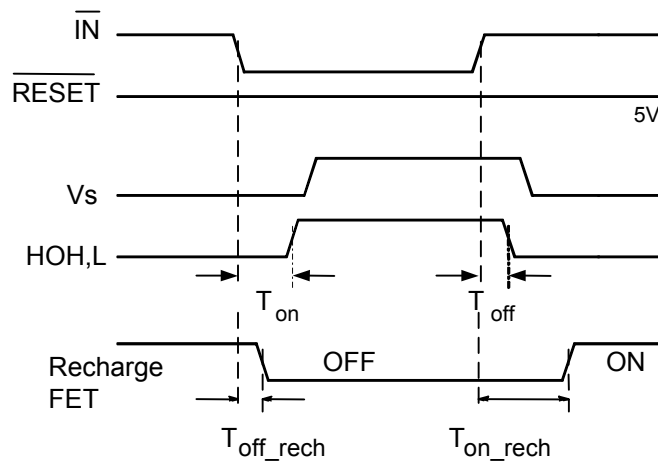


Figure 2. Input/Output Timing Diagram

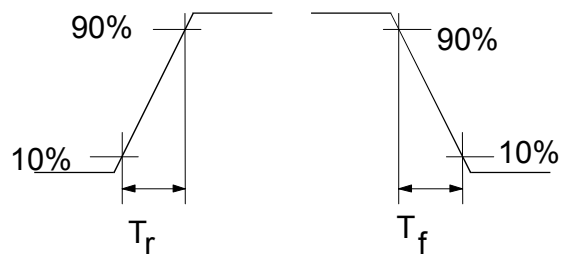


Figure 2a. Output Timing Diagram

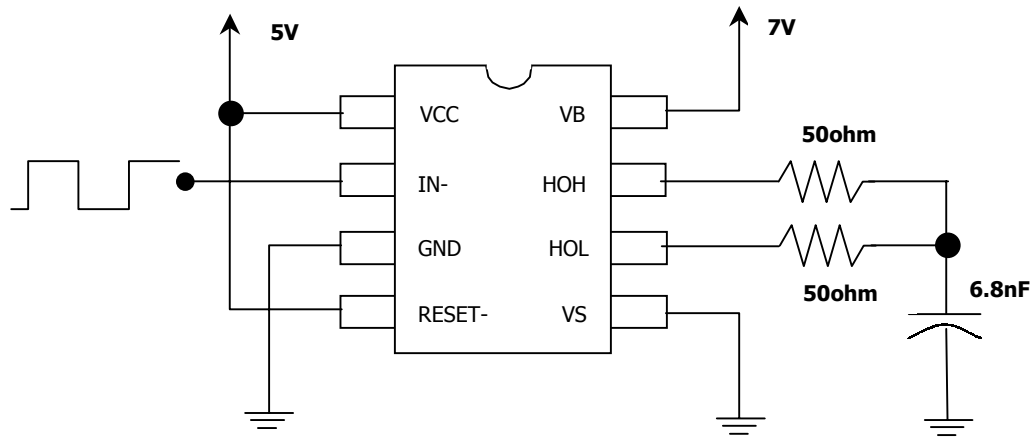


Figure 3. Switching Time Test Circuit

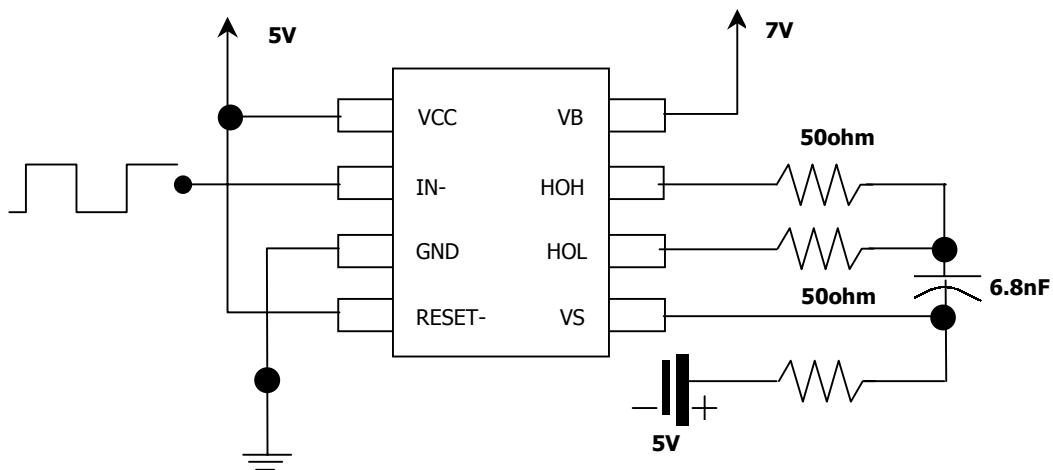


Figure 3a. Ton_rech and Toff_rech Test Circuit

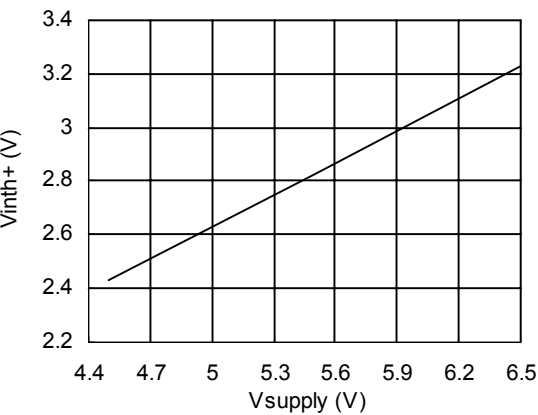


Figure 4. Positive Input and Reset Threshold Voltage vs. Vsupply

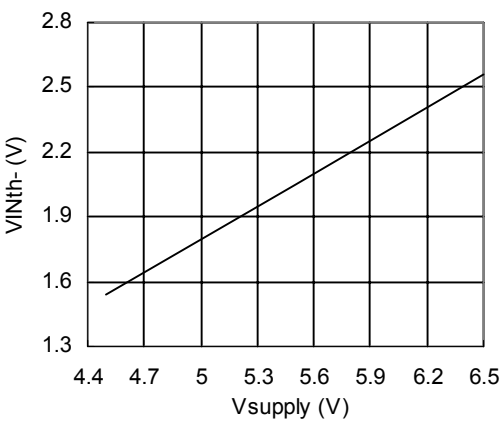


Figure 5. Negative Input and Reset Threshold Voltage vs. Vsupply

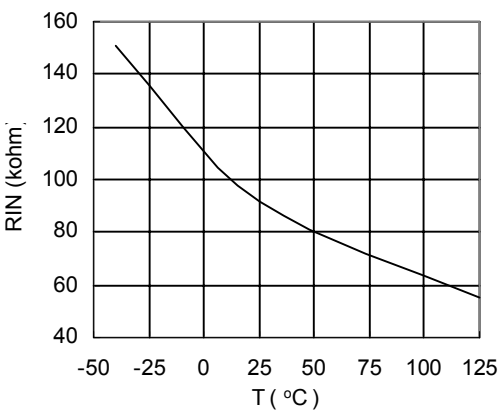


Figure 6. Input and Reset Impedance vs. Temperature

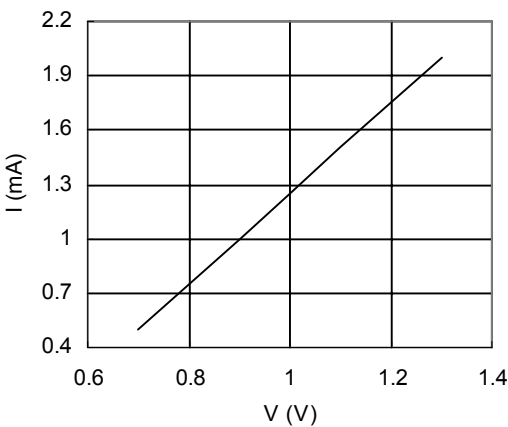


Figure 7. Recharge FET I-V Curve

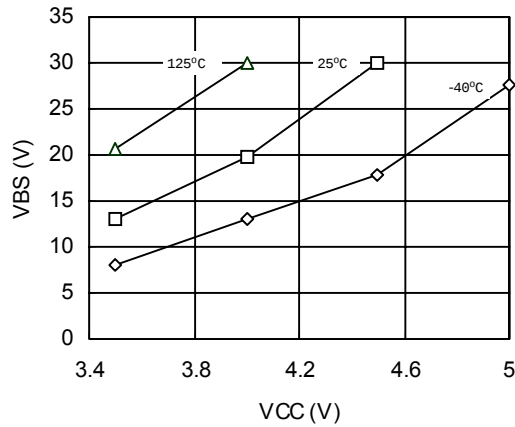


Figure 8. Reset Functionality

This graph explains the functionality limitation as a function of VCC, VBS and temperature. Each curve on the graph represents VCC Vs. VBS, for a particular temperature. For each particular temperature and VCC, the output is non-functional for any value of VBS above the drawn curve. But for any value of VBS below the curve the functionality is fine.

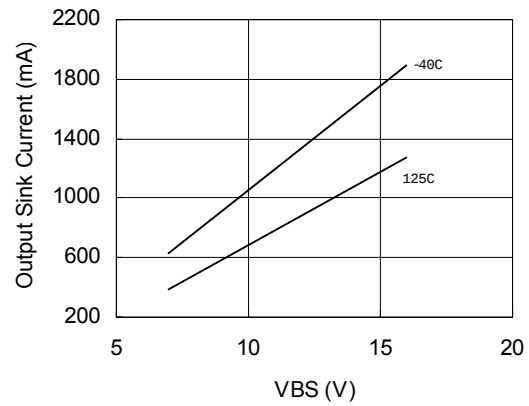


Figure 9. Output Sink Current vs. VBS

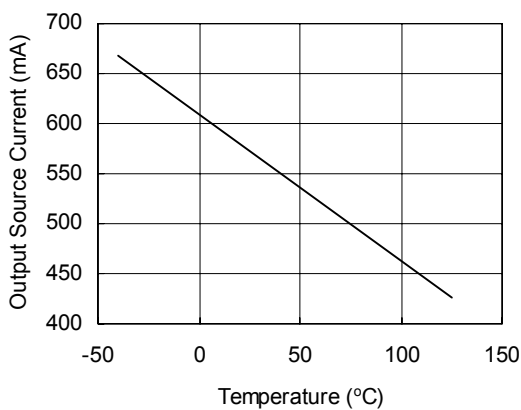


Figure 10. Output Source Current vs. Temperature, VBS=7V

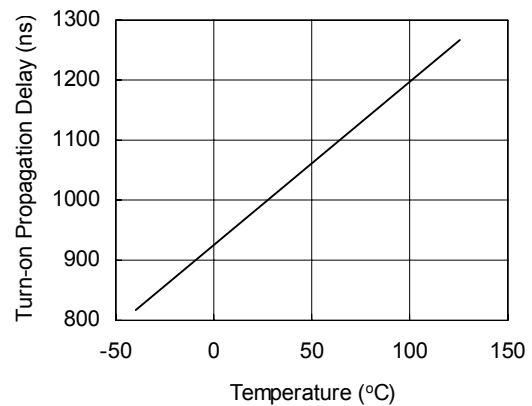


Figure 11. Turn-on Propagation Delay vs. Temperature, VBS=7V

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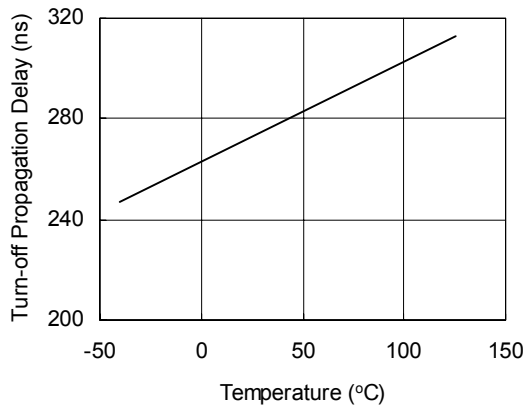


Figure 12. Turn-off Propagation Delay vs. Temperature, VBS=7V

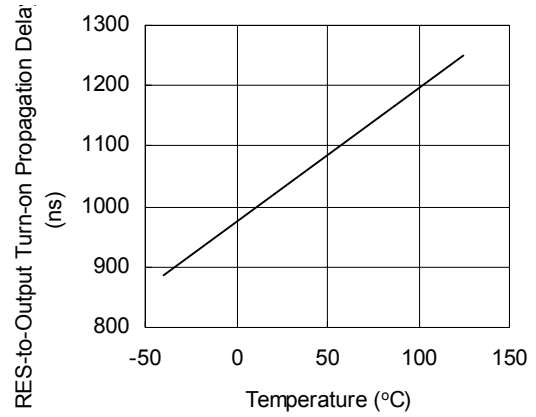


Figure 13. RES-to-Output Turn-on Propagation Delay vs. Temperature, VBS=7V

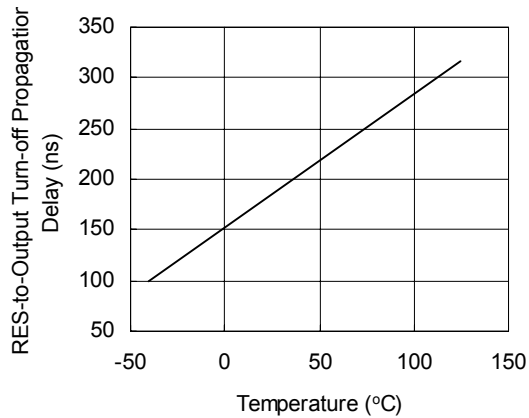


Figure 14. RES-to-Output Turn-off Propagation Delay vs. Temperature, VBS=7V

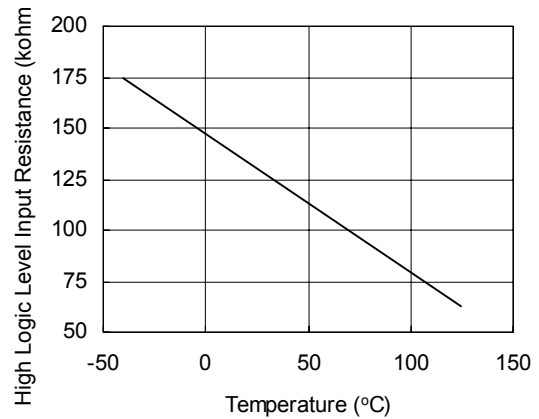


Figure 15. High Logic Level Input Resistance vs. Temperature, VBS=7V

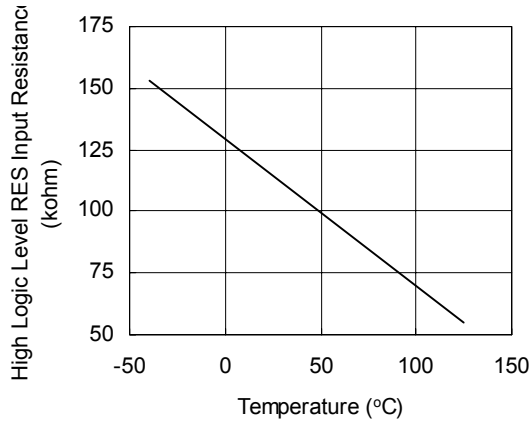


Figure 16. High Logic Level RES Input Resistance vs. Temperature, VBS=7V

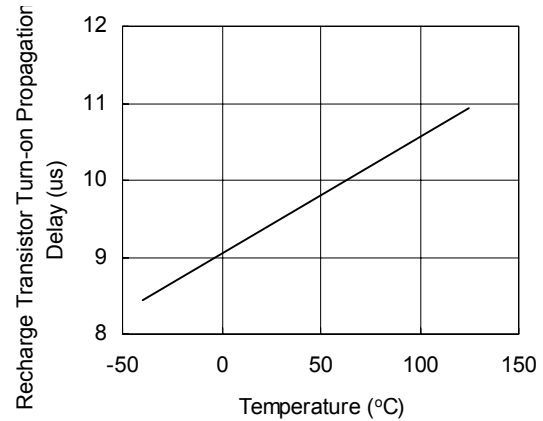


Figure 17. Recharge Transistor Turn-on Propagation Delay vs. Temperature, VBS=7V

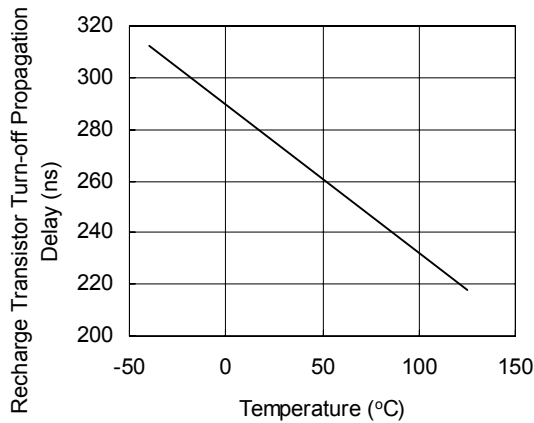


Figure 18. Recharge Transistor Turn-off Propagation Delay vs. Temperature, VBS=7V

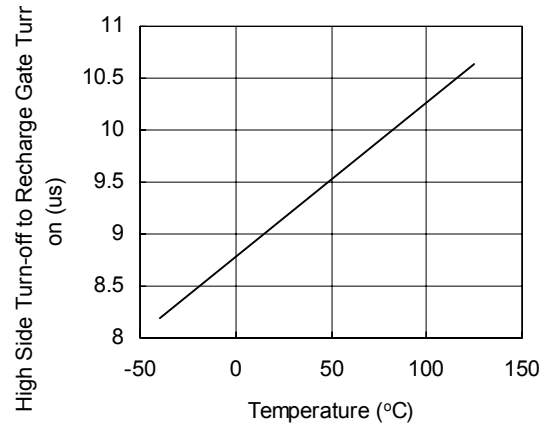


Figure 19. High Side Turn-off to Recharge Gate Turn-on vs. Temperature, VBS=7V

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Top View: Shows an 8-pin package with pins numbered 1-4 on the bottom and 5-8 on the top. Dimensions include width D, height H, and lead length E. A detail shows a hole diameter of $\varnothing 0.25$ [0.010] with a maximum material condition (M) and a note A.

Side View: Shows the package profile with dimensions A (height), C (lead height), and A1 (lead thickness). A detail shows a fillet radius of 0.10 [0.004].

Footprint View: Shows the solder pad layout with dimensions 8X 0.72 [0.028] for the pads and 8X 1.78 [0.070] for the spacing. A note indicates a 45° lead angle.

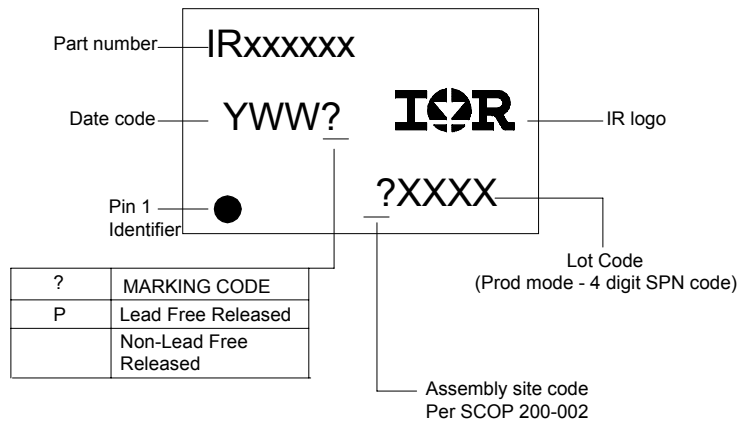
Pinout Table:

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:

- DIMENSION & TOLERANCING PER ASME Y14.5M-1994.
- CONTROLLING DIMENSION: MILLIMETER
- DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)

8-Lead SOIC IR20153S order IR20153S

Leadfree Part

8-Lead SOIC IR20153S order IR20153SPbF