



# 300mA High Efficiency Low Quiescent Current Synchronous Buck Regulator With Z-mode

The 34726 is a high efficiency, low quiescent current ( $I_Q$ ), synchronous buck regulator, implementing Freescale's innovative Z-mode architecture. Freescale's Z-mode architecture greatly improves the ripple performance during light load currents, but still maintains a low quiescent current of 65 $\mu$ A, at no load in "Sleepy" Z-mode.

The 34726 accepts an input voltage in the range of 2.7 to 5.5V, making it ideally suited for single cell Li-Ion based applications. Factory preset output voltages, ranging from 0.8V to 3.3V, reduce the number of required auxiliary components. The part is able to provide 300mA of continuous load current across the input and the output voltage ranges.

The 34726 switches at 2.0MHz to allow the use of small, surface mount inductors and capacitors to save precious board space.

The 34726 is available in the small, space saving, and low cost, 2x2 UDFN-8 packages. The part is guaranteed for operation over the -25°C to 85°C temperature range.

## Features

- 94% peak efficiency
- 2.0MHz switching frequency
- 2.7V to 5.5V input voltage range
- Automatic transition to energy saving light load Z-mode (low ripple)
- Fixed output voltage options from 0.8 to 3.3V
- 65 $\mu$ A quiescent current during sleepy Z-mode
- 300mA maximum continuous output current
- Internal 2.0ms soft start
- Thermal and over-current protection
- 0.1 $\mu$ A quiescent current in shutdown (disabled)
- Ultra thin 2x2 UDFN package
- Pb-free packaging designated by suffix code FC

**34726**

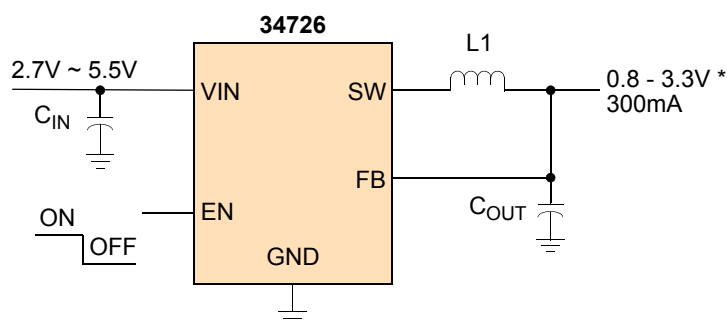
**POWER MANAGEMENT IC**



Bottom View  
**FC SUFFIX (PB-FREE)**  
**98ASA10787D**  
**8-PIN UDFN**  
**2X2**

## ORDERING INFORMATION

Device	Temperature Range ( $T_A$ )	Package
MC34726AFC/R2	-25°C to 85°C	8-UDFN
MC34726BFC/R2		
MC34726CFC/R2		



\*Programmable  
See table 1

**Figure 1. 34726 Typical Operating Circuit**

\* This document contains certain information on a new product. Specifications and information herein are subject to change without notice.

## DEVICE VARIATIONS

**Table 1. Device Variations**

Freescal Part No.	V <sub>IN</sub> Range	Output Voltage <sup>(1)</sup>	Maximum Load Current	Switch Frequency (MHz) <sup>(2)</sup>
MC34726AFC	2.7 - 5.5V	1.2V	300mA	2.0
MC34726BFC	2.7 - 5.5V	1.8V	300mA	2.0
MC34726CFC	3.6 - 5.5V	3.3V	300mA	2.0

**Notes**

1. Output voltages of: 0.8V, 0.9V, 1.0V, 1.1V, 1.3V, 1.4V, 1.5V, 1.85V, 2.0V, 2.5V options available on request. Contact Freescale sales.
2. Factory programmable at 2.0MHz or 4.0Mhz. Contact Freescale sales for availability of the 4.0MHz functionality.

## INTERNAL BLOCK DIAGRAM

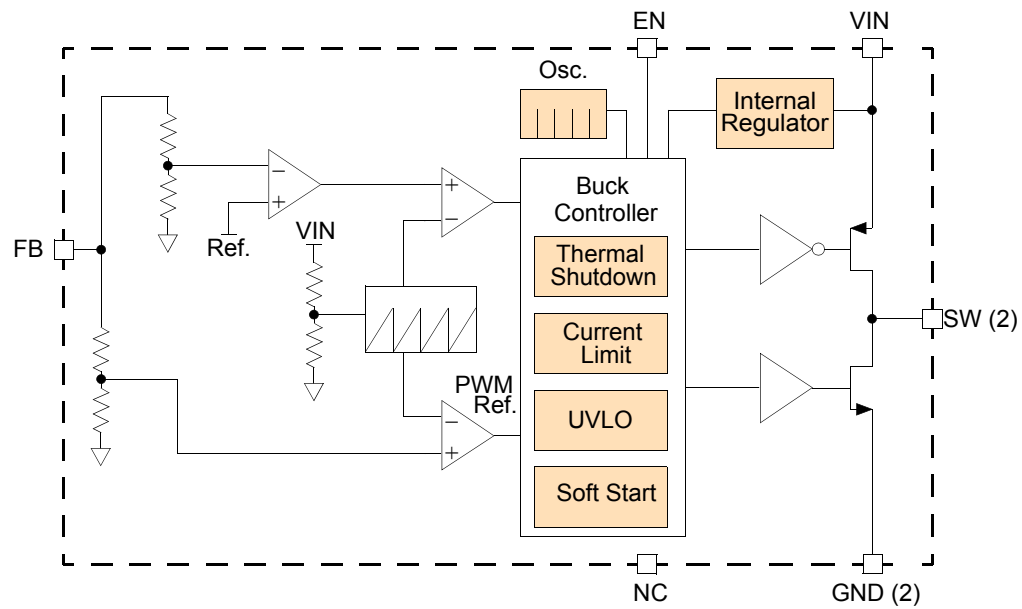


Figure 2. 34726 Simplified Internal Block Diagram

## PIN CONNECTIONS

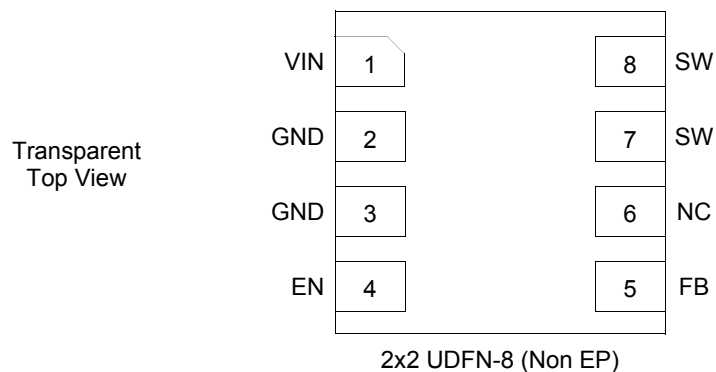


Figure 3. 34726 Pin Connections

Table 2. 34726 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on [page 10](#).

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	VIN	Input	Supply Voltage Input	Power input
2	GND	Ground	Ground	Ground
3	GND	Ground	Ground	Low noise ground
4	EN	Input	Enable	Active high enable input
5	FB	Input	Feedback Input	Feedback of the output voltage
6	NC	N/A	No Connection	Internally not connected. Connect to GND externally
7	SW	Output	Switching Node	This terminal connects to the output inductor
8	SW	Output	Switching Node	This terminal connects to the output inductor

## ELECTRICAL CHARACTERISTICS

## MAXIMUM RATINGS

**Table 3. Maximum Ratings**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
<b>ELECTRICAL RATINGS</b>			
All pins voltages	$V_{IN}, V_{EN}, V_{FB}, V_{SW}$	-0.3 to 6.0	V
ESD Voltage <sup>(1)</sup>	$V_{ESD}$		V
Human Body Model (HBM)		±2000	
Machine Model (MM)		±200	
<b>THERMAL RATINGS</b>			
Operating Ambient Temperature Range	$T_A$	-25 to +85	°C
Storage Temperature Range	$T_{STG}$	-25 to +150	°C
Maximum Lead Temperature <sup>(2),(3)</sup>	$T_{PPRT}$	Note 3	°C
Junction Temperature	$T_J$		°C
Operating Junction Temperature		125	
Maximum Junction Temperature		+150	
Thermal Resistance <sup>(4)</sup>			°C/W
Junction-to-Case	$R_{\theta JC}$	104	
Junction-to-Ambient	$R_{\theta JA}$	122	
Power Dissipation	$P_D$		W
Continuous (Derate 3.0mW/°C and over $T_A = 70^\circ\text{C}$ )		0.5	

## Notes

- ESD testing is performed in accordance with the Human Body Model (HBM) ( $C_{ZAP} = 100\text{pF}$ ,  $R_{ZAP} = 1500\Omega$ ), and the Machine Model (MM) ( $C_{ZAP} = 200\text{pF}$ ,  $R_{ZAP} = 0\Omega$ ).
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescall's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL). Go to [www.freescale.com](http://www.freescale.com), search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx)], and review parametrics.
- Device mounted on the Freescale EVB test board per JEDEC DESD51-2.

## STATIC ELECTRICAL CHARACTERISTICS

**Table 4. Static Electrical Characteristics**

Characteristics noted under conditions;  $2.7V \leq V_{IN} \leq 5.5V$ ,  $0.8V \leq V_{OUT} \leq 3.3V$ ,  $-25^{\circ}C \leq T_A \leq 85^{\circ}C$ ,  $C_{IN} = C_{OUT} = 4.7\mu F$ ,  $L1 = 4.7\mu H$  (See [Figure 1](#)), unless otherwise noted. The typical specifications are measured at the following conditions;  $T_A = +25^{\circ}C$ ,  $V_{IN} = 3.6V$ ,  $f_{SW} = 2.0MHz$  with the typical operating circuit (See [Figure 1](#)), unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{IN}$	2.7	-	5.5	V
Output Voltage (Factory preset)	$V_{OUT}$	0.8	-	3.3	V
Output Current	$I_{OUT}$	300	-	-	mA
Total Supply Current <sup>(5)</sup> Regulator disabled	$I_{DIS}$	-	0.1	1.0	$\mu A$
Quiescent Current (Switching) Sleepy Z-mode and $I_{LOAD} = 0mA$	$I_Q$	-	65	85	$\mu A$
Current Limit Current rising at high side	$I_{PK}$	-	450	-	mA
Output Voltage Accuracy (% of output voltage) Over load and temperature	$\Delta V_{OUT}$	-3%	-	3%	$V_{OUT}$
UVLO Threshold <sup>(6)</sup> $V_{IN}$ : 2.7 -5.5V $V_{IN}$ rising $V_{IN}$ falling	$V_{UVLO}$	- 2.5	- -	2.7 -	V
Enable Voltage Regulator operating Regulator shutdown	$V_{EN}$	1.6 -	- -	- 0.4	V
High Side Power MOSFET On Resistance $V_{IN} = 3.6V$ , $V_{OUT} = 1.8V$ , $T_A = 40^{\circ}C$ , $I_{LOAD} = 150mA$	$R_{DS(ON)H}$	-	250	-	$m\Omega$
Low Side Power MOSFET On Resistance $V_{IN} = 3.6V$ , $V_{OUT} = 1.8V$ , $T_A = 40^{\circ}C$ , $I_{LOAD} = 150mA$	$R_{DS(ON)L}$	-	350	-	$m\Omega$
Load Regulation $1mA < I_{LOAD} < 300mA$ and $V_{OUT} = 1.8V$	$\Delta V_{OUT}/\Delta I_{OUT}$	-	0.5	-	%
Line Regulation $V_{IN} = 2.7V$ to $5.5V$	$\Delta V_{OUT}/\Delta V_{IN}$	-	0.5	-	%
Start-up Overshoot (% of output voltage) $I_{LOAD} = 0mA$ , $V_{OUT} = 1.8V$ and $C_{OUT} = 4.7\mu F$	$V_{STO}$	-	3%	-	$V_{OUT}$
Thermal Shutdown Threshold (Junction Temperature)	$T_{STDN}$	-	140	-	$^{\circ}C$
Thermal Shutdown Hysteresis (Junction Temperature)	$T_{HYSTR}$	-	10	-	$^{\circ}C$

**Notes**

- Maximum  $I_{DIS}$  measured at  $V_{IN} = 3.6V$  and  $T_A = 25^{\circ}C$ .
- For a product with a  $V_{OUT}$  of 3.3V and a  $V_{IN}$  minimum less than 3.6V, the  $V_{OUT}$  value will track (drop below 3.3V)  $V_{IN}$  down to a value of 2.5V, where the UVLO shutdown mechanism will activate.

**DYNAMIC ELECTRICAL CHARACTERISTICS****Table 5. Dynamic Electrical Characteristics**

Characteristics noted under conditions;  $2.7V \leq V_{IN} \leq 5.5V$ ,  $0.8V \leq V_{OUT} \leq 3.3V$ ,  $-20^{\circ}C \leq T_A \leq 85^{\circ}C$ ,  $C_{IN} = C_{OUT} = 4.7\mu F$ ,  $L1 = 4.7\mu H$  (See [Figure 1](#)), unless otherwise noted. The typical specifications are measured at the following conditions;  $T_A = +25^{\circ}C$ ,  $V_{IN} = 3.6V$ ,  $f_{SW} = 2.0MHz$  with the typical operating circuit (See [Figure 1](#)), unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Switching Frequency <sup>(7)</sup>	$f_{SW}$	1.8	2.0	2.2	MHz
Maximum Duty Cycle <sup>(8)</sup> Measured from SW pin	$D_{MAX}$	95	-	100	%
Internal Soft-start Timer $V_{OUT}$ Rise Time	$t_S$	-	2.0	-	ms

**Notes**

7.  $f_{SW}$  can be factory programmed to  $\pm 20\%$  of nominal 2.0MHz.
8. The maximum duty limits the range of output voltages achievable for a given input voltage.

## ELECTRICAL PERFORMANCE CURVES

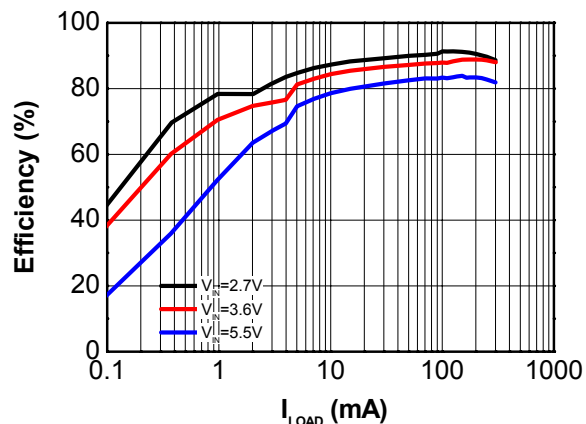


Figure 4. Efficiency vs. Load Current  
 $V_{IN} = 3.6V$ ,  $V_{OUT} = 1.8V$ ,  $T_A = 25^\circ C$

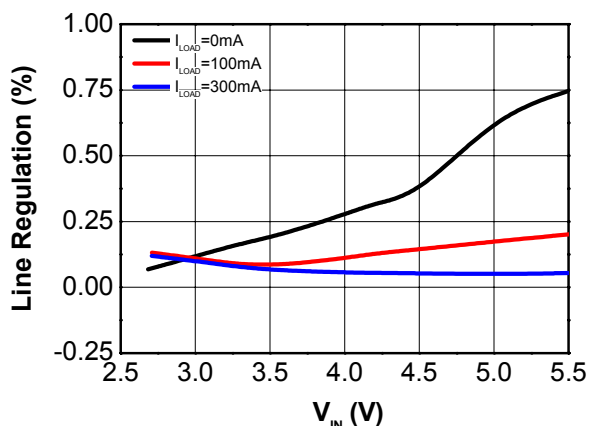


Figure 5. Line Regulation  
 $V_{IN}$  is 2.7V to 5.5V and  $V_{OUT}$  is 1.8V,  $T_A = 25^\circ C$

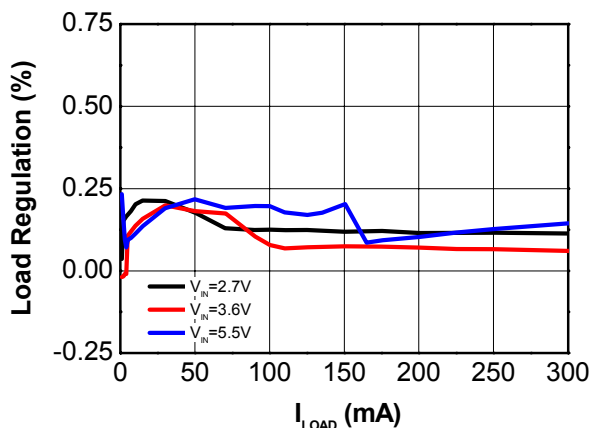


Figure 6. Load Regulation  
 $1mA < I_{LOAD} < 300mA$ ,  $V_{OUT} = 1.8V$

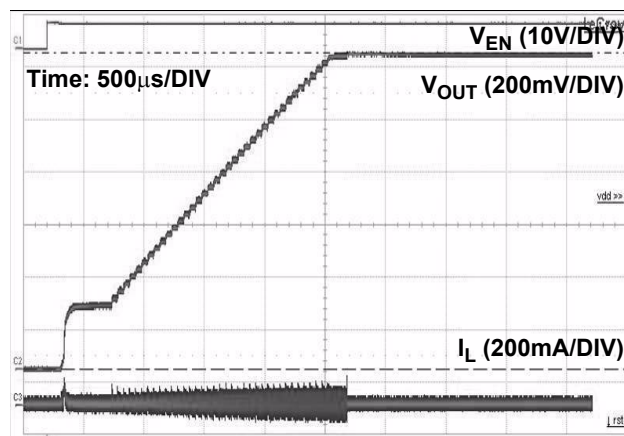


Figure 7. Start-up Response  
 $I_{LOAD} = 0mA$ ,  $V_{OUT} = 1.2V$

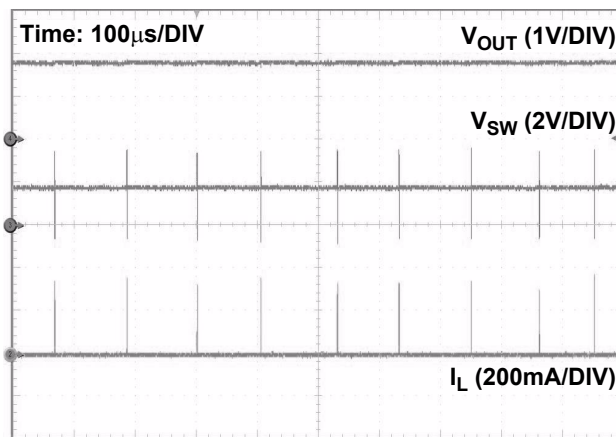


Figure 8. Sleepy Z-Mode™ Switching Waveforms  
 $V_{IN} = 3.6V$ ,  $V_{OUT} = 1.8V$  and  $I_{LOAD} = 1.0mA$

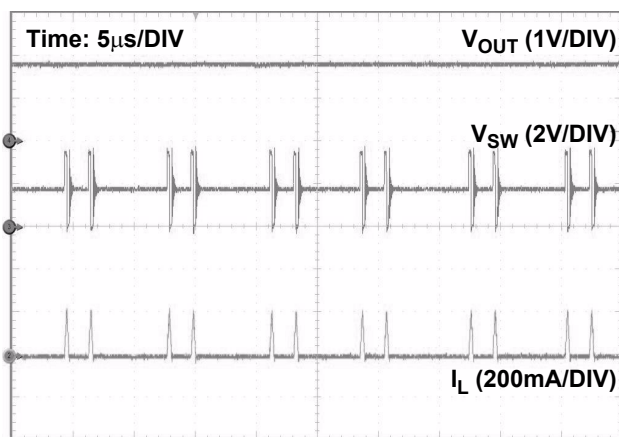


Figure 9. Z-Mode™ Switching Waveforms  
 $V_{IN} = 3.6V$ ,  $V_{OUT} = 1.8V$  and  $I_{LOAD} = 10mA$



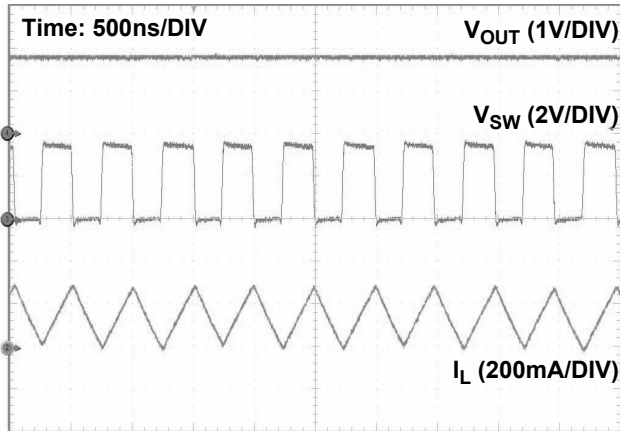


Figure 10. CCM Switching Waveforms  
 $V_{IN} = 3.6V$ ,  $V_{OUT} = 1.8V$  and  $I_{LOAD} = 150mA$

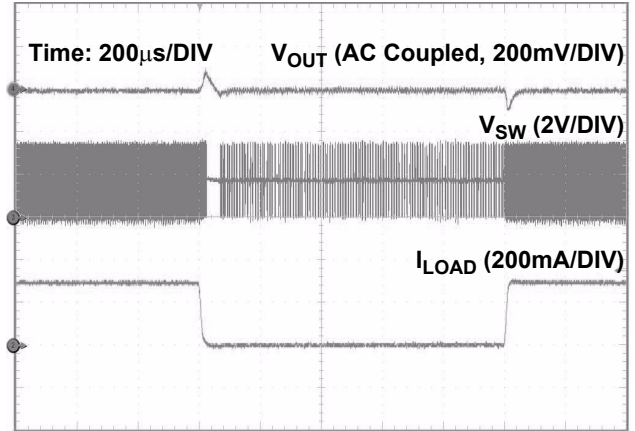


Figure 12. Load Transient in Z-Mode™  
 $V_{IN} = 3.6V$ ,  $I_{LOAD} = 10mA$  to  $300mA$

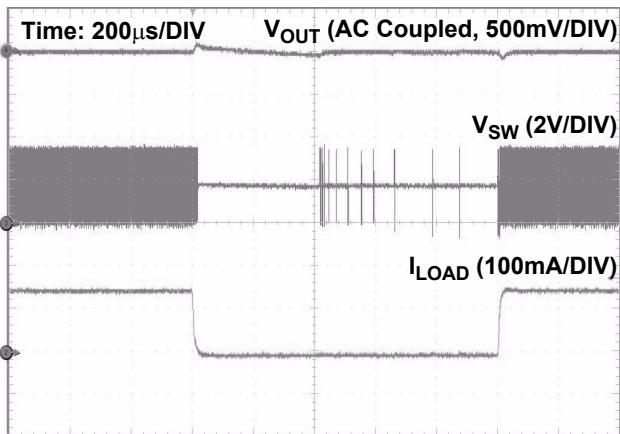


Figure 11. Load Transient in Sleepy Z-Mode™  
 $V_{IN} = 3.6V$ ,  $I_{LOAD} = 1mA$  to  $150mA$

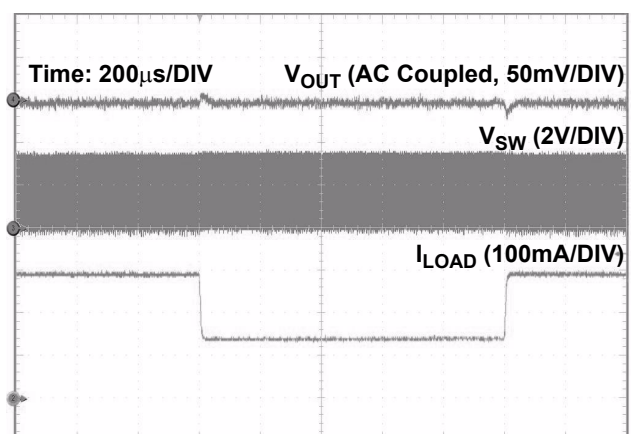


Figure 13. Load Transient in CCM  
 $V_{IN} = 3.6V$ ,  $I_{LOAD} = 150mA$  to  $300mA$

## FUNCTIONAL DESCRIPTION

### *INTRODUCTION*

The 34726 is a high efficiency, synchronous, buck regulator, utilizing a voltage mode control architecture with feed forward. It is capable of providing a 300mA load current for output voltages of 0.8V to 3.3V, from a single input voltage rail between 2.7V and 5.5V.

In a buck converter, most of the losses at high output loads are due to conduction losses in the power train, but at light output loads, the conduction losses are reduced and most of the losses become switching losses. Using Freescale's Z-mode architecture, the 34726, at light output loads, will smoothly transition into a lower switching frequency, thus improving its efficiency.

### *FUNCTIONAL PIN DESCRIPTION*

#### **SUPPLY VOLTAGE INPUT (VIN)**

2.7V to 5.5V DC power input. Bypass with a 4.7 $\mu$ F ceramic capacitor as close as possible to the VIN and GND pins.

#### **GROUND (GND)**

Ground.

#### **ENABLE (EN)**

Active high enable input. EN is over-voltage protected to 6.0V, independent of the supply voltage. Drive with a logic high signal (or connect to VIN) for normal operation. Drive with a logic low signal, or connect to GND will disable the 34726.

#### **FEEDBACK INPUT (FB)**

Feedback of the output voltage.

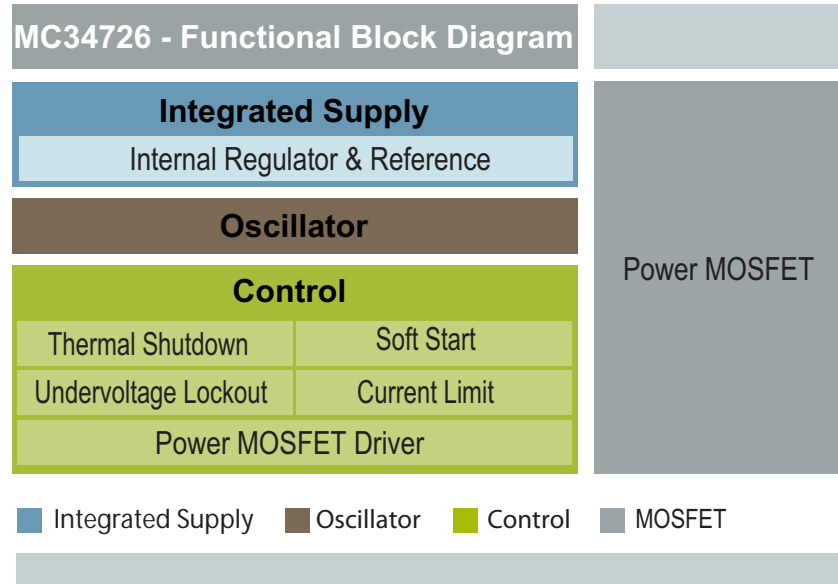
#### **SWITCHING NODE (SW)**

This terminal connects to the output inductor. The node internally connects the drain of both high side MOSFET and low side MOSFET.

#### **NO CONNECTION (NC)**

Internally not connected. Connect to GND externally.

## FUNCTIONAL INTERNAL BLOCK DESCRIPTION



**Figure 14. 34726 Functional Internal Block Diagram**

### INTEGRATED SUPPLY

#### INTERNAL REGULATOR AND REFERENCE

The internal regulator and reference block steps down the high input voltage to lower voltage, to power all the internal blocks, and provides the reference voltage for the other internal blocks.

#### OSCILLATOR

The oscillator block provides 2.0MHz clock signal to the controller.

### CONTROLLER

#### THERMAL SHUTDOWN

The thermal shutdown block monitors the die temperature. Once the die temperature reaches its threshold, this block turns off the device to prevent the further die temperature rise.

#### SOFT-START

The soft-start block controls the output voltage ramp after the device is enabled, to limit the in-rush current. The start-up time is internally set to approximately 2.0ms, and is independent of input voltage, output voltage, or load current.

The soft-start sequence also occurs upon recovery from any fault condition.

#### UVLO

The UVLO block monitors the input voltage. Once the input voltage is lower than the falling threshold voltage, this block turns off the device, to avoid unpredictable circuit behavior.

#### CURRENT LIMIT

The current limit block monitors the inductor current. When the peak inductor current reaches its current limit, this block turns off the high side MOSFET, to prevent the device and external components from damage.

#### POWER-MOSFET DRIVER

The power-MOSFET-driver block controls the phase of the driver signals and enhances the drive capability of these

#### POWER-MOSFET

The power-MOSFET block contains two power MOSFETs. One is a PMOS that passes the current from the input to the output, and the other one is an NMOS that provides the inductor current loop when PMOS is turned off.

## FUNCTIONAL DEVICE OPERATION

### OPERATIONAL MODES

#### Z-MODE OPERATION

The 34726 operates as a typical fixed frequency, PWM regulator, at moderate to heavy load currents. As the load is decreased, such that operation transitions from continuous conduction mode (CCM) to discontinuous conduction mode (DCM), the duty cycle is reduced until it approaches 85% of the full load duty cycle. At this point the 34726 transitions into Z-mode operation, where the Z-mode Factor is 0.85. In Z-mode, the regulator skips pulses whenever the duty cycle is

below 85% of the CCM duty cycle. As the load decreases, this pulse skipping reduces the switching frequency and the switching losses thus improving efficiency. For example, if a light load demanded a 30% duty cycle at 2.0MHz, with Z-mode this same load will require only  $(0.3/0.85)^2 \times 2.0\text{MHz} = 0.249\text{MHz}$  switching frequency, hence switching losses will be reduced by almost ten fold. [Figure 15](#) illustrates the transition to and the exit from Z-mode.

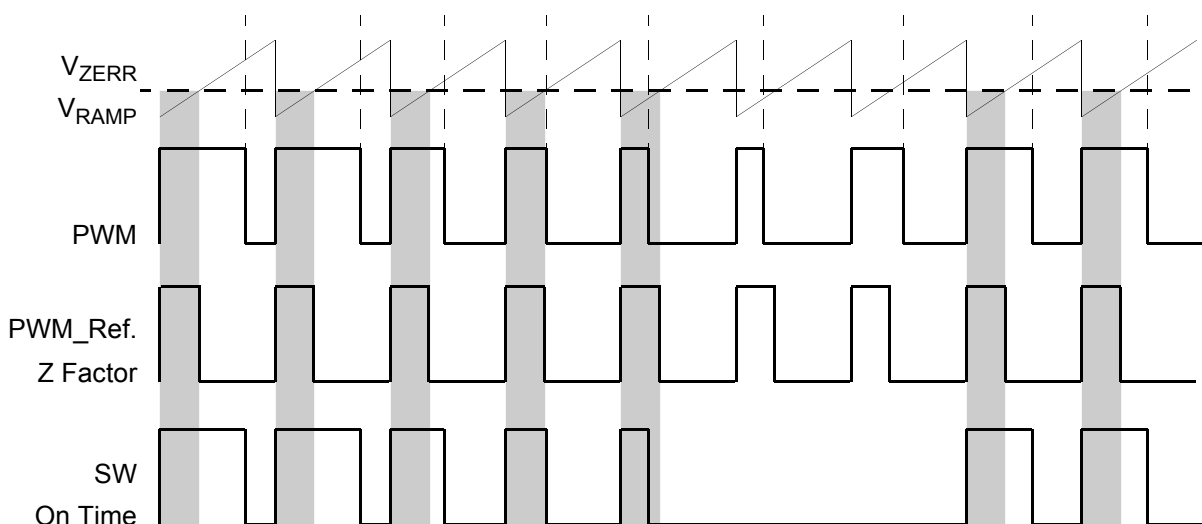


Figure 15. Z-mode Operation

#### SLEEPY Z-MODE OPERATION

To improve low current efficiency, the 34726 transitions into the Sleepy Z-mode at load currents of approximately 1.0mA and lower. This is accomplished by powering down

internal circuit blocks to lower the device's quiescent current. Additionally, the oscillator frequency drops to 250kHz and the low side switch is turned off to emulate the operation of an asynchronous buck converter.

### DETAILED FUNCTIONAL DEVICE OPERATION

#### OVER-CURRENT PROTECTION

The 34726 implements two layers of protection during overload conditions. The first is a current limit feature to prevent the device and external components from damage. When the peak inductor current reaches the over-current limit, nominally 450mA, the high side MOSFET turns off to provide cycle by cycle protection. If the over-current condition persists and the die temperature surpasses the over-temperature protection (OTP) threshold, this second layer of protection shuts down the device.

#### SHORT-CIRCUIT PROTECTION

When a short-circuit condition occurs on the output, typical regulators will tend to operate at maximum duty cycle. This condition can saturate the inductor and produce severe peak currents, resulting in damage to the device. The 34726 avoids this scenario by detecting output voltages below 0.5V. Upon detection, the part re-starts continuously until the short circuit condition is removed, or the part surpasses its OTP threshold.

## OVER-TEMPERATURE PROTECTION

To limit its operating temperature, the 34726 shuts down if the junction temperature of the switching MOSFET surpasses 140°C. If the junction temperature subsequently drops to 130°C, the 34726 re-starts.

## SOFT-START OPERATION

To limit the in-rush current, an internal timer controls the output voltage ramp after the part is enabled. The start-up time is internally set to approximately 2.0ms and is independent of input voltage, output voltage, or load current.

The soft-start sequence also occurs upon recovery from any fault condition.

## UNDER-VOLTAGE LOCK-OUT

The UVLO threshold is set to 2.7V for rising  $V_{IN}$ , and to 2.5V for falling  $V_{IN}$ . For a  $V_{OUT}$  of 3.3V, the  $V_{OUT}$  value will track  $V_{IN}$  below 3.6V until the 2.5V falling  $V_{IN}$  threshold is reached.

If the UVLO falling threshold is met, the part shuts down and will power up again with soft-start, when the UVLO rising threshold is surpassed.

## TYPICAL APPLICATIONS

### APPLICATION INFORMATION

#### INPUT CAPACITOR

The input capacitor is used to minimize the input voltage transient that may cause instability when the load transient current is high. Typically a 4.7µF X5R ceramic capacitor is sufficient for most applications.

#### OUTPUT CAPACITOR

For stable operation and low output voltage ripple, an X5R ceramic capacitor of 4.7µF minimum value is needed.

Depending on the load transient current, a larger capacitance may be required.

#### INDUCTOR SELECTION

A 4.7µH low DC resistance inductor is typically used for the 34726 to guarantee the system stable operation.

### TYPICAL APPLICATIONS

#### 1.2V OUTPUT DC/DC CONVERTOR

Figure 16 shows a typical application using 34726A.  $C_{IN}$  and  $C_{OUT}$  are typically 4.7µF/X5R ceramic capacitors. L1 is typically a 4.7µH low DC resistance inductor. The FB

connects to the output directly for monitoring the output voltage. Normally, the EN pin connects to the input supply directly to enable the regulator.

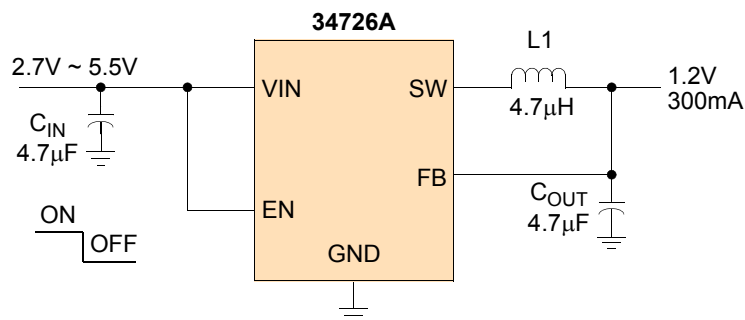
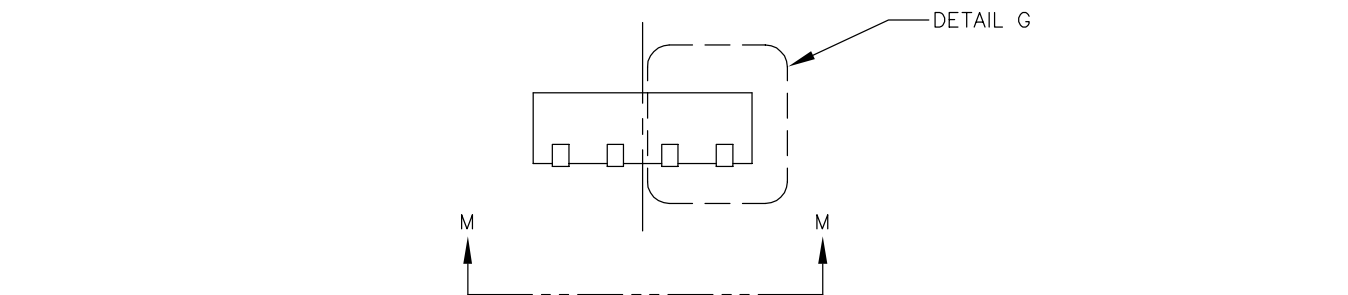
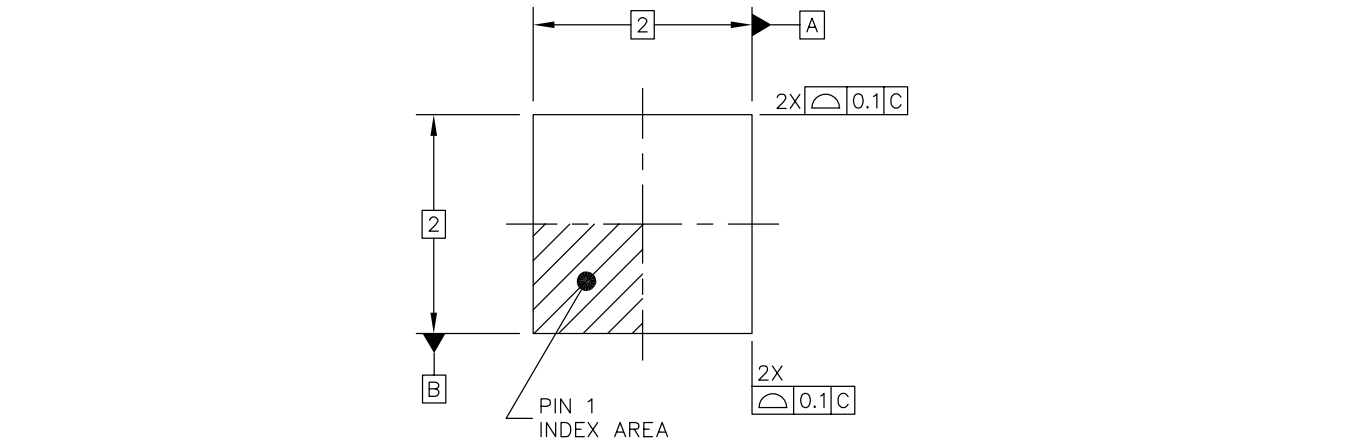


Figure 16. 1.2V/300mA DC/DC convertor

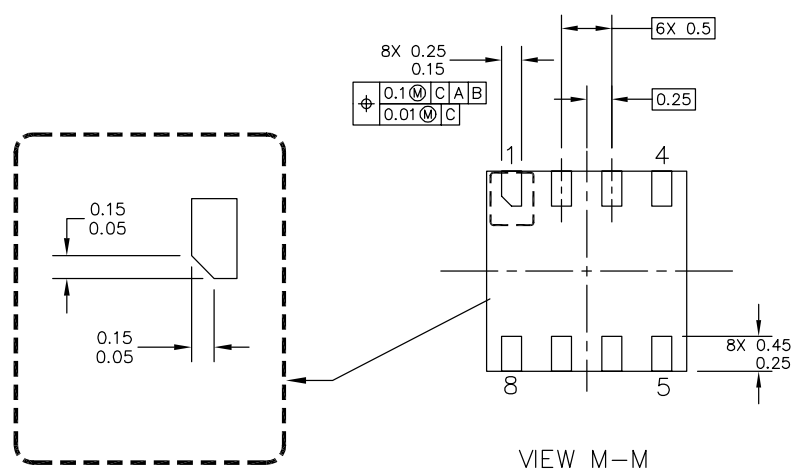
## PACKAGE DIMENSIONS

For the most current package revision, visit [www.freescale.com](http://www.freescale.com) and perform a keyword search using the “98A” listed below.

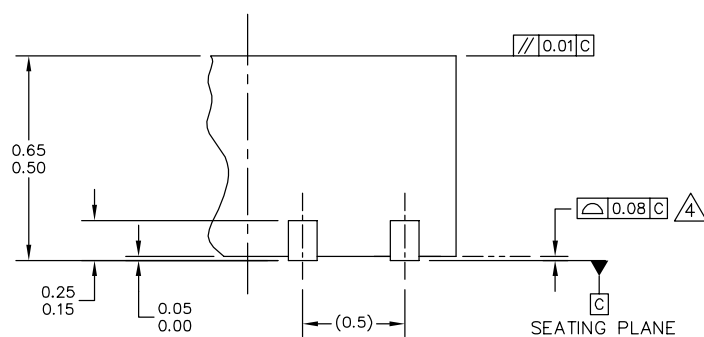


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<b>TITLE:</b> PLASTIC ULTRA-THIN FINE PITCH DUAL FLAT NON-LEADED (UDFN) PACKAGE, 8 TERMINAL, 2 X 2 X 0.65, 0.5 PITCH		DOCUMENT NO: 98ASA10787D		REV: A	
		CASE NUMBER: 1944-02		10 DEC 2007	
		STANDARD: NON-JEDEC			

FC SUFFIX  
12-PIN  
98ASA10787D  
REVISION A



PIN 1 BACKSIDE IDENTIFIER




DETAIL G  
VIEW ROTATED 90° CW

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		CASE NUMBER: 1944-02		10 DEC 2007	
		STANDARD: NON-JEDEC			

**FC SUFFIX**  
12-PIN  
98ASA10787D  
REVISION A



## NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS UF-PSON.
4.  COPLANARITY APPLIES TO LEADS.
5. MIN. METAL GAP SHOULD BE 0.2 MM.

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		STANDARD: NON-JEDEC			

**FC SUFFIX**  
12-PIN  
98ASA10787D  
REVISION A

## REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	5/2008	<ul style="list-style-type: none"><li>Initial Release</li></ul>

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