

High Speed Operational Amplifier

FEATURES

- *Guaranteed* 1.0mV Max. Input Offset Voltage
- *Guaranteed* 100,000 Min. Gain
- *Guaranteed* 50V/ μ s Slew Rate
- *Guaranteed* 20nA Max. Input Offset Current
- 15MHz Bandwidth
- Unity Gain Stable

APPLICATIONS

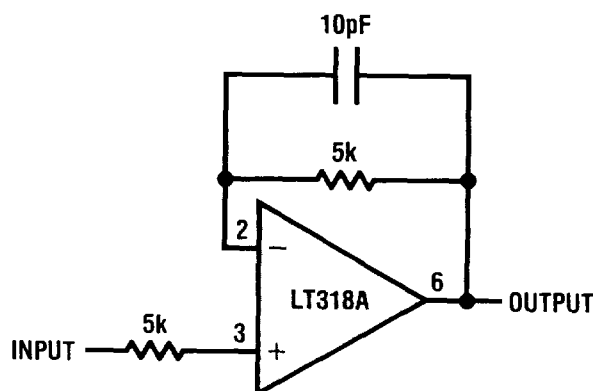
- Wideband Amplifiers
- High Frequency Absolute Value Circuits
- D/A Converter Amplifiers
- Fast Integrators

DESCRIPTION

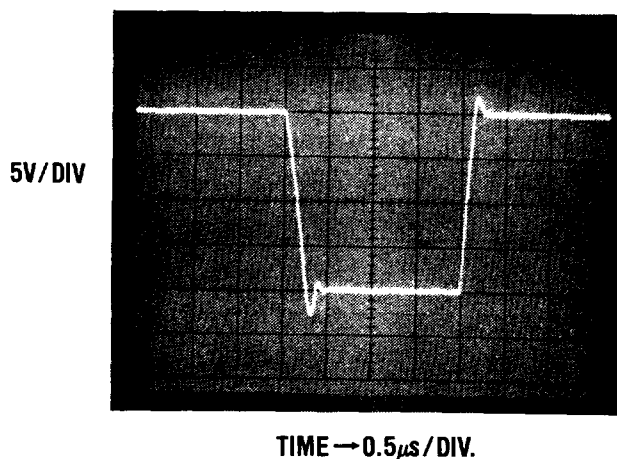
The LT118A is an improved version of the industry standard LM118. The LT118A features lower input offset voltage, lower input offset currents, higher gain and higher common mode and power supply rejection. Because of these enhancements, the LT118A will improve the accuracy of most applications. Unlike many wideband amplifiers, the LT118A is unity gain stable and has a slew rate of 50V/ μ s. When used in inverting amplifier applications, feedforward compensation can be used to achieve slew rates in excess of 150V/ μ s. Linear Technology Corporation's advanced processing techniques make the LT118A an ideal choice for high speed applications.

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Voltage Follower



Voltage Follower Pulse Response



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 20V$
Differential Input Current (Note 1)	$\pm 10mA$
Input Voltage (Note 2)	$\pm 20V$
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LT118A/LM118	$-55^{\circ}C$ to $125^{\circ}C$
LT318A/LM318	$0^{\circ}C$ to $70^{\circ}C$
Storage Temperature Range	
All Devices	$-65^{\circ}C$ to $150^{\circ}C$
Lead Temperature (Soldering, 10 sec.)	$300^{\circ}C$

PACKAGE/ORDER INFORMATION

TOP VIEW	ORDER PART NUMBER
	LT118AH LM118H LT318AH LM318H
METAL CAN H PACKAGE	
HERMETIC DIP J8 PACKAGE PLASTIC DIP N8 PACKAGE	LT118AJ8 LM118J8 LT318AJ8 LM318J8 LT318AN8 LM318N8

ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LT118A			LM118			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●		0.5 1	1 2		2 4 6		mV mV
I_{OS}	Input Offset Current		●		6 10	20 30		6 50 100		nA nA
I_B	Input Bias Current		●		120	250 500		120 250 500		nA nA
R_{IN}	Input Resistance			1	3		1	3		MΩ
A_V	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	●	100 100	500		50 25	200		V/mV V/mV
SR	Slew Rate	$V_S = \pm 15V$, $A_V = 1$		50	70		50	70		V/ μs
GBW	Gain Bandwidth Product	$V_S = \pm 15V$			15			15		MHz
	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 2k\Omega$	●	± 12	± 13		± 12	± 13		V
	Input Voltage Range	$V_S = \pm 15V$	●	± 11.5			± 11.5			V
I_S	Supply Current	$T_A = 125^{\circ}C$			5 4.5	8 7		5 4.5	8 7	mA mA
CMRR	Common Mode Rejection Ratio		●	86	100		80	100		dB
PSRR	Power Supply Rejection Ratio		●	86	100		70	80		dB

ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	LT318A TYP	MAX	MIN	LM318 TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		●	0.5	1 2		4	10 15	mV mV
I_{OS}	Input Offset Current		●	10	20 30		30	200 750	nA nA
I_B	Input Bias Current		●	150	250 500		150	500 750	nA nA
R_{IN}	Input Resistance			0.5	3		0.5	3	MΩ
A_V	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	●	100	500		25	200	V/mV V/mV
SR	Slew Rate	$V_S = \pm 15V$, $A_V = 1$		50	70		50	70	V/ μs
GBW	Gain Bandwidth Product	$V_S = \pm 15V$		15			15		MHz
	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 2k\Omega$	●	± 12	± 13		± 12	± 13	V
	Input Voltage Range	$V_S = \pm 15V$	●	± 11.5			± 11.5		V
I_S	Supply Current			5	10		5	10	mA
CMRR	Common Mode Rejection Ratio		●	86	100		70	100	dB
PSRR	Power Supply Rejection Ratio		●	86	100		65	80	dB

The ● denotes those specifications which apply over the full operating temperature range.

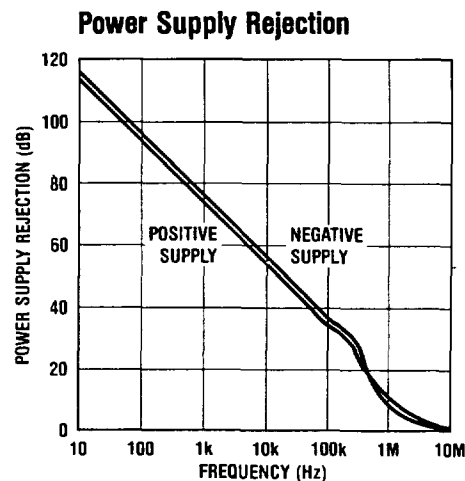
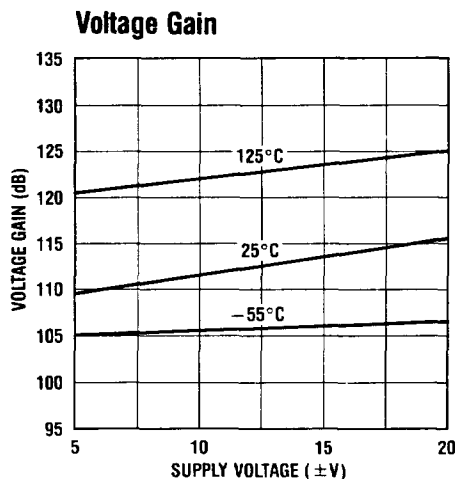
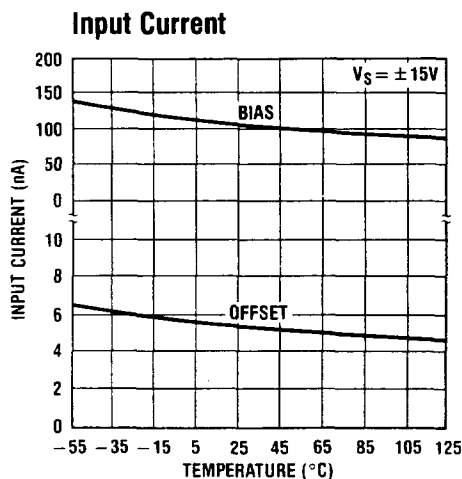
The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

Note 1: The inputs are shunted with back-to-back zeners for overvoltage protection. Excessive current will flow if a differential voltage greater than 5V is applied to the inputs.

Note 2: For supply voltages less than $\pm 15V$, the maximum input voltage is equal to the supply voltage.

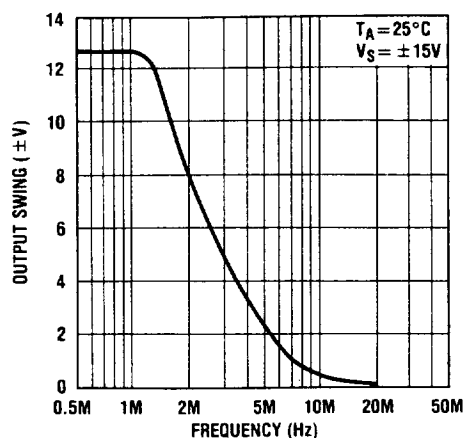
Note 3: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$. The power supplies must be bypassed with a $0.1\mu F$ or greater disc capacitor within 4 inches of the device.

TYPICAL PERFORMANCE CHARACTERISTICS

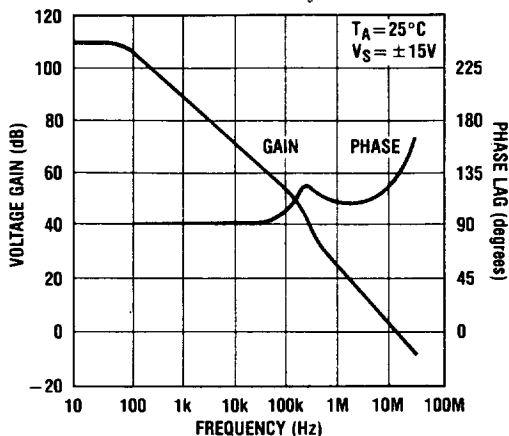


TYPICAL PERFORMANCE CHARACTERISTICS

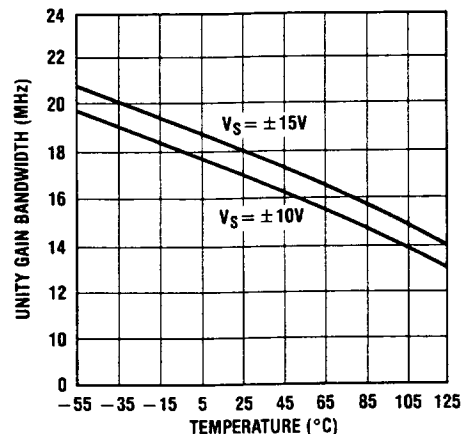
Large Signal Frequency Response



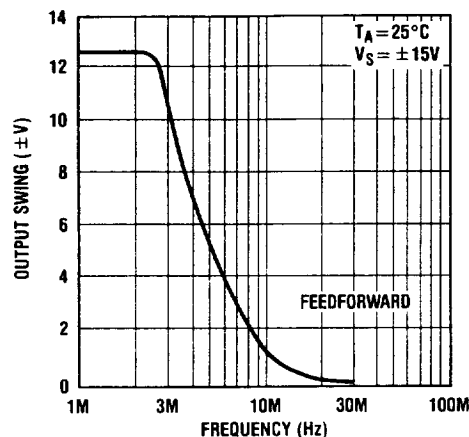
Open Loop Frequency Response



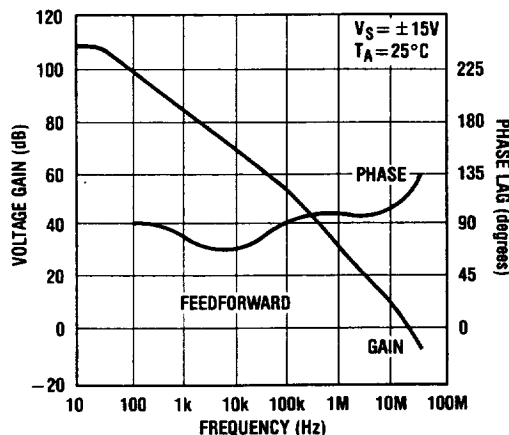
Unity Gain Bandwidth



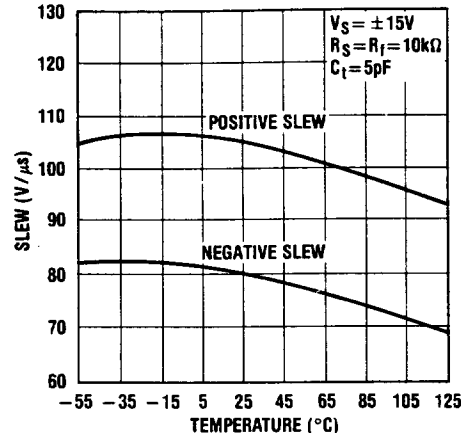
Large Signal Frequency Response



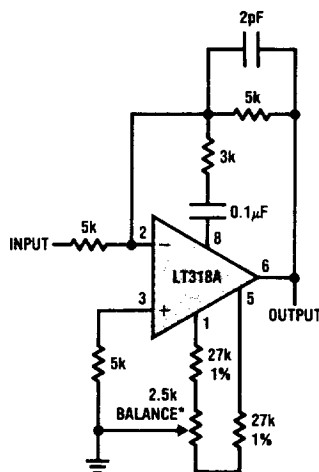
Open Loop Frequency Response



Voltage Follower Slew Rate

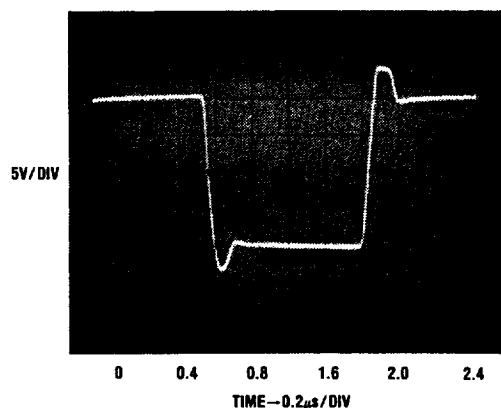


Feedforward Compensation for Slew Rates of $150V/\mu s$

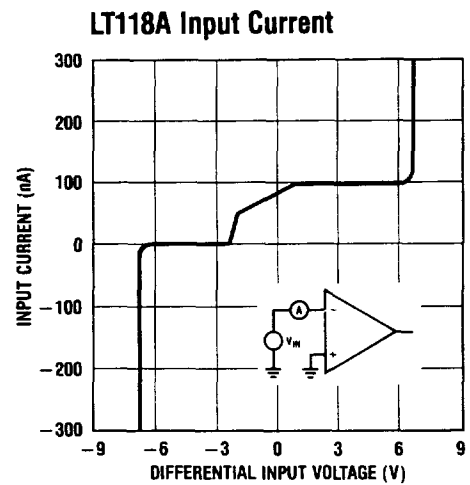
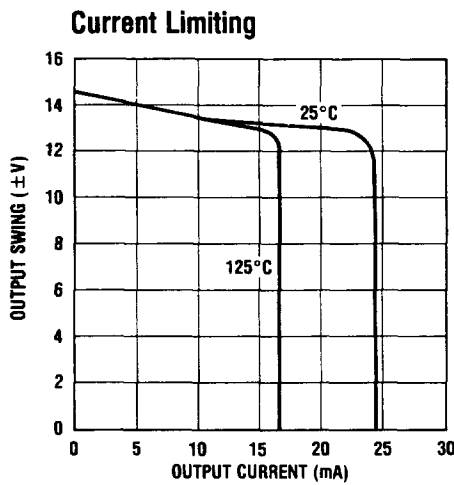
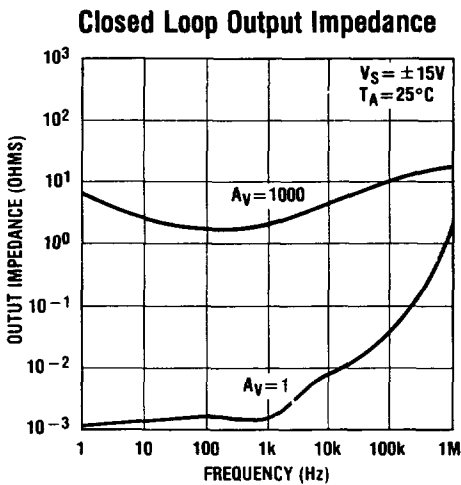
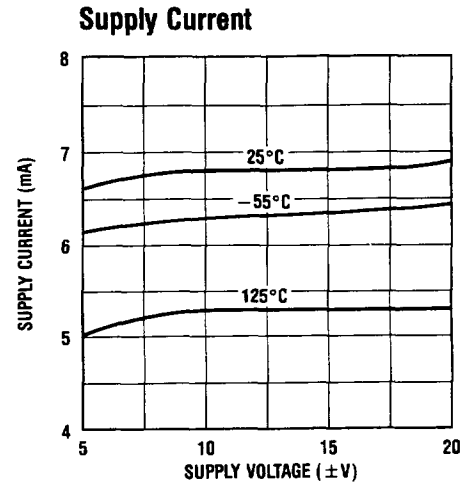
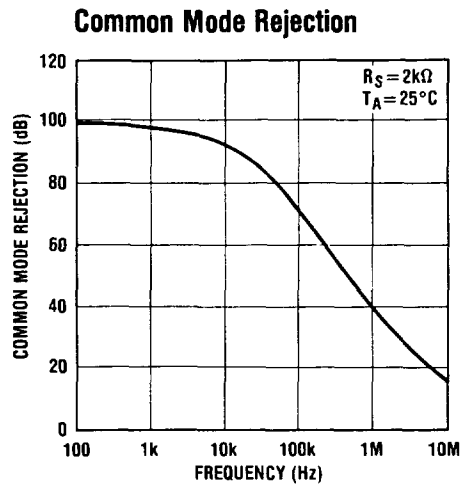
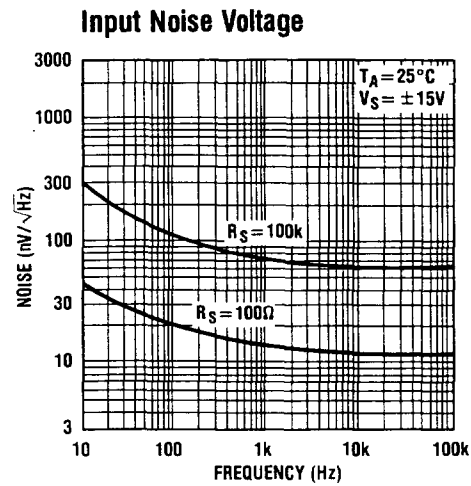


*BALANCE CIRCUIT NECESSARY FOR INCREASED SLEW RATE

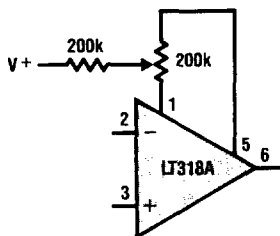
Pulse Response of Feedforward Inverter



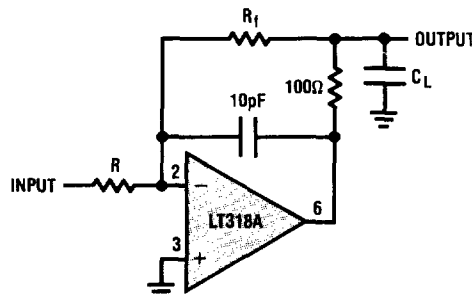
TYPICAL PERFORMANCE CHARACTERISTICS



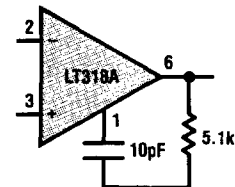
Offset Balancing



Isolating Large Capacitive Loads

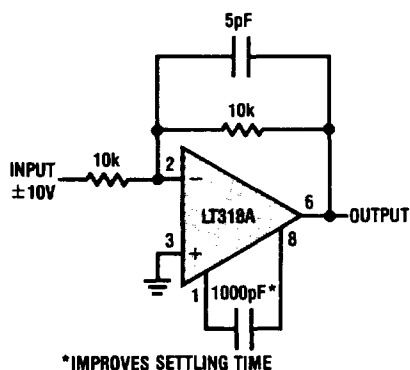


Overcompensation for Increased Stability

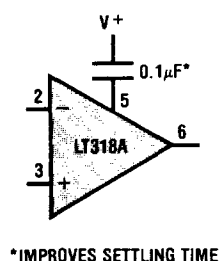


SETTLING TIME CIRCUITS

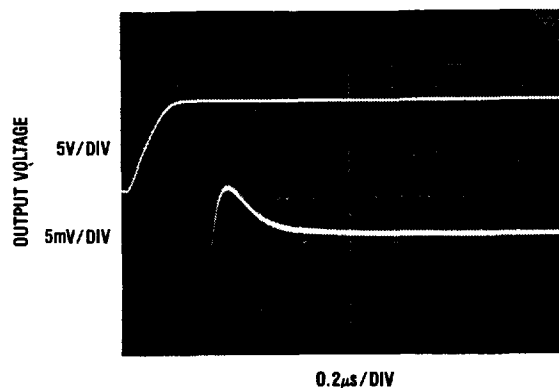
Settling Time Test Circuit



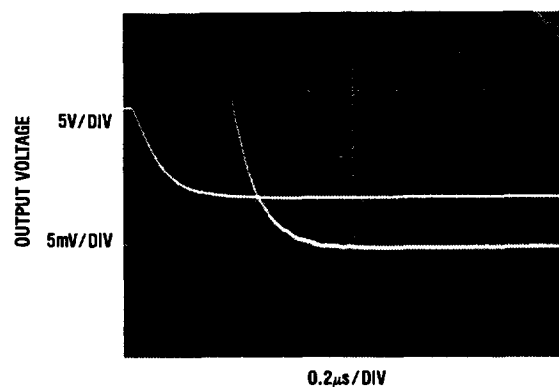
Alternate Compensation for Improved Settling Time



Settling Time



Settling Time



APPLICATIONS INFORMATION

Because of their wider bandwidth, the LT118A and LM118 operational amplifiers require more application care than most general purpose low frequency amplifiers. One of the most critical requirements is that power supplies should be bypassed with a 0.1μF (or larger) disc ceramic capacitor within an inch of the device. Also, stray capacitance at either the input or output can cause oscillation. While input capacitance can be compensated by placing a capacitor across the feedback resistor, load capacitance must be minimized or isolated as shown. Even the 50pF input capacitance of a 1X scope probe can alter the response of the device.

Settling time, an important parameter in many high speed amplifier applications, is difficult to measure and optimize. Settling time is very "application dependent" and is influenced by external components, layout and the amplifier. In general, the settling time to 0.01% can be minimized by using a circuit similar to that shown. In addition to the compensation network shown, a capacitor is needed across the feedback resistor to minimize ringing.

Power supply bypassing can also affect settling time. The amplifier has low power supply rejection ratio at high frequencies, so transients and ringing on the supply leads can appear at the output. Large (22μF) solid tantalum capacitors are preferred to minimize supply aberrations.

INPUT

R_{IN}
10k*

10k

1N4148

300pF

+15V

LT1008

2 7 6 4 3 1

10k

30pF

-15V

R_f
10k*

10pF

1000pF

+15V

LT1008

2 7 6 4 3 1

10k

-15V

OUTPUT

FULL POWER BANDWIDTH
SLEW RATE = 50V/ μ sec
SETTLING (10V STEP) =
BIAS CURRENT DC = 30 μ A
OFFSET DRIFT = 0.3 μ V/ $^{\circ}$ C
OFFSET VOLTAGE = 30 μ V

*1% METAL FILM

IC DIAGRAM

The diagram is a detailed schematic of the IC60000, a 10-bit 100ns CMOS DAC. It features a complex internal circuit with 30 transistors (Q1-Q30), 30 resistors (R1-R30), and 3 capacitors (C1-C3). The circuit is organized into several functional blocks: a reference current source (Q1-Q6, R1-R6), a 10-bit current mirror array (Q7-Q10, R7-R10), a 10-bit current mirror array (Q11-Q14, R11-R14), a 10-bit current mirror array (Q15-Q18, R15-R18), a 10-bit current mirror array (Q19-Q22, R19-R22), a 10-bit current mirror array (Q23-Q26, R23-R26), a 10-bit current mirror array (Q27-Q30, R27-R30), and a 10-bit current mirror array (Q31-Q34, R31-R34). The circuit is powered by a 5V supply (pin 1) and a 0V supply (pin 2). The output is taken from pin 3. The diagram is labeled 'IC60000' and '10-BIT 100NS CMOS DAC'.

J8 Package
8 Lead Hermetic DIP



T_{jmax} 150°C	θ_{ja} 150°C/W	θ_{jc} 45°C/W
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T_{jmax}	θ_{ja}
150°C	100°C/W

**N8 Package
8 Lead Plastic**



T_{jmax}	θ_{ja}
100°C	130°C/W