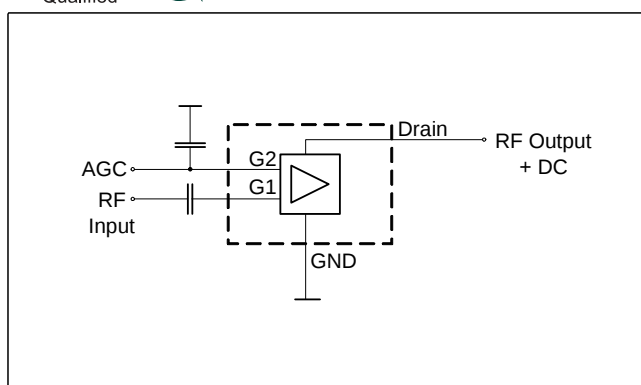
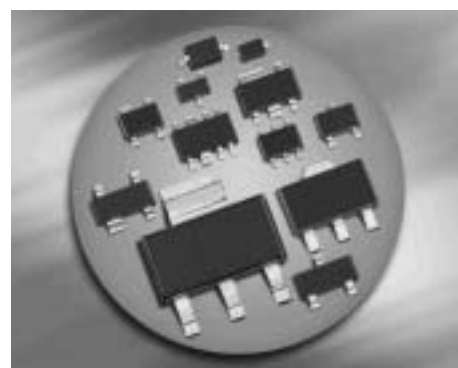


Silicon N-Channel MOSFET Tetrode

- For low noise, high gain controlled input stage up to 1 GHz
- Operating voltage 9 V
- Integrated biasing network
- Pb-free (RoHS compliant) package¹⁾
- Qualified according AEC Q101



ESD (Electrostatic discharge) sensitive device, observe handling precaution!

Type	Package	Pin Configuration						Marking
BF1009S	SOT143	1=S	2=D	3=G2	4=G1	-	-	JLs
BF1009SR	SOT143R	1=D	2=S	3=G1	4=G2	-	-	JLs

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	12	V
Continuous drain current	I_D	25	mA
Gate 1/ gate 2-source current	$\pm I_{G1/2SM}$	10	
Gate 1 (external biasing)	$+V_{G1SE}$	3	V
Total power dissipation $T_S \leq 76^\circ\text{C}$, BF1009S, BF1009SR	P_{tot}	200	mW
Storage temperature	T_{stg}	-55 ... 150	$^\circ\text{C}$
Channel temperature	T_{ch}	150	

¹⁾Pb-containing package may be available upon special request

Note:

It is not recommended to apply external DC-voltage on Gate 1 in active mode.

Thermal Resistance

Parameter	Symbol	Value	Unit
Channel - soldering point ¹⁾ BF1009S, BF1009SR	R_{thchs}	≤ 370	K/W

Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Drain-source breakdown voltage $I_D = 500 \mu A, V_{G1S} = 0, V_{G2S} = 0$	$V_{(BR)DS}$	12	-	-	V
Gate1-source breakdown voltage $+I_{G1S} = 10 \text{ mA}, V_{G2S} = 0, V_{DS} = 0$	$+V_{(BR)G1SS}$	9	-	12	
Gate2 source breakdown voltage $\pm I_{G2S} = 10 \text{ mA}, V_{G1S} = 0, V_{DS} = 0$	$\pm V_{(BR)G2SS}$	9	-	12	
Gate1-source leakage current $V_{G1S} = 6 \text{ V}, V_{G2S} = 0$	$+I_{G1SS}$	-	-	60	μA
Gate 2 source leakage current $\pm V_{G2S} = 8 \text{ V}, V_{G1S} = 0, V_{DS} = 0$	$\pm I_{G2SS}$	-	-	50	nA
Drain current $V_{DS} = 9 \text{ V}, V_{G1S} = 0, V_{G2S} = 6 \text{ V}$	I_{DSS}	-	-	500	μA
Operating current (selfbiased) $V_{DS} = 9 \text{ V}, V_{G2S} = 6 \text{ V}$	I_{DSO}	10	13	16	mA
Gate2-source pinch-off voltage $V_{DS} = 9 \text{ V}, I_D = 500 \mu A$	$V_{G2S(p)}$	-	0.9	-	V

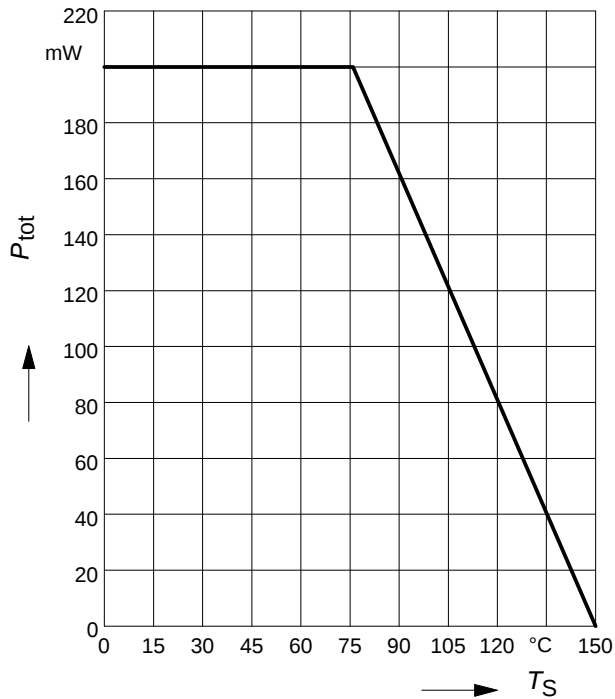
¹⁾For calculation of R_{thJA} please refer to Application Note Thermal Resistance

Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC Characteristics (verified by random sampling)					
Forward transconductance $V_{DS} = 9\text{ V}, V_{G2S} = 6\text{ V}$	g_{fs}	26	30	-	mS
Gate1 input capacitance $V_{DS} = 9\text{ V}, V_{G2S} = 6\text{ V}, f = 10\text{ MHz}$	C_{g1ss}	-	2.1	2.7	pF
Output capacitance $V_{DS} = 9\text{ V}, V_{G2S} = 6\text{ V}, f = 10\text{ MHz}$	C_{dss}	-	0.9	-	
Power gain (self biased) $V_{DS} = 9\text{ V}, V_{G2S} = 6\text{ V}, f = 800\text{ MHz}$	G_p	18	22	-	dB
Noise figure $V_{DS} = 9\text{ V}, V_{G2S} = 6\text{ V}, f = 800\text{ MHz}$	F	-	1.4	2.1	dB
Gain control range $V_{DS} = 9\text{ V}, V_{G2S} = 6 \dots 0\text{ V}, f = 800\text{ MHz}$	ΔG_p	40	50	-	

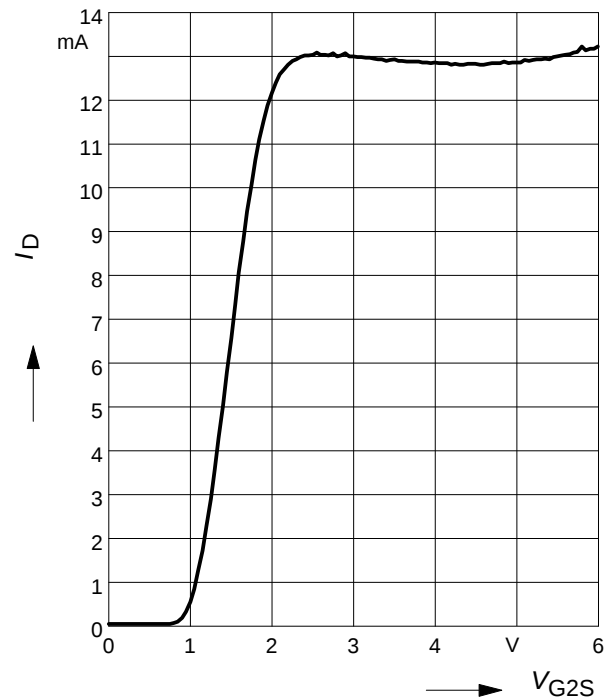
Total power dissipation $P_{\text{tot}} = f(T_S)$

BF1009S, BF1009SR



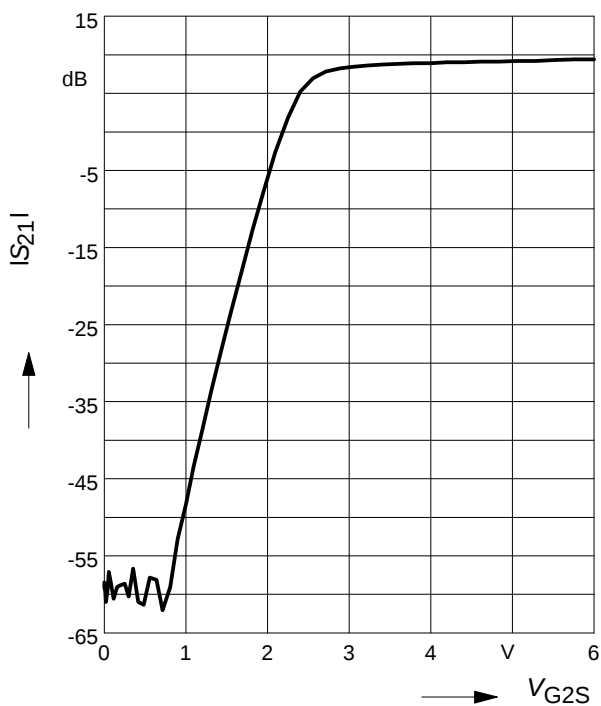
Drain current $I_D = f(V_{G2S})$

$V_{DS} = 9 \text{ V}$



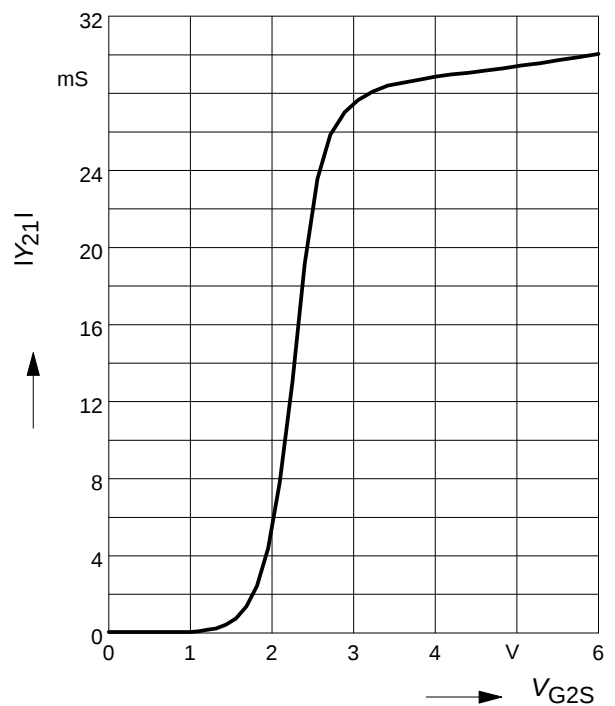
Insertion power gain

$|S_{21}|^2 = f(V_{G2S}), f = 200 \text{ MHz}$



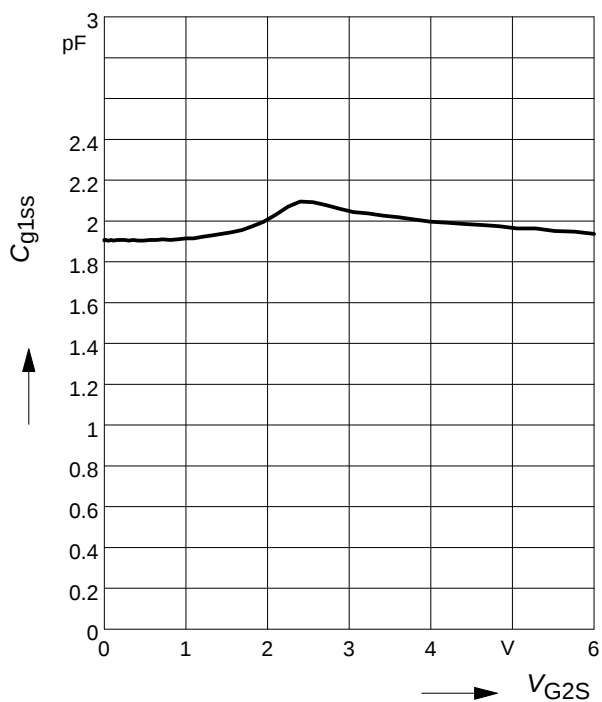
Forward transfer admittance

$|Y_{21}| = f(V_{G2S}), f = 200 \text{ MHz}$



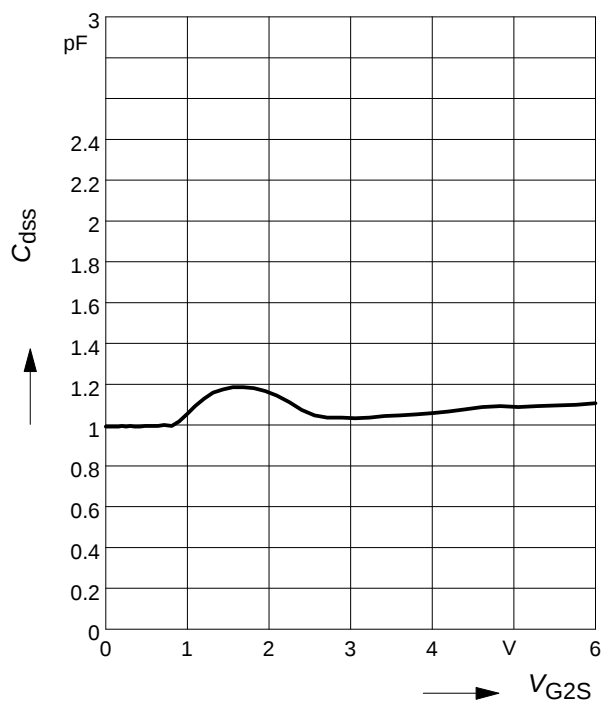
Gate 1 input capacitance $C_{g1ss} = f(V_{G2S})$

$f = 200 \text{ MHz}$



Output capacitance $C_{dss} = f(V_{G2S})$

$f = 200 \text{ MHz}$



Technical drawing of a 4-pin connector, showing a 3D perspective view and two cross-sectional views (A-A and B-B).

3D Perspective View:

- Overall width: 2.9 ± 0.1
- Pin spacing (center-to-center): 1.9
- Pin 1 and 2 are on the left, Pin 3 and 4 are on the right.
- Pin 1 and 2 are labeled with a "1" and "2" respectively.
- Pin 3 and 4 are labeled with a "3" and "4" respectively.
- Pin 1 and 2 are labeled with a "1" and "2" respectively.
- Pin 3 and 4 are labeled with a "3" and "4" respectively.

Cross-section A-A:

- Overall height: 1.3 ± 0.1
- Pin height: $0.8^{+0.1}_{-0.05}$
- Pin diameter: 0.25 M B
- Pin spacing (center-to-center): 1.7
- Pin 1 and 2 are labeled with a "1" and "2" respectively.
- Pin 3 and 4 are labeled with a "3" and "4" respectively.
- Pin 1 and 2 are labeled with a "1" and "2" respectively.
- Pin 3 and 4 are labeled with a "3" and "4" respectively.

Cross-section B-B:

- Overall width: 2.9 ± 0.1
- Pin spacing (center-to-center): 1.9
- Pin diameter: 0.25 M B
- Pin height: $0.4^{+0.1}_{-0.05}$
- Pin 1 and 2 are labeled with a "1" and "2" respectively.
- Pin 3 and 4 are labeled with a "3" and "4" respectively.
- Pin 1 and 2 are labeled with a "1" and "2" respectively.
- Pin 3 and 4 are labeled with a "3" and "4" respectively.

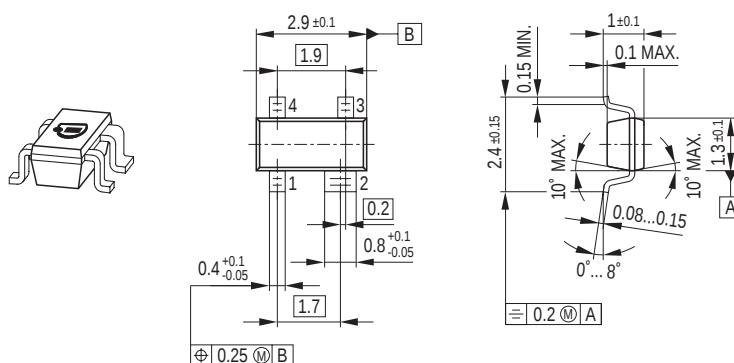
Diagram illustrating the marking on the BFP181 package:

- Manufacturer:** infineon
- Date code (YM):** 2005, June
- Pin 1:** Indicated by a line pointing to the first pin.
- Type code:** BFP181

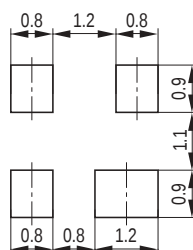
Technical drawing of a mechanical part showing top and side views with dimensions:

- Top View Dimensions:**
 - Overall width: 4
 - Overall height: 8
 - Distance from left edge to center of first hole: 3.15
 - Distance between centers of first and second holes: 2.6
 - Distance between centers of second and third holes: 2.6
 - Distance from center of third hole to right edge: 2.6
- Side View Dimensions:**
 - Overall thickness: 0.2
 - Distance from bottom edge to center of hole: 1.15
- Other Features:**
 - Three circular holes are shown in the top view.
 - A rectangular feature is shown on the left side of the top view.
 - A dimension line labeled "Pin 1" points to the left edge of the part.

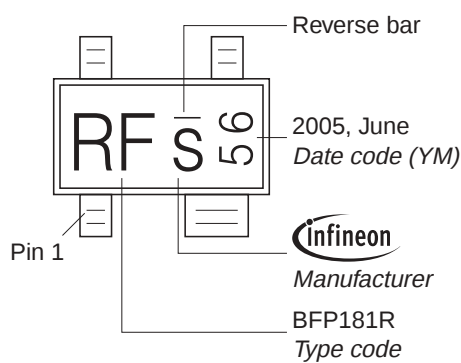
Package Outline



Foot Print

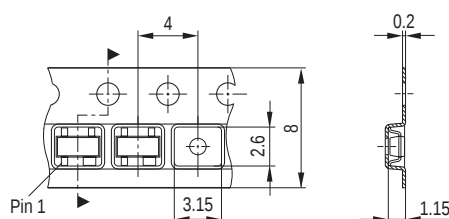


Marking Layout (Example)



Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
 Reel ø330 mm = 10.000 Pieces/Reel



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