

# SN54LV374A, SN74LV374A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS408A – APRIL 1998 – REVISED JUNE 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical  $V_{OLP}$  (Output Ground Bounce)**  
< 0.8 V at  $V_{CC}$ ,  $T_A = 25^\circ\text{C}$
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)**  
> 2 V at  $V_{CC}$ ,  $T_A = 25^\circ\text{C}$
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )**
- **Package Options Include Plastic Small-Outline (DW, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

## description

The 'LV374A devices are octal edge-triggered D-type flip-flops designed for 2-V to 5.5-V  $V_{CC}$  operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

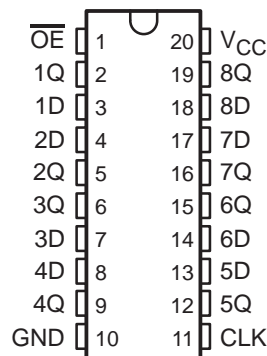
A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

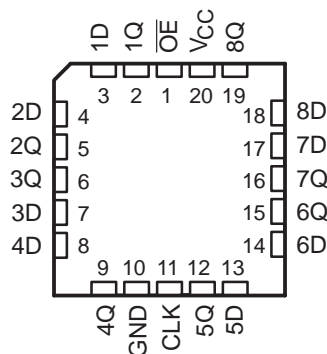
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LV374A is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74LV374A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54LV374A . . . J OR W PACKAGE  
SN74LV374A . . . DB, DGV, DW, NS, OR PW PACKAGE  
(TOP VIEW)



SN54LV374A . . . FK PACKAGE  
(TOP VIEW)



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**TEXAS  
INSTRUMENTS**

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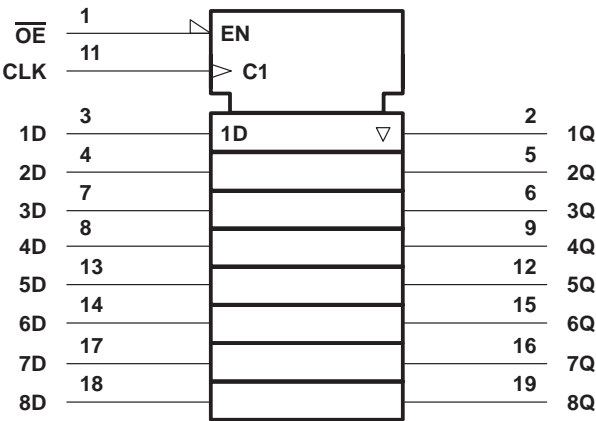
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OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS  
WITH 3-STATE OUTPUTS

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FUNCTION TABLE  
(each flip-flop)

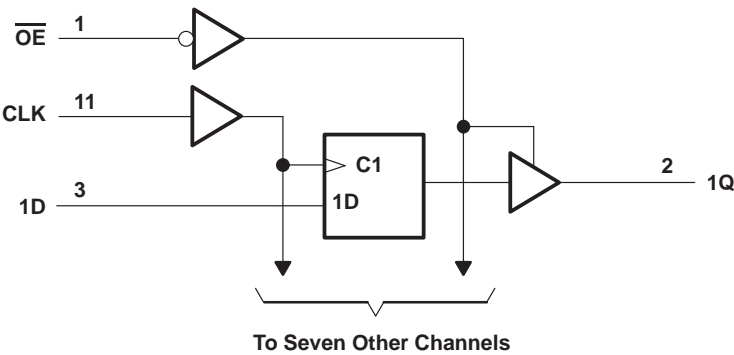
INPUTS			OUTPUT Q
$\overline{\text{OE}}$	CLK	D	
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	L	X	$Q_0$
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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Supply voltage range, $V_{CC}$	.....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	.....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Notes 1 and 2)	.....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	.....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	.....	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	.....	$\pm 35$ mA
Continuous current through $V_{CC}$ or GND	.....	$\pm 70$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3):		
DB package	.....	115°C/W
DGV package	.....	146°C/W
DW package	.....	97°C/W
NS package	.....	100°C/W
PW package	.....	128°C/W
Storage temperature range, $T_{stg}$	.....	-65°C to 150°C

NOTES:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JEDEC 51.

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## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

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#### recommended operating conditions (see Note 4)

			SN54LV374A		SN74LV374A		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage		2	5.5	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		1.5		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.7		V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.7		V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.7		V <sub>CC</sub> × 0.7		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5		0.5		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.3		V <sub>CC</sub> × 0.3		
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.3		V <sub>CC</sub> × 0.3		
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.3		V <sub>CC</sub> × 0.3		
V <sub>I</sub>	Input voltage		0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
		3-state	0	5.5	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V	−50		−50		μA
		V <sub>CC</sub> = 2.3 V to 2.7 V	−2		−2		mA
		V <sub>CC</sub> = 3 V to 3.6 V	−8		−8		
		V <sub>CC</sub> = 4.5 V to 5.5 V	−16		−16		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V	50		50		μA
		V <sub>CC</sub> = 2.3 V to 2.7 V	2		2		mA
		V <sub>CC</sub> = 3 V to 3.6 V	8		8		
		V <sub>CC</sub> = 4.5 V to 5.5 V	16		16		
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V <sub>CC</sub> = 3 V to 3.6 V	0	100	0	100	
		V <sub>CC</sub> = 4.5 V to 5.5 V	0	20	0	20	
T <sub>A</sub>	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LV374A			SN74LV374A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = −50 μA	2 V to 5.5 V	V <sub>CC</sub> −0.1			V <sub>CC</sub> −0.1			V
	I <sub>OH</sub> = −2 mA	2.3 V	2			2			
	I <sub>OH</sub> = −8 mA	3 V	2.48			2.48			
	I <sub>OH</sub> = −16 mA	4.5 V	3.8			3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I <sub>OL</sub> = 2 mA	2.3 V	0.4			0.4			
	I <sub>OL</sub> = 8 mA	3 V	0.44			0.44			
	I <sub>OL</sub> = 16 mA	4.5 V	0.55			0.55			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V	±1			±1			μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V	±5			±5			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	20			20			μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0 V	5			5			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	2.9			2.9			pF

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**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)**

		$T_A = 25^\circ\text{C}$		SN54LV374A		SN74LV374A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_W$	Pulse duration, CLK high or low	6		7		7		ns
$t_{su}$	Setup time, data before CLK $\uparrow$	5		5.5		5.5		ns
$t_h$	Hold time, data after CLK $\uparrow$	2.5		2.5		2.5		ns

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)**

		$T_A = 25^\circ\text{C}$		SN54LV374A		SN74LV374A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_W$	Pulse duration, CLK high or low	5		5.5		5.5		ns
$t_{su}$	Setup time, data before CLK $\uparrow$	4		4		4		ns
$t_h$	Hold time, data after CLK $\uparrow$	2		2		2		ns

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

		$T_A = 25^\circ\text{C}$		SN54LV374A		SN74LV374A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_W$	Pulse duration, CLK high or low	5		5		5		ns
$t_{su}$	Setup time, data before CLK $\uparrow$	3		3		3		ns
$t_h$	Hold time, data after CLK $\uparrow$	2		2		2		ns

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV374A		SN74LV374A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			$C_L = 15\text{ pF}^*$	60	105		50		50		MHz
			$C_L = 50\text{ pF}$	50	85		40		40		
$t_{pd}^*$	CLK	Q	$C_L = 15\text{ pF}$	9.7	16.3		1	19	1	19	ns
$t_{en}^*$	$\overline{OE}$	Q		8.9	15.9		1	19	1	19	
$t_{dis}^*$	$\overline{OE}$	Q		6.3	12.6		1	15	1	15	
$t_{pd}$	CLK	Q	$C_L = 50\text{ pF}$	11.8	19.3		1	23	1	23	ns
$t_{en}$	$\overline{OE}$	Q		10.9	18.8		1	22	1	22	
$t_{dis}$	$\overline{OE}$	Q		8.2	17.3		1	19	1	19	
$t_{sk(o)}^\dagger$					2					2	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

# SN54LV374A, SN74LV374A

## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV374A		SN74LV374A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}^*$	80	150		70		70		MHz
			$C_L = 50\text{ pF}$	55	110		50		50		
$t_{\text{pd}}^*$	CLK	Q	$C_L = 15\text{ pF}$		6.8	12.7	1	15	1	15	ns
$t_{\text{en}}^*$	$\overline{\text{OE}}$	Q			6.3	11	1	13	1	13	
$t_{\text{dis}}^*$	$\overline{\text{OE}}$	Q			4.7	10.5	1	12.5	1	12.5	
$t_{\text{pd}}$	CLK	Q	$C_L = 50\text{ pF}$		8.3	16.2	1	18.5	1	18.5	ns
$t_{\text{en}}$	$\overline{\text{OE}}$	Q			7.7	14.5	1	16.5	1	16.5	
$t_{\text{dis}}$	$\overline{\text{OE}}$	Q			5.9	14	1	16	1	16	
$t_{\text{sk(o)}}^\dagger$					1.5					1.5	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV374A		SN74LV374A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}^*$	130	205		110		110		MHz
			$C_L = 50\text{ pF}$	85	170		75		75		
$t_{\text{pd}}^*$	CLK	Q	$C_L = 15\text{ pF}$		4.9	8.1	1	9.5	1	9.5	ns
$t_{\text{en}}^*$	$\overline{\text{OE}}$	Q			4.6	7.6	1	9	1	9	
$t_{\text{dis}}^*$	$\overline{\text{OE}}$	Q			3.4	6.8	1	8	1	8	
$t_{\text{pd}}$	CLK	Q	$C_L = 50\text{ pF}$		5.9	10.1	1	11.5	1	11.5	ns
$t_{\text{en}}$	$\overline{\text{OE}}$	Q			5.5	9.6	1	11	1	11	
$t_{\text{dis}}$	$\overline{\text{OE}}$	Q			4	8.8	1	10	1	10	
$t_{\text{sk(o)}}^\dagger$					1					1	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

noise characteristics,  $V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER		SN74LV374A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.57	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.53	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		2.88		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage		0.99		V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		$V_{CC}$	TYP	UNIT
$C_{\text{pd}}$	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	3.3 V	21.1	pF
				5 V	22.8	

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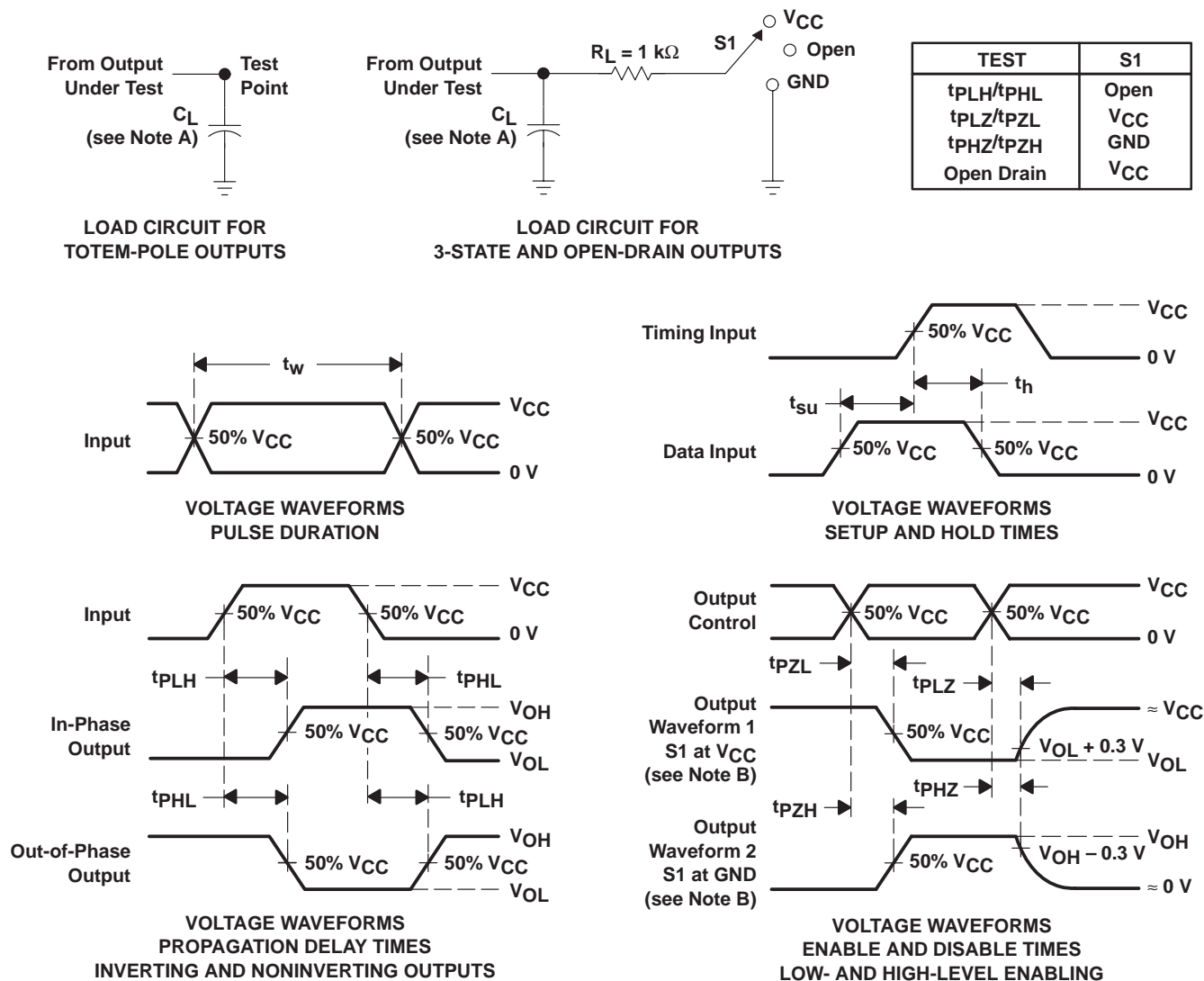


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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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