

# SN74AS304 OCTAL DIVIDE-BY-2 CIRCUIT/CLOCK DRIVER

D3555, JULY 1990

- Maximum Output Skew of 1 ns
- Maximum Pulse Skew of 1 ns
- Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include Plastic "Small Outline" Packages, and Standard Plastic 300-mil DIPs

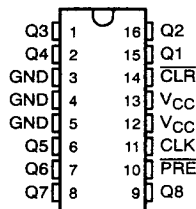
## description

The SN74AS304 contains eight flip-flops designed to have low skew between outputs. The eight outputs (in-phase with CLK) toggle on successive CLK pulses.  $\overline{PRE}$  and  $\overline{CLR}$  pins are provided to set the Q outputs high or low independent of the CLK input.

The SN74AS304 has output and pulse skew parameters  $t_{sk(o)}$  and  $t_{sk(p)}$  to ensure performances as a clock driver when a divide-by-two function is required.

The SN74AS304 is characterized for operation from 0°C to 70°C.

D OR N PACKAGE  
(TOP VIEW)

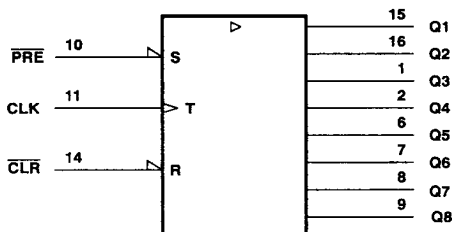


FUNCTION TABLE

INPUTS			OUTPUTS Q1-Q8
$\overline{CLR}$	$\overline{PRE}$	CLK	
L	H	X	L
H	L	X	H
L	L	X	$L^\dagger$
H	H	$\uparrow$	$\overline{Q}_0$
H	H	L	$Q_0$

$^\dagger$  This configuration will not persist when  $\overline{PRE}$  or  $\overline{CLR}$  returns to its inactive (high) level.

## logic symbol $^\ddagger$



$^\ddagger$  This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

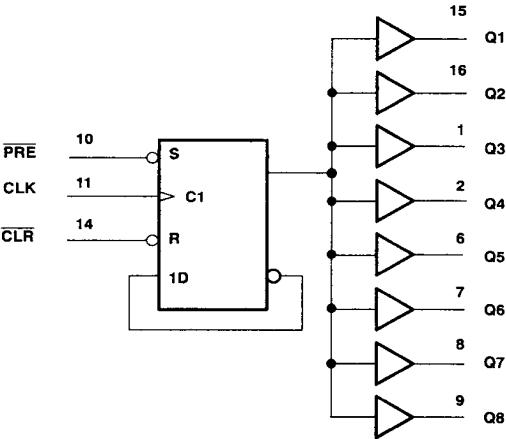
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SN74AS304

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	– 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level output current			– 24	mA
$I_{OL}$	Low-level output current			48	mA
$T_A$	Operating free-air temperature	0		70	°C

# SN74AS304

## OCTAL DIVIDE-BY-2 CIRCUIT/CLOCK DRIVER

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.5 \text{ V}$	$I_I = -18 \text{ mA}$			-1.2	V
$V_{OH}$	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -2 \text{ mA}$	$V_{CC}^{-2}$			V
	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -24 \text{ mA}$	2	2.8		
$V_{OL}$	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 48 \text{ mA}$		0.3	0.5	V
$I_I$	$V_{CC} = 5.5 \text{ V}$	$V_I = 7 \text{ V}$			0.1	mA
$I_{IH}$	$V_{CC} = 5.5 \text{ V}$	$V_I = 2.7 \text{ V}$			20	$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.5 \text{ V}$	$V_I = 0.4 \text{ V}$			-0.5	mA
$I_{O}^{\dagger}$	$V_{CC} = 5.5 \text{ V}$	$V_O = 2.25 \text{ V}$	-50		-150	mA
$I_{CC}$	$V_{CC} = 5.5 \text{ V}$	See Note 1		45	75	mA

† All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

NOTE 1:  $I_{CC}$  is measured with CLK and PRE grounded, then with CLK and CLR grounded.

### timing requirements (see Note 2)

PARAMETER		MIN	NOM	MAX	UNIT
$f_{\text{clock}}$	Clock frequency	0		80	MHz
$t_w$	Pulse duration	CLK high	4		ns
		CLK low	6		
		CLR or PRE low	5		
$t_{su}$	Setup time before CLK†	CLR or PRE inactive	6		ns

### switching characteristics over recommended operating free-air temperature range (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$f_{\text{max}}^{\S}$				80			MHz
$t_{PLH}$	CLK	Q	$R_L = 500 \Omega$ , $C_L = 50 \text{ pF}$	2	6	9	ns
$t_{PHL}$				2	6	9	
$t_{PLH}$	PRE or CLR	Q	$R_L = 500 \Omega$ , $C_L = 50 \text{ pF}$	3	7	12	ns
$t_{PHL}$				3	7	12	
$t_{sk(o)}$	CLK	Q	$R_L = 500 \Omega$ , $C_L = 10 \text{ pF to } 30 \text{ pF}$			1	ns
$t_{sk(p)}$	CLK	Q1, Q8	$R_L = 500 \Omega$ , $C_L = 10 \text{ pF to } 30 \text{ pF}$			1	ns
		Q2 to Q7				1.5	
$t_r$						4.5	ns
$t_f$						3.5	ns

† All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§  $f_{\text{max}}$  minimum values are at  $C_L = 0 \text{ to } 30 \text{ pF}$ .

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.