

**PRELIMINARY****CY62256V****32K x 8 Static RAM****Features**

- **Low voltage range:**
 - 2.7V – 3.6V (62256V)
 - 2.3V – 2.7V (62256V25)
 - 1.6V – 2.0V (62256V18)
- **Low active power and standby power**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

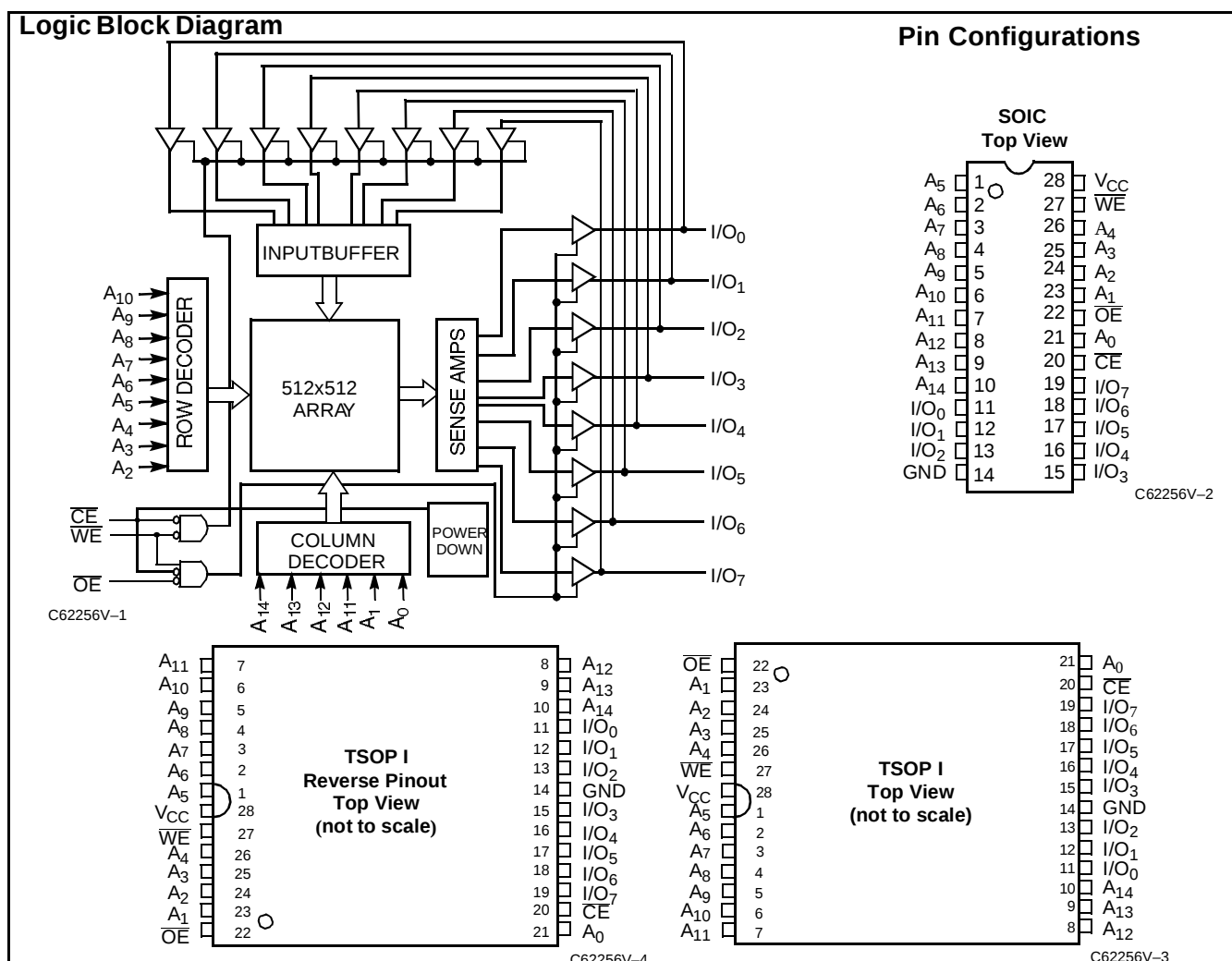
Functional Description

The CY62256V family is composed of three high-performance CMOS static RAM's organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and three-state driv-

ers. These devices have an automatic power-down feature, reducing the power consumption by over 99% when deselected. The CY62256V family is available in the standard 450-mil-wide (300-mil body width) SOIC, TSOP, and reverse TSOP packages.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.





Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to + 150°C

Ambient Temperature with
Power Applied 0°C to + 70°C

Supply Voltage to Ground Potential
(Pin 28 to Pin 14) -0.5V to + 4.6V

DC Voltage Applied to Outputs
in High Z State^[1] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5V$

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	1.6V to 3.6V
Industrial	-40°C to +85°C	1.6V to 3.6V

Note:

1. V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.

Product Portfolio

Product	Vcc Range			Speed	Power Dissipation (LL Devices)			
					Operating(I_{CC})		Standby (I_{SB2})	
	Min.	Typ.	Max.		Typical	Maximum	Typical	Maximum
CY62256V	2.7V	3.0	3.6V	70 ns	11 mA	30 mA	0.1 uA	5 uA
CY62256V25	2.3V	2.5V	2.7V	100 ns	9 mA	15 mA	0.1 uA	4 uA
CY62256V18	1.6V	1.8V	2.0V	200 ns	5 mA	10 mA	0.1 uA	3 uA

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62256V-70			Unit
			Min.	Typ. ^[2]	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -1.0 \text{ mA}$	2.4			V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 2.1 \text{ mA}$			0.4	V
V_{IH}	Input HIGH Voltage		2.2		$V_{CC} + 0.3V$	V
V_{IL}	Input LOW Voltage		-0.5		0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1		+1	uA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled	-1		+1	uA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$		11	30	mA
I_{SB1}	Automatic CE Power-Down Current— TTL Inputs	Max. V_{CC} , $\overline{CE} \geq V_{IH}, V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{MAX}$		100	300	uA
I_{SB2}	Automatic CE Power-Down Current— CMOS Inputs	Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V, f = 0$		0.1	50	uA
					5	uA
					10	uA

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62256V25-100			Unit
			Min.	Typ. ^[2]	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -0.1 \text{ mA}$	2			V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 0.1 \text{ mA}$			0.4	V
V_{IH}	Input HIGH Voltage		1.7		$V_{CC} + 0.3V$	V
V_{IL}	Input LOW Voltage		-0.3		0.7	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1		+1	uA

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions			CY62256V25-100			Unit
					Min.	Typ. ^[2]	Max.	
I _{OZ}	Output Leakage Cur- rent	GND ≤ V _O ≤ V _{CC} , Output Disabled			−1		+1	uA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Com'l	Std/L /LL		14	23	mA
I _{SB1}	Automatic CE Pow- er-Down Current— TTL Inputs	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Com'l	Std/L /LL		75	225	uA
I _{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$ V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0	Com'l	Std/L	0.1	40	uA	
				LL		4	uA	
			Ind'l	LL			8	uA

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			CY62256V18-200			Unit	
					Min.	Typ. ^[2]	Max.		
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = −0.1 mA			0.8*V _{cc}			V	
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 0.1 mA					0.2	V	
V _{IH}	Input HIGH Voltage				0.7*V _{cc}		V _{CC} +0.3V	V	
V _{IL}	Input LOW Voltage				−0.5		0.2*V _{cc}	V	
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}			−1		+1	uA	
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled			−1		+1	uA	
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Com'l	Std/L /LL		10	17	mA	
I _{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Com'l	Std/L /LL		56	165	uA	
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0	Com'l	Std/L		0.1	30	uA	
				LL				3	uA
			Ind'l	LL				6	uA

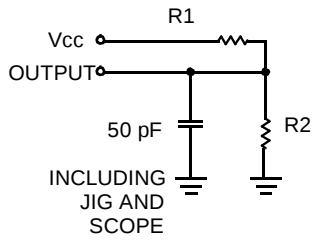
Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ C$, $f = 1 \text{ MHz}$, $V_{CC} = 3.0V$	6	pF
C_{OUT}	Output Capacitance		8	pF

Notes:

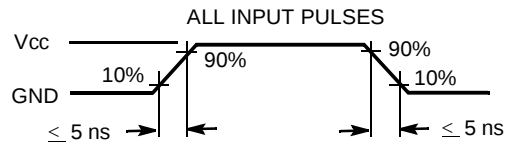
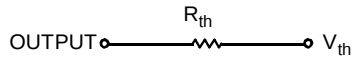
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC} \text{ Typ.}$, $T_A = 25^\circ C$, and $t_{AA} = 70 \text{ ns}$.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



C62256V-5

Equivalent to: THÉVENIN EQUIVALENT



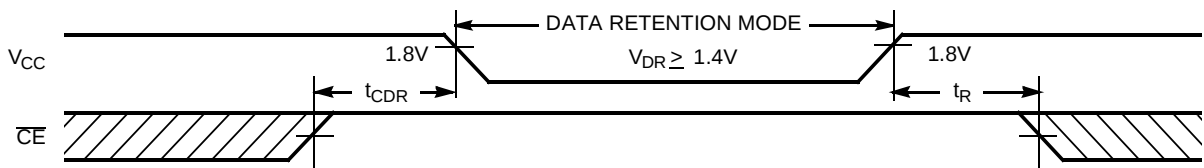
C62256V-6

AC Test Load			
Vcc	3.3 V	2.5V	1.8V
R1	1103	16.6K	13.6K
R2	1554	15.4K	11.4K
RTH	645	8K	6.2K
VTH	1.75V	1.2V	0.82V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description		Conditions ^[4]	Min.	Typ. ^[2]	Max.	Unit
V _{DR}	V _{CC} for Data Retention			1.4			V
I _{CCDR}	Data Retention Current	Coml	Std/L	V _{CC} = 1.6 CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		30	uA
			LL		0.1	3	uA
		Ind.	LL			6	uA
t _{CDR} ^[3]	Chip Deselect to Data Retention Time			0			ns
t _R ^[3]	Operation Recovery Time			t _{RC}			ns

Data Retention Waveform



C62256V-7

Switching Characteristics Over the Operating Range^[5]

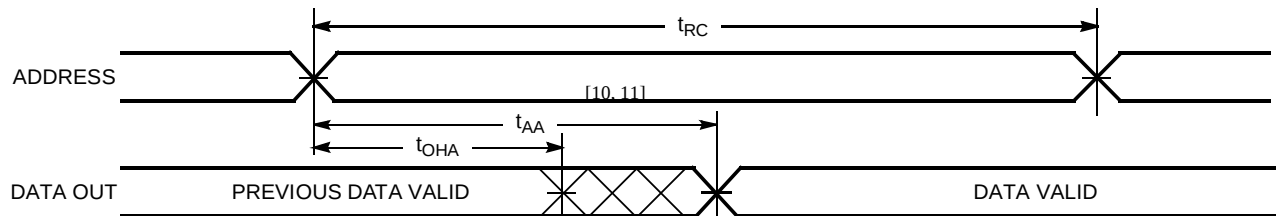
Parameter	Description	CY62256V-70		CY62256V25-100		CY62256V18-200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	70		100		200		ns
t _{AA}	Address to Data Valid		70		100		200	ns
t _{OHA}	Data Hold from Address Change	10		10		10		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		70		100		200	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		35		75		125	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z ^[6]	5		5		10		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[6, 7]		25		50		75	ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[6]	10		10		10		ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[6, 7]		25		50		75	ns
t _{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power-Down		70		100		200	ns
WRITE CYCLE ^[8,9]								
t _{WC}	Write Cycle Time	70		100		200		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	60		90		180		ns
t _{AW}	Address Set-Up to Write End	60		90		180		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	50		80		160		ns
t _{SD}	Data Set-Up to Write End	30		60		100		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[6, 7]		25		50		100	ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[6]	10		10		10		ns

Notes:

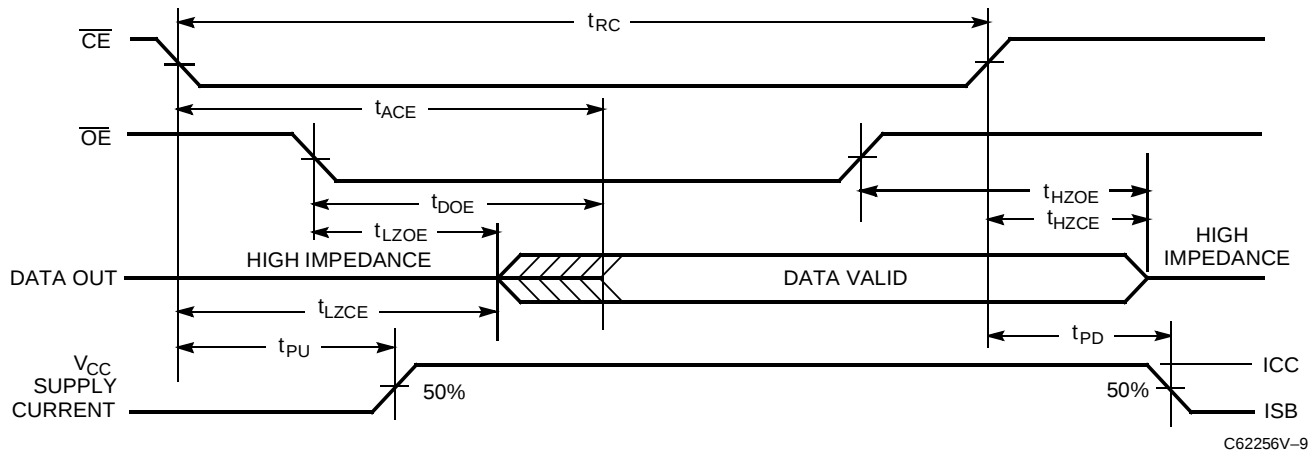
4. No input may exceed $V_{CC}+0.3V$.
5. Test conditions assume signal transition time of 5 ns or less timing reference levels of $V_{CC}/2$, input pulse levels of 0 to V_{CC} , and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.

Switching Waveforms

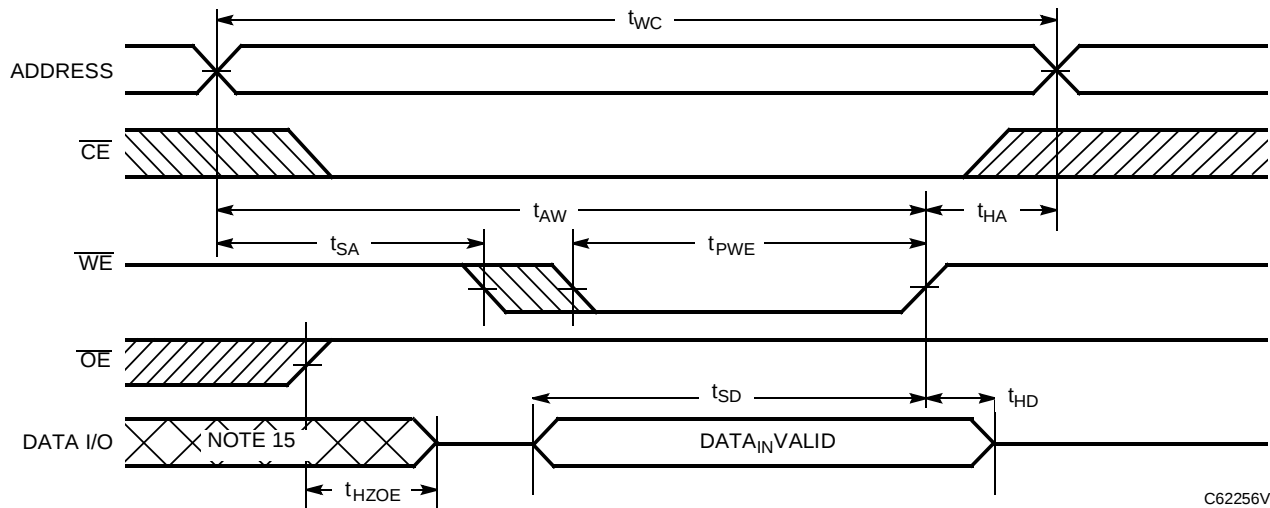
Read Cycle No. 1^[10, 11]



C62256V-8

Switching Waveforms (continued)
Read Cycle No. 2 ^[11, 12]


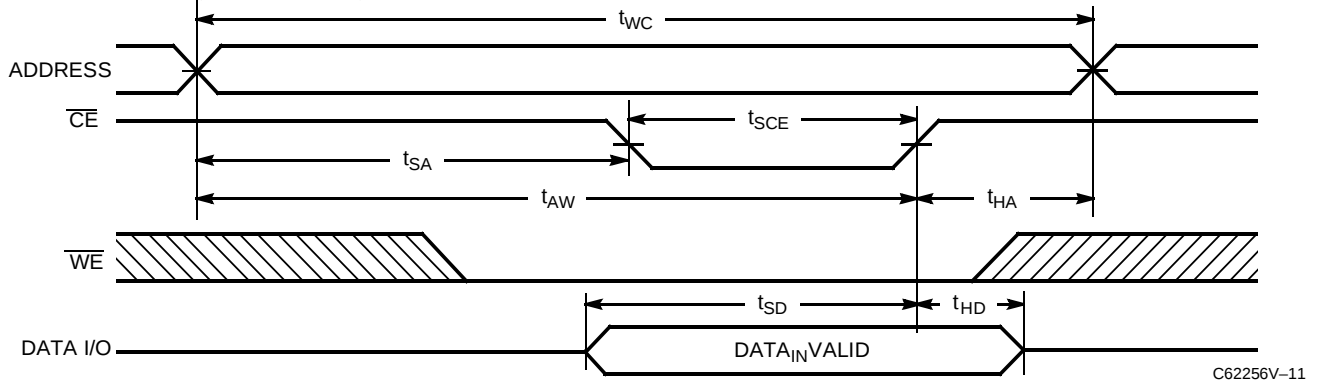
C62256V-9

Write Cycle No. 1 (WE Controlled) ^[8, 13, 14]


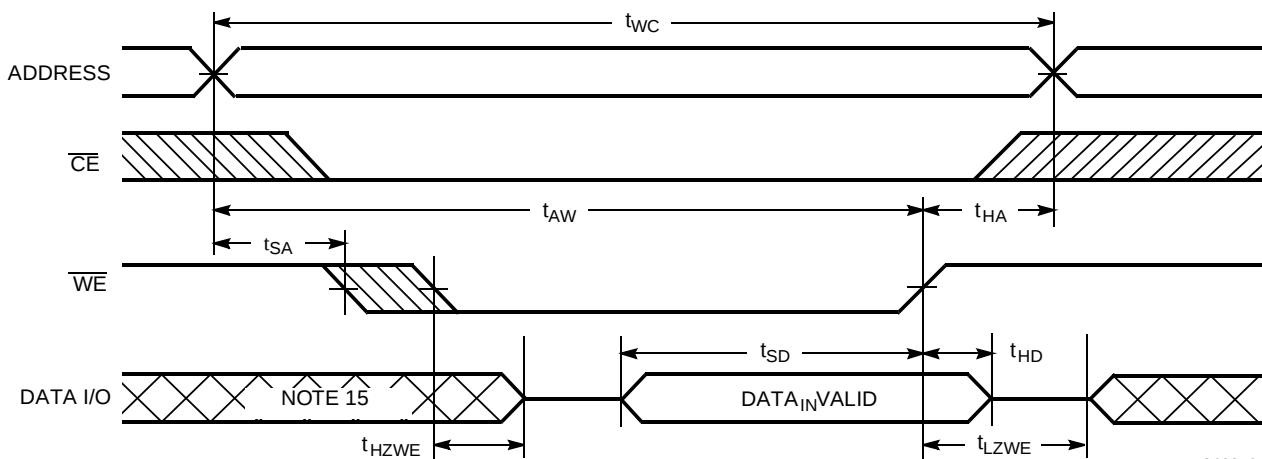
C62256V-10

Notes:

8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD} .
10. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
11. $\overline{WE}$ is HIGH for read cycle.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)
Write Cycle No. 2 ($\overline{CE}$ Controlled) [8, 13, 14]


C62256V-11

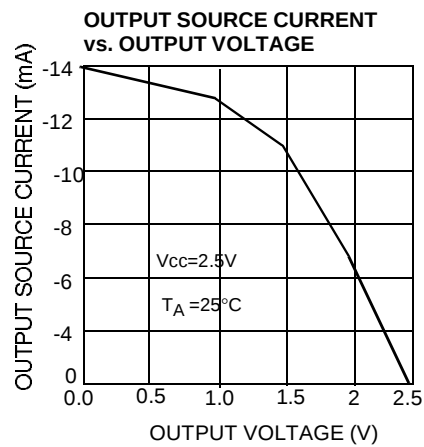
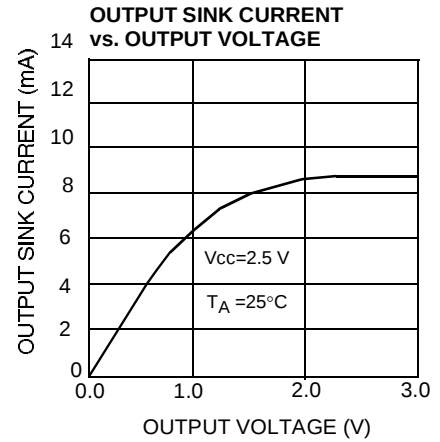
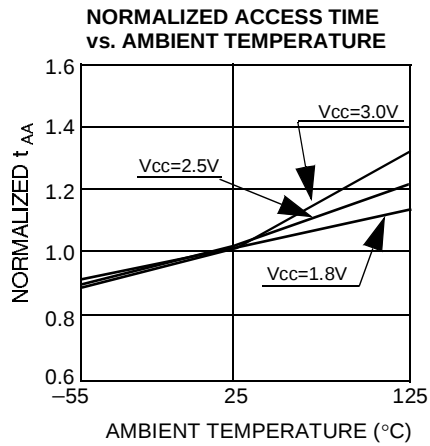
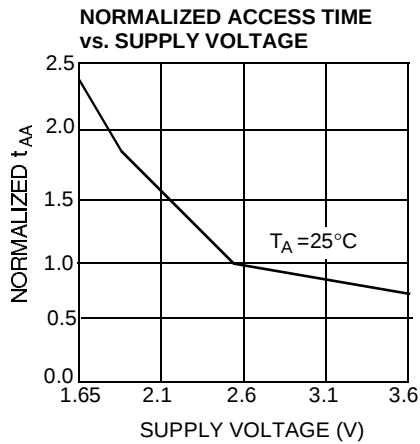
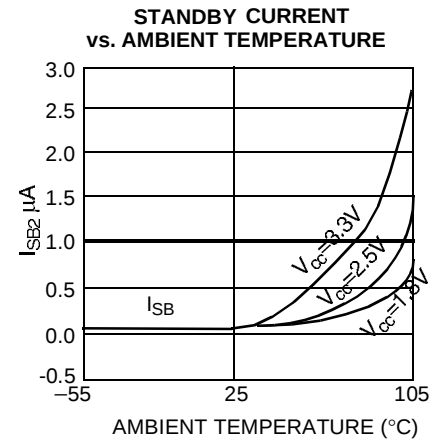
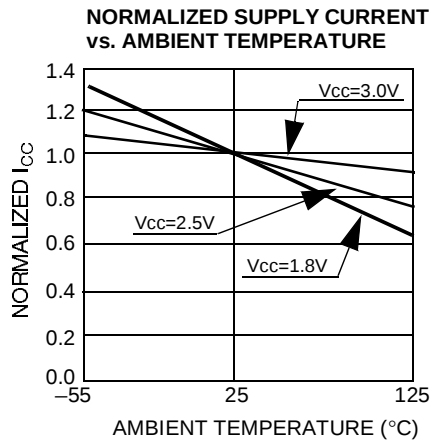
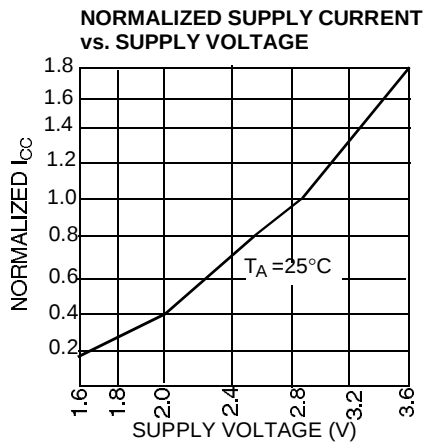
Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [9, 14]


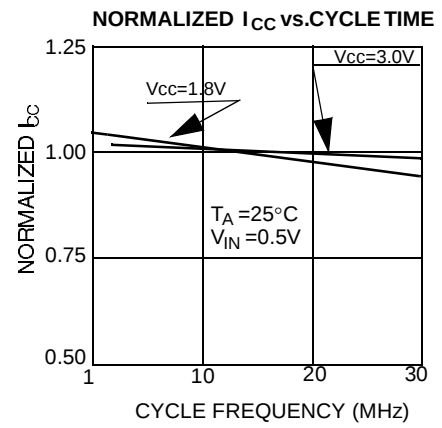
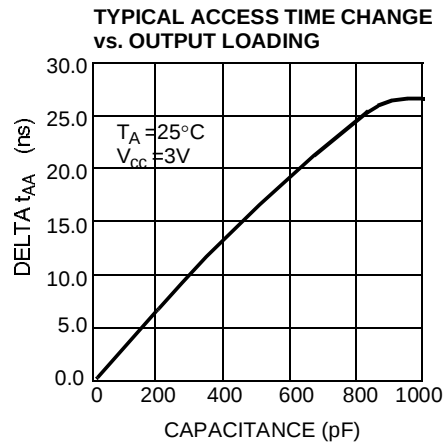
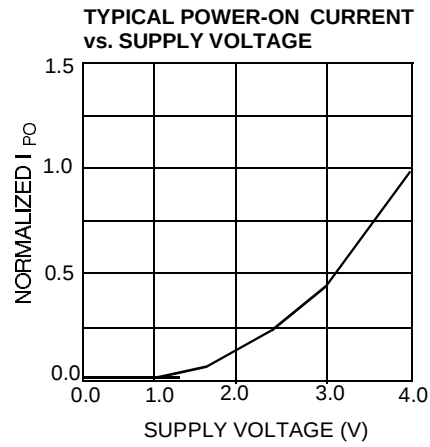
C62256V-12

Notes:

13. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in output state and input signals should not be applied.

Typical DC and AC Characteristics



Typical DC and AC Characteristics (continued)


Truth Table

CE	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62256V -70SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	Commercial
	CY62256V L-70SNC			
	CY62256V LL-70SNC			
	CY62256V -70ZRC	ZR28	28-Lead Reverse Thin Small Outline Package	
	CY62256V L-70ZRC			
	CY62256V LL-70ZRC			
	CY62256V -70ZC	Z28	28-Lead Thin Small Outline Package	
	CY62256V L-70ZC			
	CY62256V LL-70ZC			
	CY62256V -70ZI	Z28	28-Lead Thin Small Outline Package	Industrial
	CY62256V L-70ZI			
	CY62256V LL-70ZI			
	CY62256V -70SNI	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	
	CY62256VL -70SNI			
	CY62256VLL -70SNI			
	CY62256V -70ZRI	ZR28	28-Lead Reverse Thin Small Outline Package	
	CY62256V L-70ZRI			
	CY62256V LL-70ZRI			
100	CY62256V25-100SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	Commercial
	CY62256V25L-100SNC			
	CY62256V25LL-100SNC			
	CY62256V25-100ZRC	ZR28	28-Lead Reverse Thin Small Outline Package	
	CY62256V25L-100ZRC			
	CY62256V25LL-100ZRC			
	CY62256V25-100ZC	Z28	28-Lead Thin Small Outline Package	
100	CY62256V25L-100ZC	Z28	28-Lead Thin Small Outline Package	Commercial
	CY62256V25LL-100ZC			
200	CY62256V18-200SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	Commercial
	CY62256V18L-200SNC			
	CY62256V18LL-200SNC			
	CY62256V18-200ZRC	ZR28	28-Lead Reverse Thin Small Outline Package	
	CY62256V18L-200ZRC			
	CY62256V18LL-200ZRC			
	CY62256V18-200ZC	Z28	28-Lead Thin Small Outline Package	
	CY62256V18LL-200ZC			
200	CY62256V18L-200ZC	Z28	28-Lead Thin Small Outline Package	Commercial

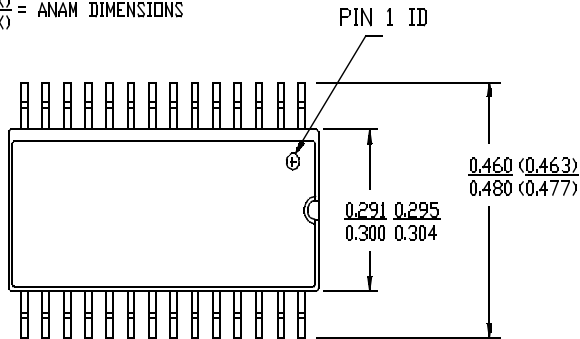
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Package Diagrams

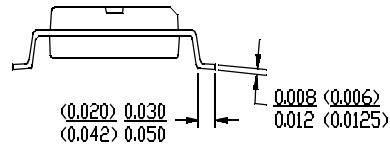
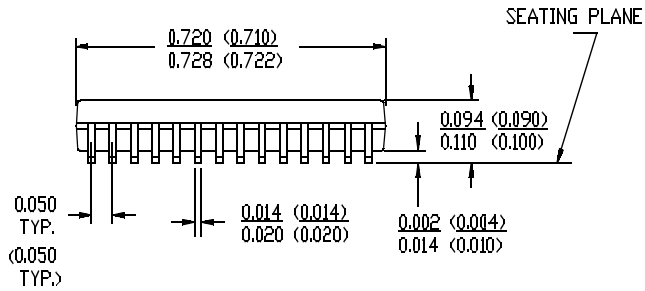
28-Lead 450-Mil (300-Mil Body Width) SOIC S22

.XXX = HYUNDAI DIMENSIONS
.XXX

<XXX> = ANAM DIMENSIONS
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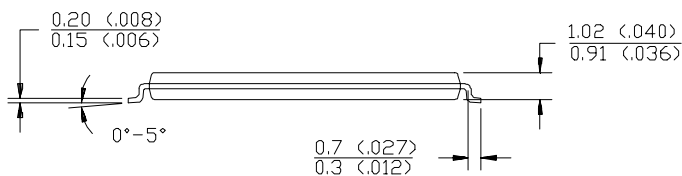
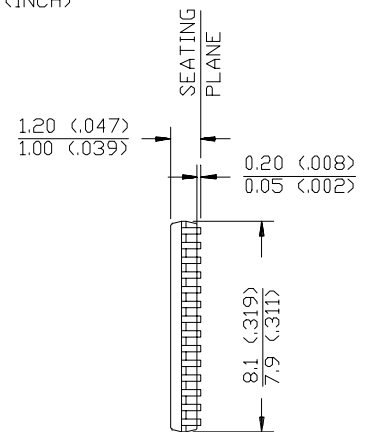
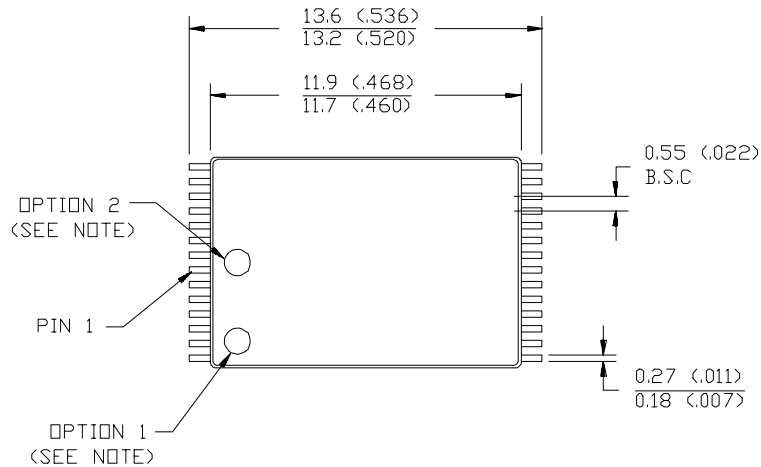
DIMENSIONS IN INCHES MIN.
MAX.
LEAD COPLANARITY 0.004 MAX.



28-Lead Reverse Thin Small Outline Package ZR28

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER
AS SHOWN IN OPTION 1 OR OPTION 2

DIMENSION IN MM (INCH)
MAX.
MIN.



Package Diagrams (continued)
28-Lead Thin Small Outline Package Z28

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER
AS SHOWN IN OPTION 1 OR OPTION 2

DIMENSION IN MM (INCH)
MAX.
MIN.

