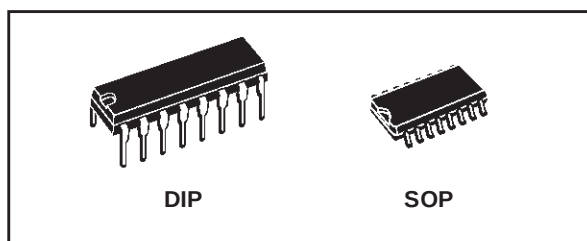




HCF4043B

QUAD NOR 3-STATE R-S LATCH

- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 3-LEVEL OUTPUTS WITH COMMON OUTPUT ENABLE
- SEPARATE SET AND RESET INPUT FOR EACH LATCH
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT
 $I_l = 100\text{nA (MAX) AT } V_{DD} = 18\text{V } T_A = 25^\circ\text{C}$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



ORDER CODES

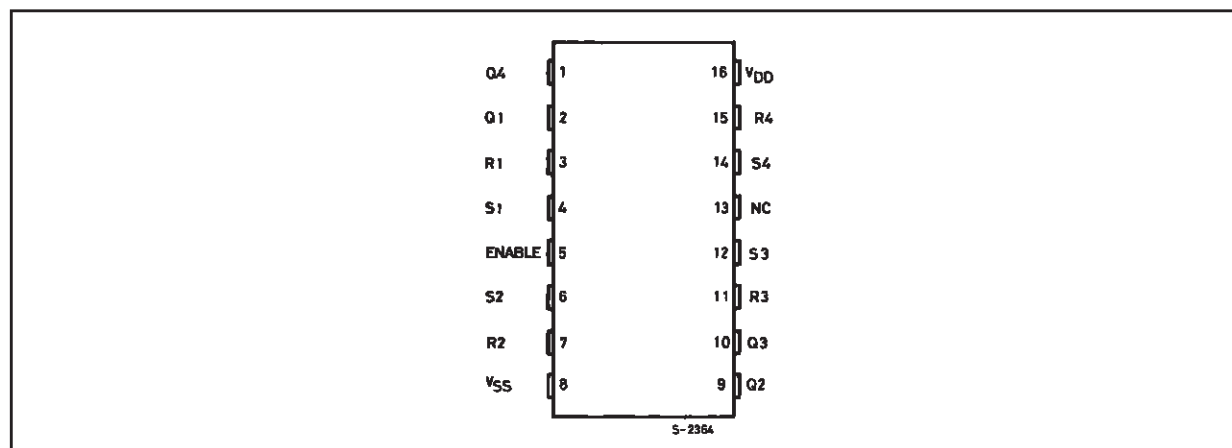
PACKAGE	TUBE	T & R
DIP	HCF4043BEY	
SOP	HCF4043BM1	HCF4043M013TR

DESCRIPTION

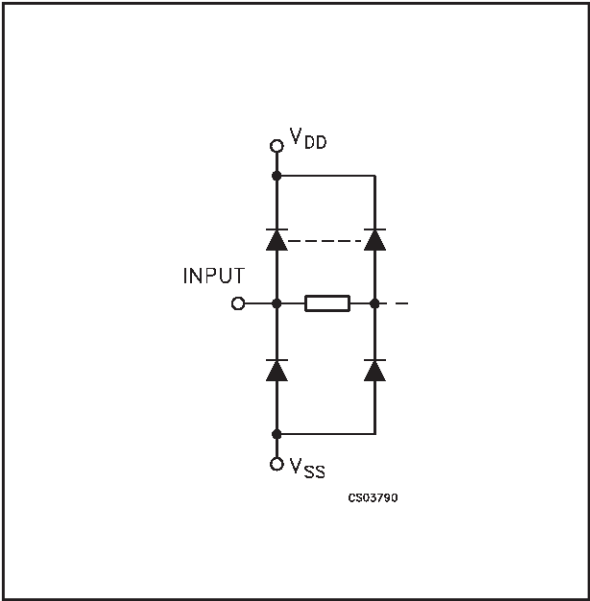
The HCF4043B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. The HCF4043B is a quad cross-coupled 3-state CMOS NOR latch. Each latch has a separate Q output and individual SET and RESET input. The Q outputs are

controlled by a common ENABLE input. A logic "1" or "high" on the ENABLE inputs connects the latch states to the Q outputs. A logic "0" or "low" on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common bussing of the outputs.

PIN CONNECTION



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

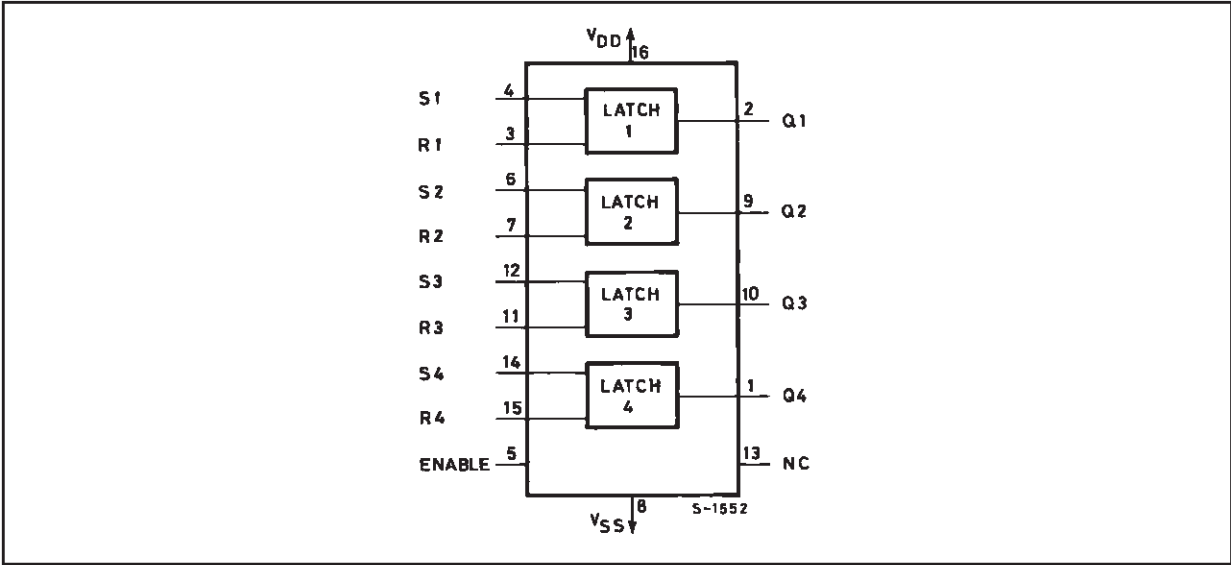
PIN No	SYMBOL	NAME AND FUNCTION
4, 6, 12, 14	S1 to S4	Set Inputs
3, 7, 11, 15	R1 to R4	Reset Inputs
5	ENABLE	Enable Input
2, 9, 10, 1	Q1 to Q4	Outputs
13	NC	Not Connected
8	VSS	Negative Supply Voltage
16	VDD	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUT Qn
ENABLE	Sn	Rn	
L	X	X	Z
H	L	H	L
H	H	X	H
H	L	L	LATCHED

X : Don't Care

FUNCTIONAL DIAGRAM



DC SPECIFICATIONS

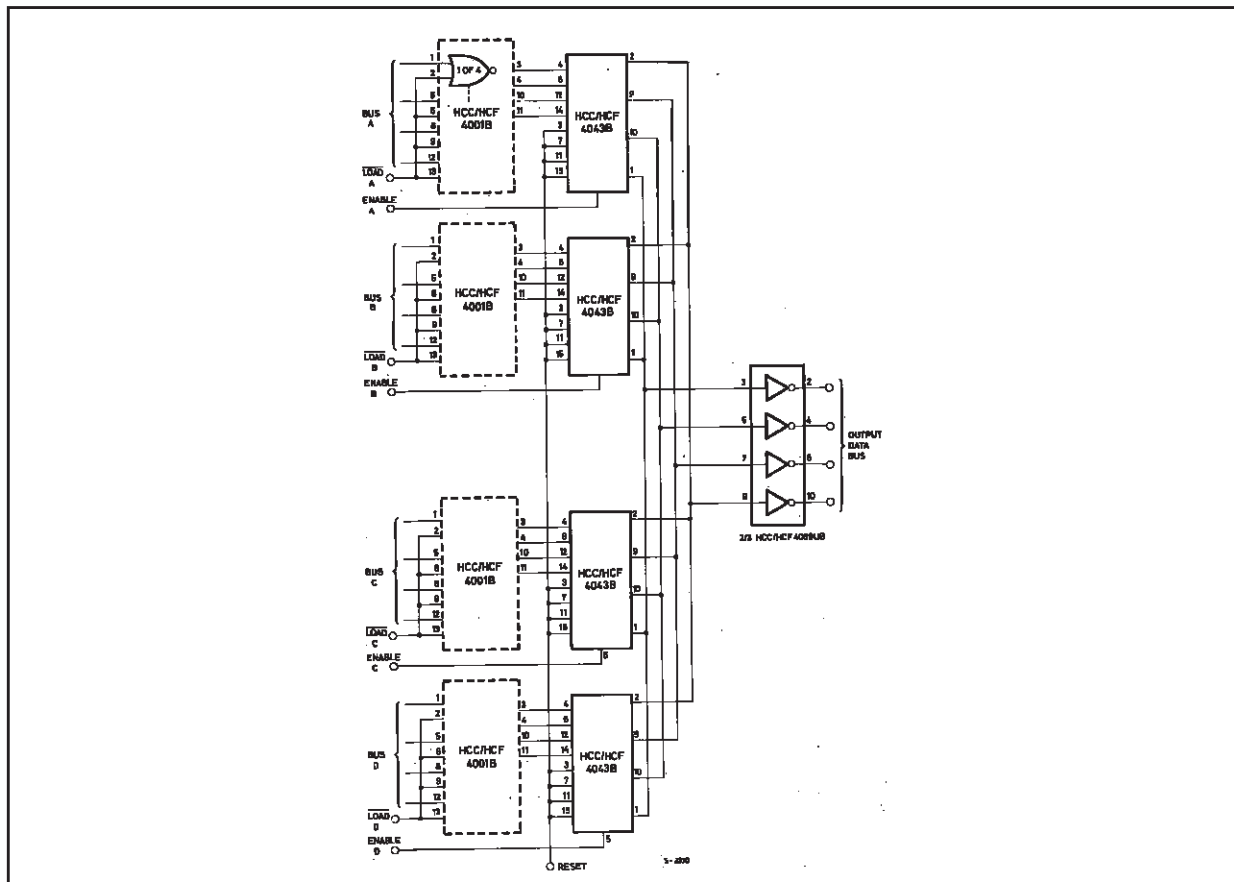
Symbol	Parameter	Test Condition				Value							Unit
		V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I _L	Quiescent Current	0/5			5		0.02	1		30		30	μA
		0/10			10		0.02	2		60		60	
		0/15			15		0.02	4		120		120	
		0/20			20		0.04	20		600		600	
V _{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V _{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V _{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V _{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I _{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I _{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I _I	Input Leakage Current	0/18	Any Input		18		±10 ⁻⁵	±0.1		±1		±1	μA
I _{OZ}	3-State Output	0/18	0/18		18		±10 ⁻⁴	±0.4		±12		±12	μA
C _I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

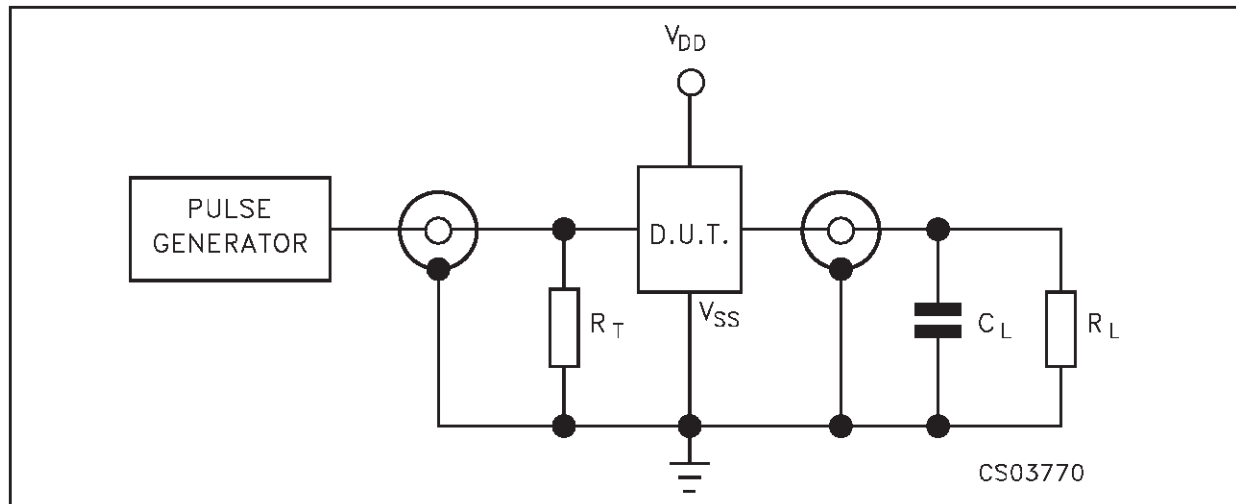
DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $C_L = 50\text{pF}$, $R_L = 200\text{K}\Omega$, $t_r = t_f = 20\text{ ns}$)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (SET or RESET to Q)	5			150	300	ns
		10			70	140	
		15			50	100	
t_{PZH} t_{PZL}	3-State Propagation Delay Time (Enable to Q)	5			115	230	ns
		10			55	110	
		15			40	80	
t_{PLZ} t_{PHZ}	3-State Propagation Delay Time (Disable to Q)	5			90	180	ns
		10			50	100	
		15			35	70	
t_{TLH} t_{THL}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
t_W	Pulse Width (Set or Reset)	5		160	80		ns
		10		80	40		
		15		40	20		

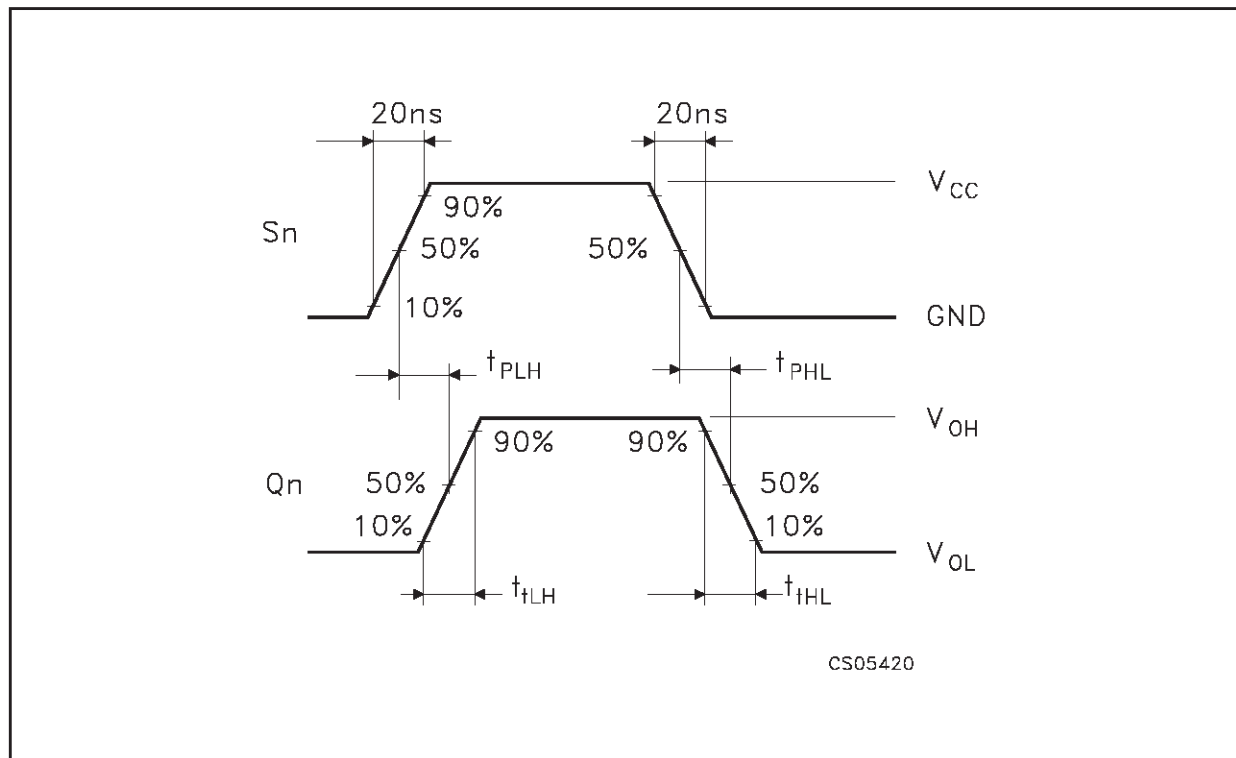
 (*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.

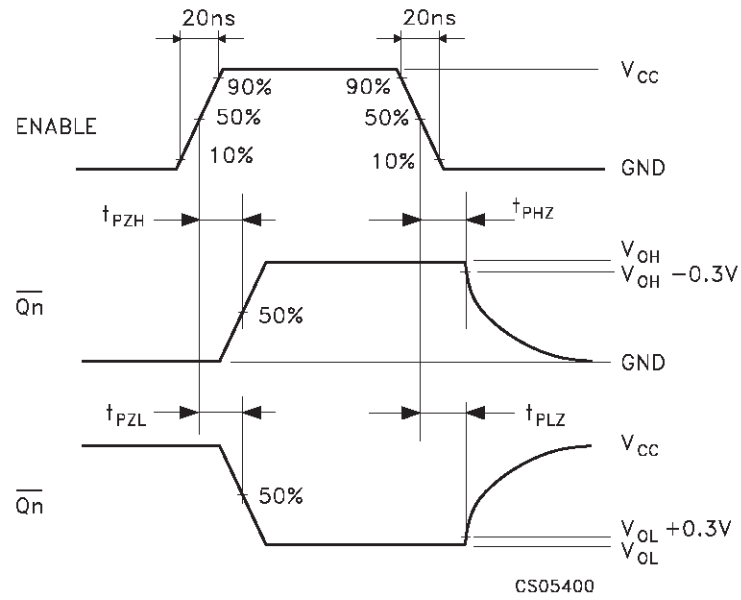
TYPICAL APPLICATIONS
MULTIPLE BUS STORAGE


TEST CIRCUIT



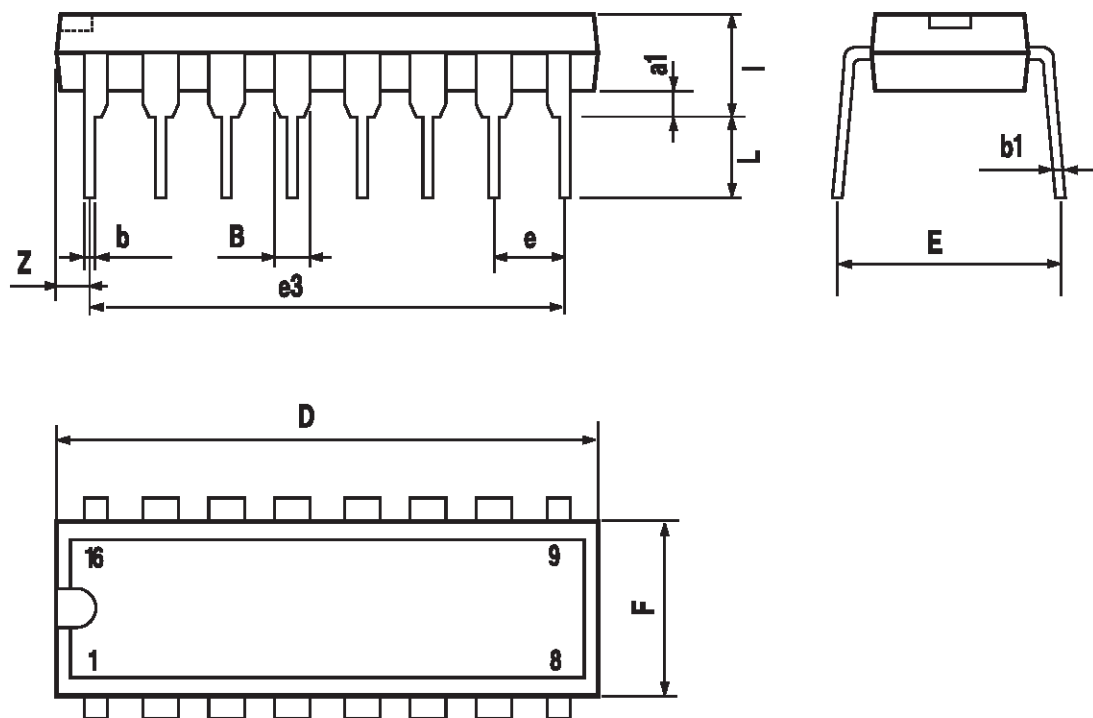
$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_L = 200\text{k}\Omega$
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM : PROPAGATION DELAY TIMES ($f=1\text{MHz}$; 50% duty cycle)

WAVEFORM 2 : OUTPUT ENABLE AND DISABLE TIMES (f=1MHz; 50% duty cycle)

Plastic DIP-16 (0.25) MECHANICAL DATA

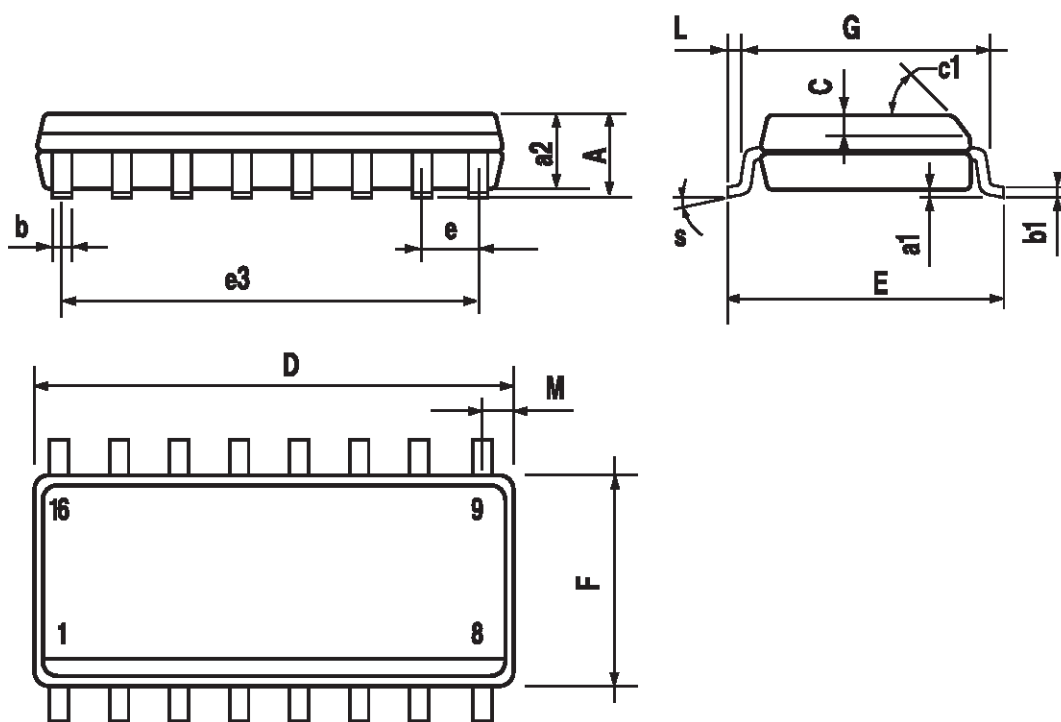
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

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