

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- *DOC™* (Dynamic Output Control) Circuit Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation
- Dynamic Drive Capability Is Equivalent to Standard Outputs With I_{OH} and I_{OL} of ± 24 mA at 2.5-V V_{CC}
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Package Options Include Plastic Thin Shrink Small-Outline (DGG) and Thin Very Small-Outline (DGV) Packages

description

A Dynamic Output Control (DOC) circuit is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical V_{OL} vs I_{OL} and V_{OH} vs I_{OH} curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

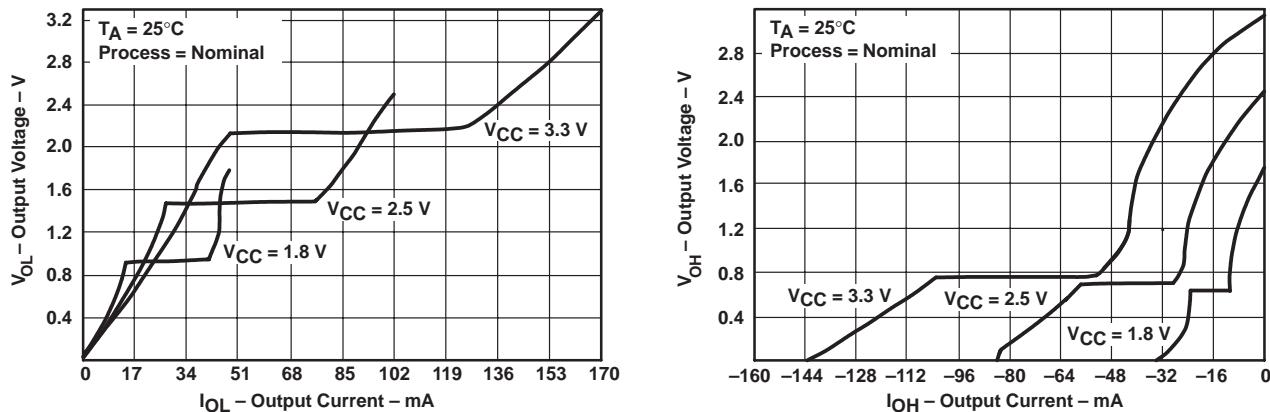


Figure 1. Output Voltage vs Output Current

This 16-bit bus transceiver and register is operational at 1.2-V to 3.6-V V_{CC} , but is designed specifically for 1.65-V to 3.6-V V_{CC} operation.

The SN74AVC16646 can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 2 illustrates the four fundamental bus-management functions that can be performed with the SN74AVC16646.

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data.



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16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

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description (continued)

The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The SN74AVC16646 is characterized for operation from -40°C to 85°C .

terminal assignments

DGG OR DGV PACKAGE (TOP VIEW)		
1DIR	1	56
1CLKAB	2	55
1SAB	3	54
GND	4	53
1A1	5	52
1A2	6	51
V_{CC}	7	50
1A3	8	49
1A4	9	48
1A5	10	47
GND	11	46
1A6	12	45
1A7	13	44
1A8	14	43
2A1	15	42
2A2	16	41
2A3	17	40
GND	18	39
2A4	19	38
2A5	20	37
2A6	21	36
V_{CC}	22	35
2A7	23	34
2A8	24	33
GND	25	32
2SAB	26	31
2CLKAB	27	30
2DIR	28	29
		\overline{OE}
		1CLKBA
		1SBA
		GND
		V_{CC}
		1B1
		1B2
		1B3
		1B4
		1B5
		GND
		1B6
		1B7
		1B8
		2B1
		2B2
		2B3
		GND
		2B4
		2B5
		2B6
		V_{CC}
		2B7
		2B8
		GND
		2SBA
		2CLKBA
		\overline{OE}

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FUNCTION TABLE
 (each 8-bit transceiver/register)

INPUTS						DATA I/Os		OPERATION OR FUNCTION
\overline{OE}	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

† The data-output functions may be enabled or disabled by various signals at \overline{OE} and DIR. Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

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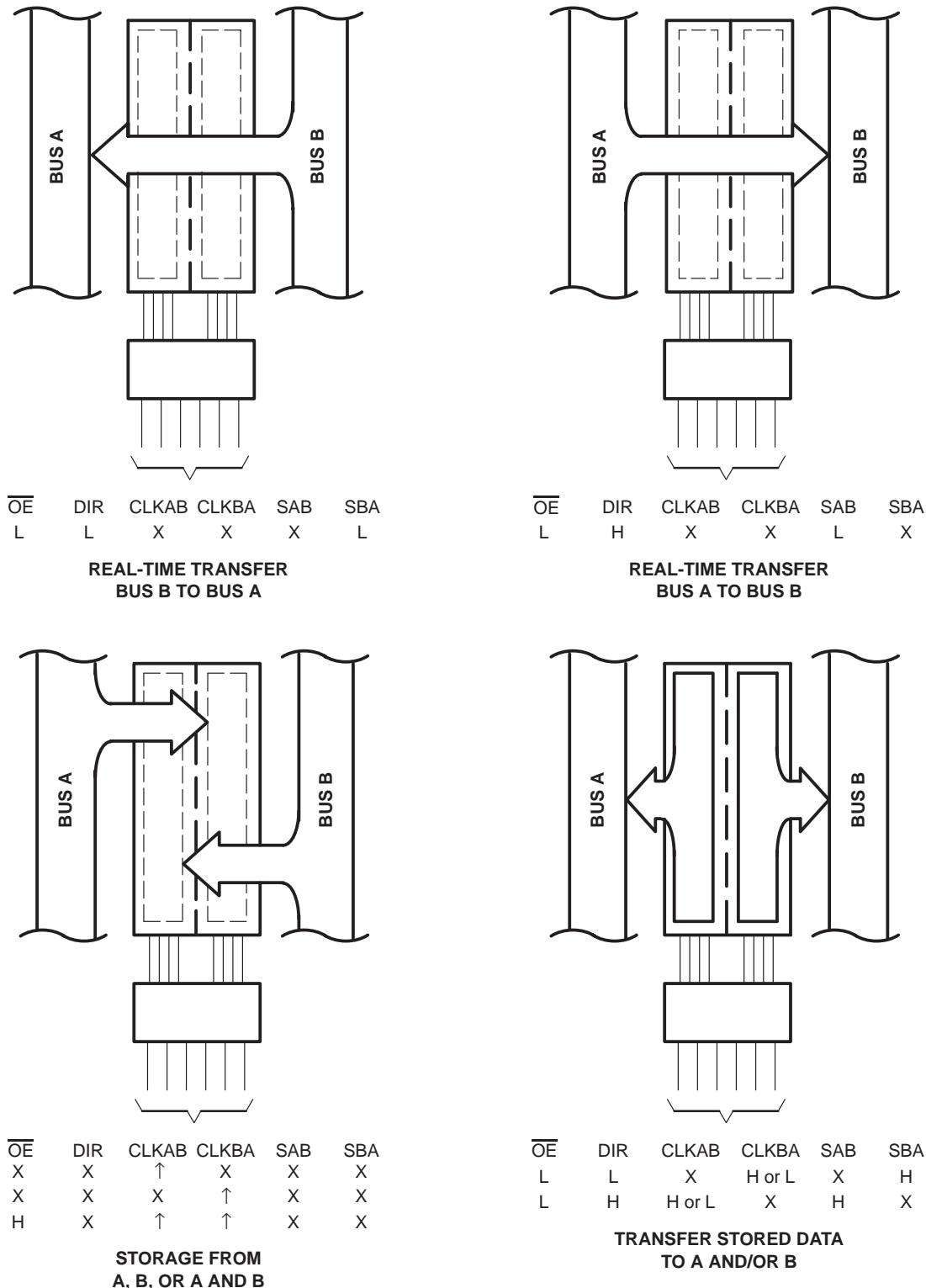
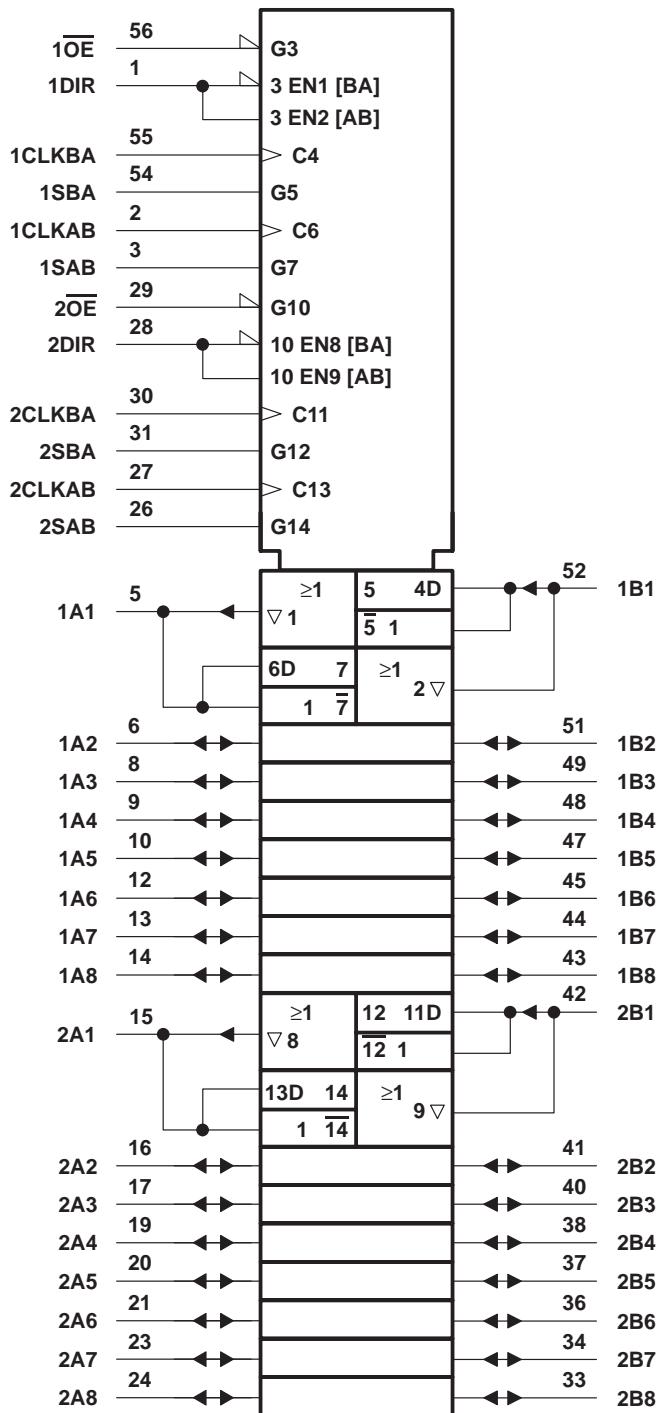


Figure 2. Bus-Management Functions

logic symbol†

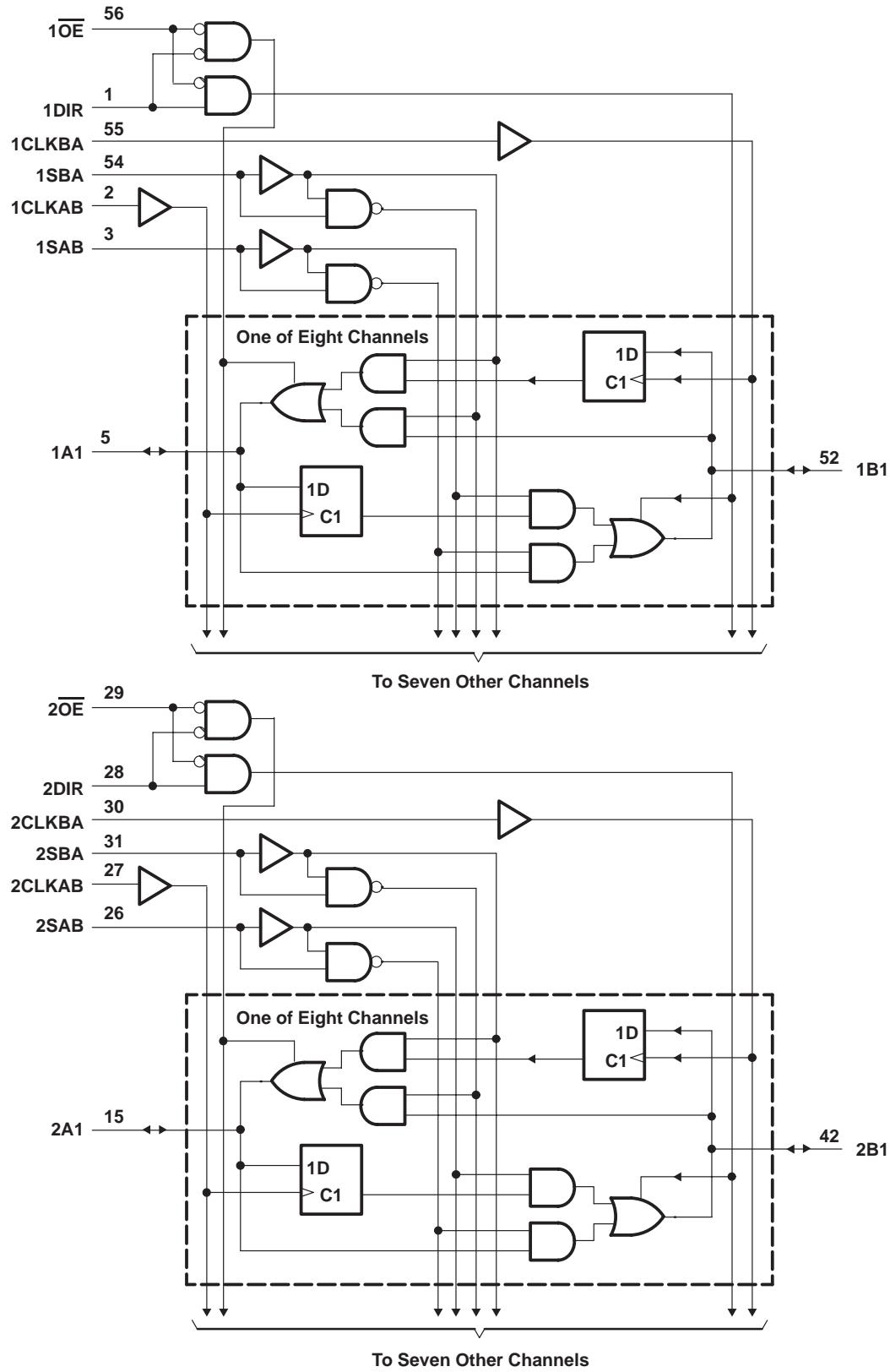


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Voltage range applied to any input/output when the output is in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 4.6 V
Voltage range applied to any input/output when the output is in the high or low state, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Continuous output current, I_O	± 50 mA
Continuous current through each V_{CC} or GND	± 100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	64°C/W
DGV package	48°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
 3. The package thermal impedance is calculated in accordance with JEDEC 51.

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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.2	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 1.2 V	V _{CC}		V
		V _{CC} = 1.4 V to 1.6 V	0.65 × V _{CC}		
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 3 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 1.2 V	GND		V
		V _{CC} = 1.4 V to 1.6 V	0.35 × V _{CC}		
		V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 3 V to 3.6 V	0.8		
V _I	Input voltage		0	3.6	V
V _O	Output voltage	Active state	0	V _{CC}	V
		3-state	0	3.6	
I _{OHS}	Static high-level output current [†]	V _{CC} = 1.4 V to 1.6 V	-2		mA
		V _{CC} = 1.65 V to 1.95 V	-4		
		V _{CC} = 2.3 V to 2.7 V	-8		
		V _{CC} = 3 V to 3.6 V	-12		
I _{OLS}	Static low-level output current [†]	V _{CC} = 1.4 V to 1.6 V	2		mA
		V _{CC} = 1.65 V to 1.95 V	4		
		V _{CC} = 2.3 V to 2.7 V	8		
		V _{CC} = 3 V to 3.6 V	12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.4 V to 3.6 V	5	ns/V	
T _A	Operating free-air temperature		-40	85	°C

[†] Dynamic drive capability is equivalent to standard outputs with I_{OH} and I_{OL} of ±24 mA at 2.5-V V_{CC}. See Figure 1 for V_{OL} vs I_{OL} and V_{OH} vs I_{OH} characteristics. Refer to the TI application reports, **AVC Logic Family Technology and Applications**, literature number **SCEA006**, and **Dynamic Output Control (DOC™) Circuitry Technology and Applications**, literature number **SCEA009**.

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT	
V _{OH}	I _{OH} S = -100 µA		1.2 V to 3.6 V	V _{CC} –0.2			V	
	I _{OH} S = -2 mA, V _{IH} = 0.91 V		1.4 V	1.05				
	I _{OH} S = -4 mA, V _{IH} = 1.07 V		1.65 V	1.2				
	I _{OH} S = -8 mA, V _{IH} = 1.7 V		2.3 V	1.75				
	I _{OH} S = -12 mA, V _{IH} = 2 V		3 V	2.3				
V _{OL}	I _{OLS} = 100 µA		1.2 V to 3.6 V		0.2		V	
	I _{OLS} = 2 mA, V _{IL} = 0.49 V		1.4 V		0.4			
	I _{OLS} = 4 mA, V _{IL} = 0.57 V		1.65 V		0.45			
	I _{OLS} = 8 mA, V _{IL} = 0.7 V		2.3 V		0.55			
	I _{OLS} = 12 mA, V _{IL} = 0.8 V		3 V		0.7			
I _I	Control inputs	V _I = V _{CC} or GND	3.6 V		±2.5	µA		
I _{off}		V _I or V _O = 3.6 V	0		±10	µA		
I _{OZ} ‡		V _O = V _{CC} or GND, V _I = V _{CC}	3.6 V		±12.5	µA		
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V		40	µA		
C _i	CLK inputs	V _I = V _{CC} or GND	2.5 V		3		pF	
			3.3 V		3			
	Control inputs		2.5 V		3.5			
			3.3 V		3.5			
C _{io}	A or B ports	V _O = V _{CC} or GND	2.5 V		8		pF	
			3.3 V		8			

† Typical values are measured at T_A = 25°C.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 3 through 6)

			V _{CC} = 1.2 V	V _{CC} = 1.5 V ± 0.1 V	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency					150	250	350	MHz
t _w	Pulse duration	CLKAB or CLKBA high or low			3.3	2	1.4		ns
t _{su}	Setup time	A before CLKAB↑ or B before CLKBA↑	2.1	1.6	1.2	0.9	0.8		ns
t _h	Hold time	A after CLKAB↑ or B after CLKBA↑	1.3	1	0.8	0.6	0.6		ns

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 3 through 6)

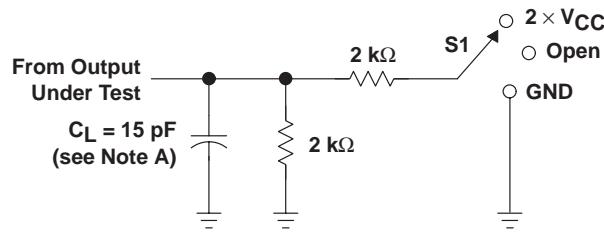
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.2 V	V _{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
				TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}							150		250		350		MHz
t _{pd}	A or B	B or A	4.2	1.6	4.8	1.5	4.3	1.2	3.1	0.9	2.6	ns	
	CLKAB or CLKBA	A or B	5.9	2.2	7.4	1.9	6.1	1.3	4	1	3.3		
	SAB or SBA		8.2	2.6	10	2.4	6.3	1.8	5.1	1.5	4		
t _{en}	OE	A or B	6.5	2.2	8	1.9	7	1.4	4.6	1.1	4	ns	
t _{dis}	OE	A or B	6.7	2.6	8	2.6	7.2	1.4	4.3	1.4	4.2	ns	
t _{en}	DIR	A or B	6.9	2.2	8.7	1.9	7.4	1.4	5	1.1	4.3	ns	
t _{dis}	DIR	A or B	7.5	2.6	8.7	2.6	7.6	1.4	4.5	1.4	4.3	ns	

operating characteristics, T_A = 25°C

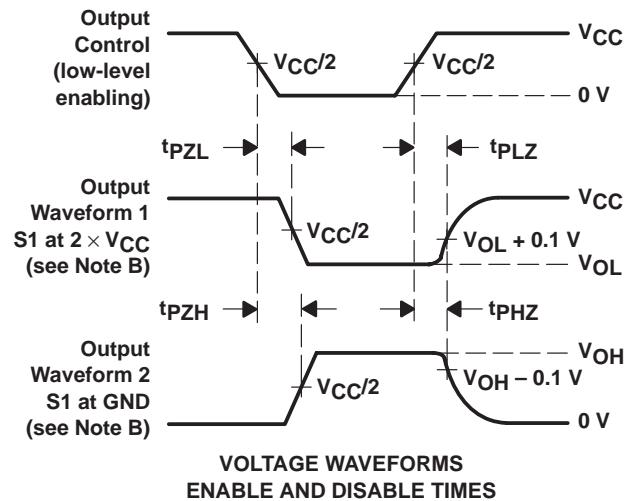
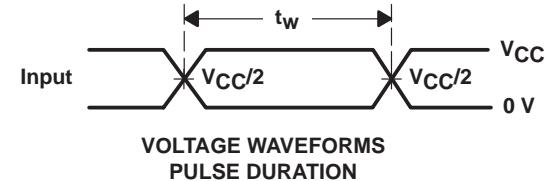
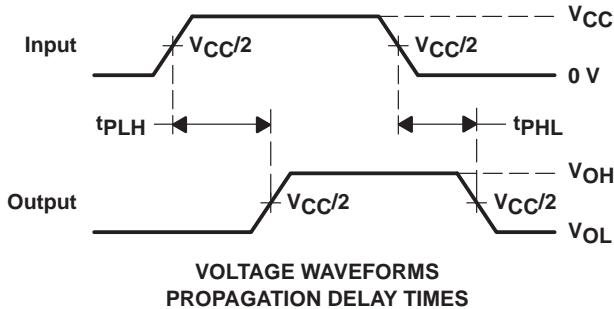
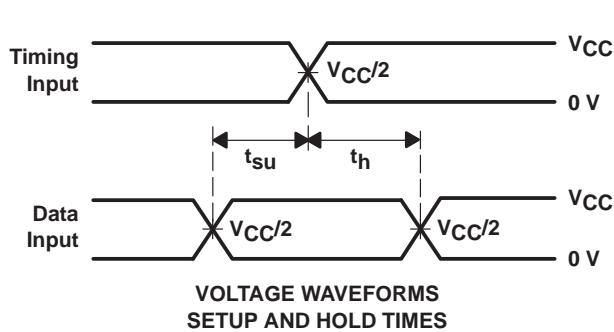
PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
		TYP	TYP	TYP	
C _{pd} Power dissipation capacitance	Outputs enabled	62	73	120	pF
	Outputs disabled	25	29	34	

PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.2 \text{ V AND } 1.5 \text{ V} \pm 0.1 \text{ V}$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

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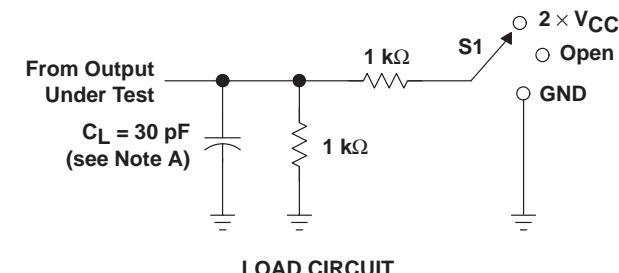
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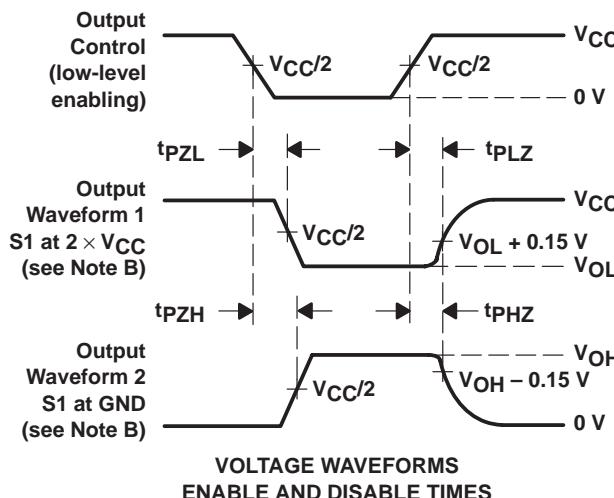
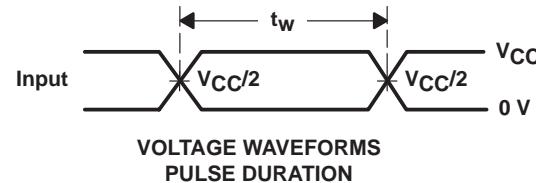
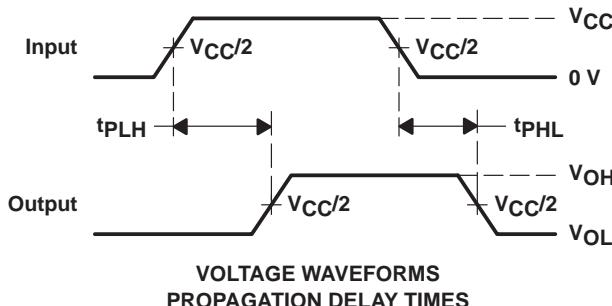
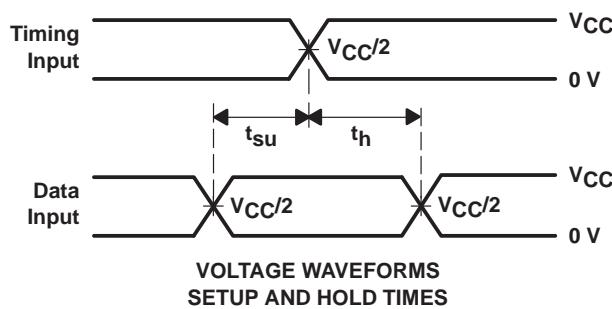
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PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



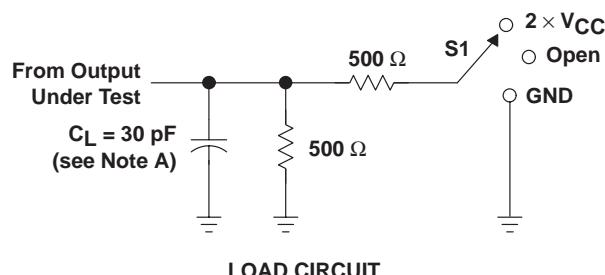
NOTES:

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- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .

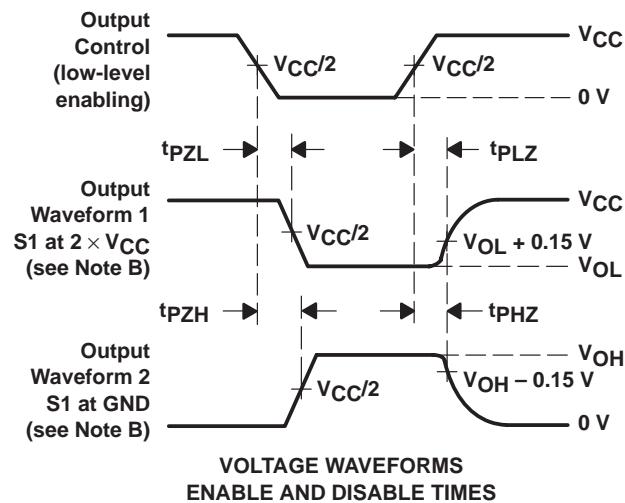
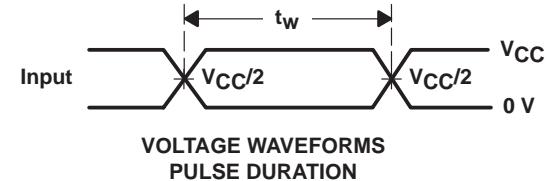
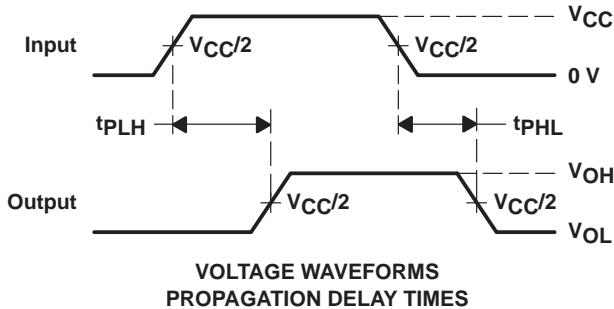
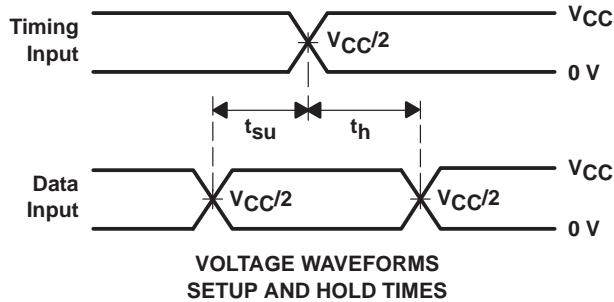
Figure 4. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 \times V_{CC}
t_{PHZ}/t_{PZH}	GND



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .

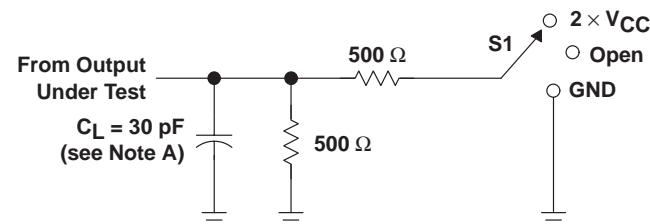
Figure 5. Load Circuit and Voltage Waveforms

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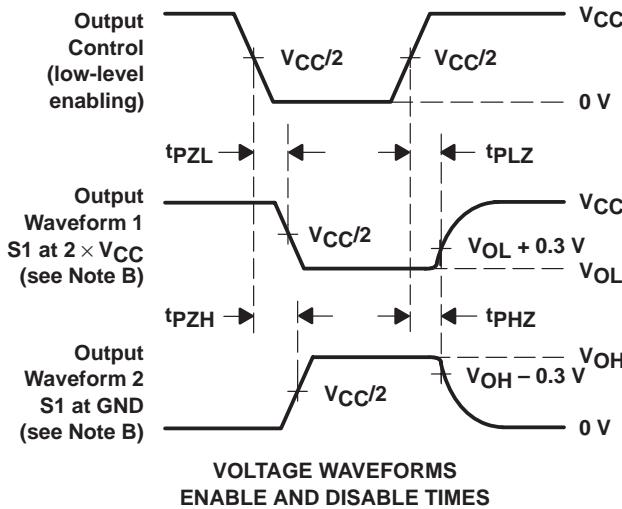
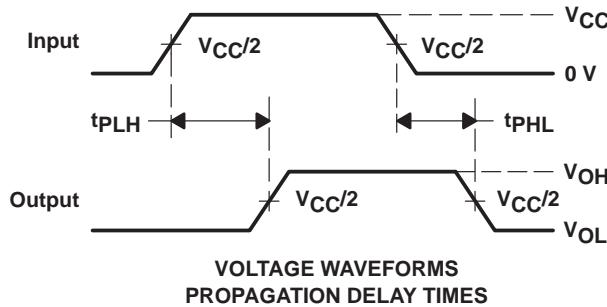
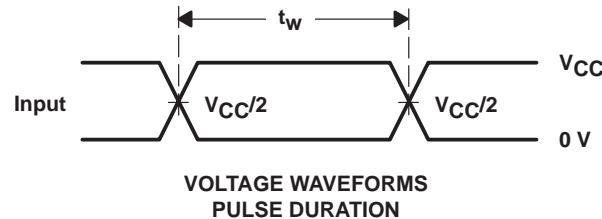
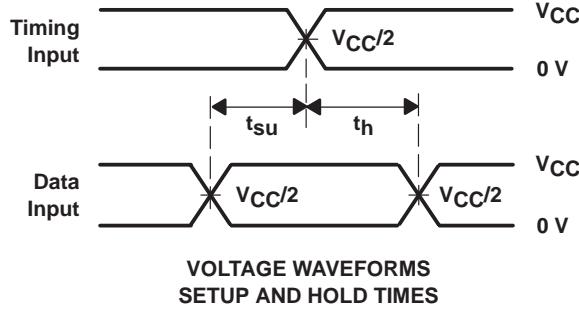
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PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 \times V_{CC}
t_{PHZ}/t_{PZH}	GND



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 6. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AVC16646DGGR	ACTIVE	TSSOP	DGG	56	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74AVC16646DGVR	ACTIVE	TVSOP	DGV	56	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

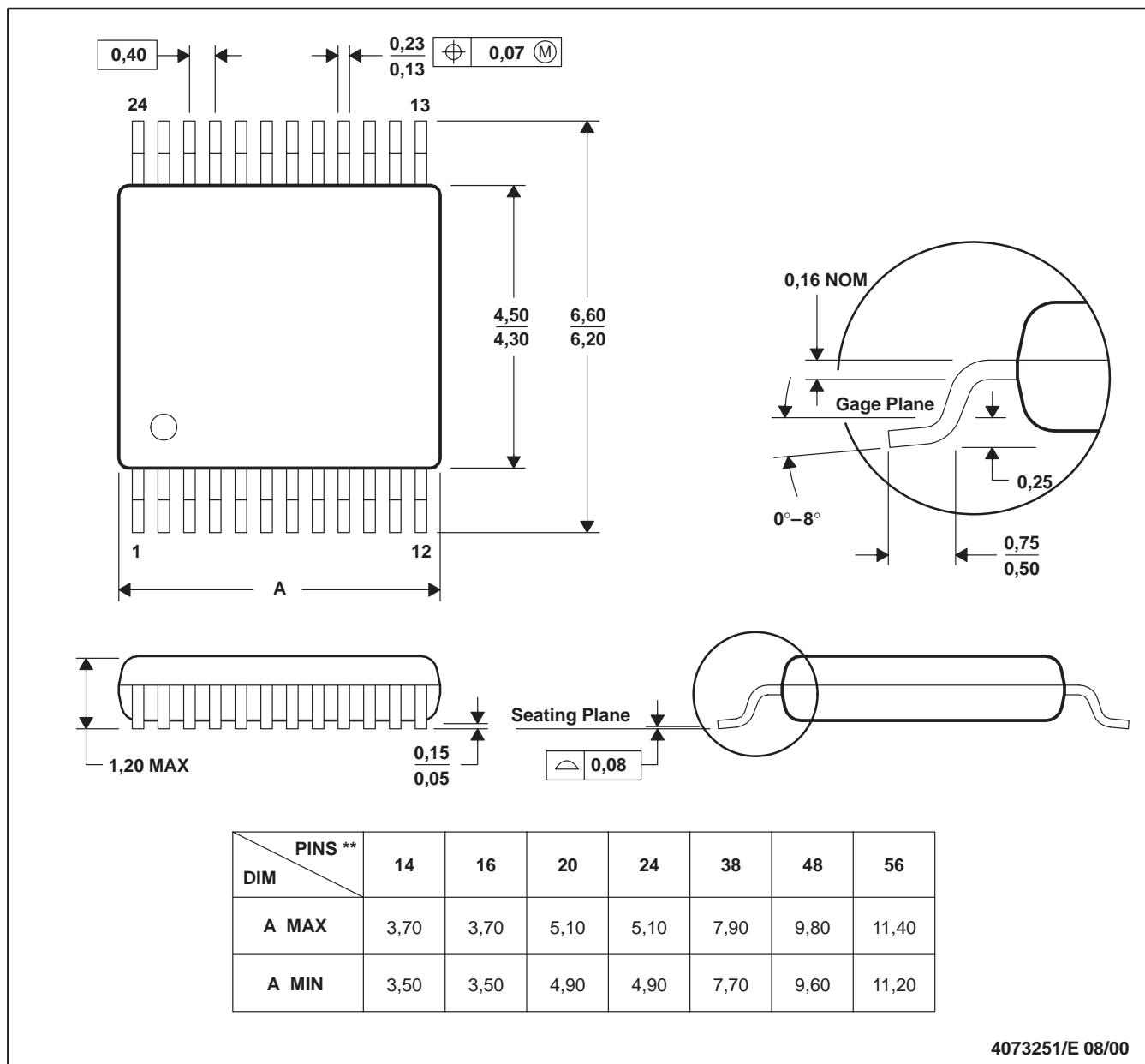
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DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

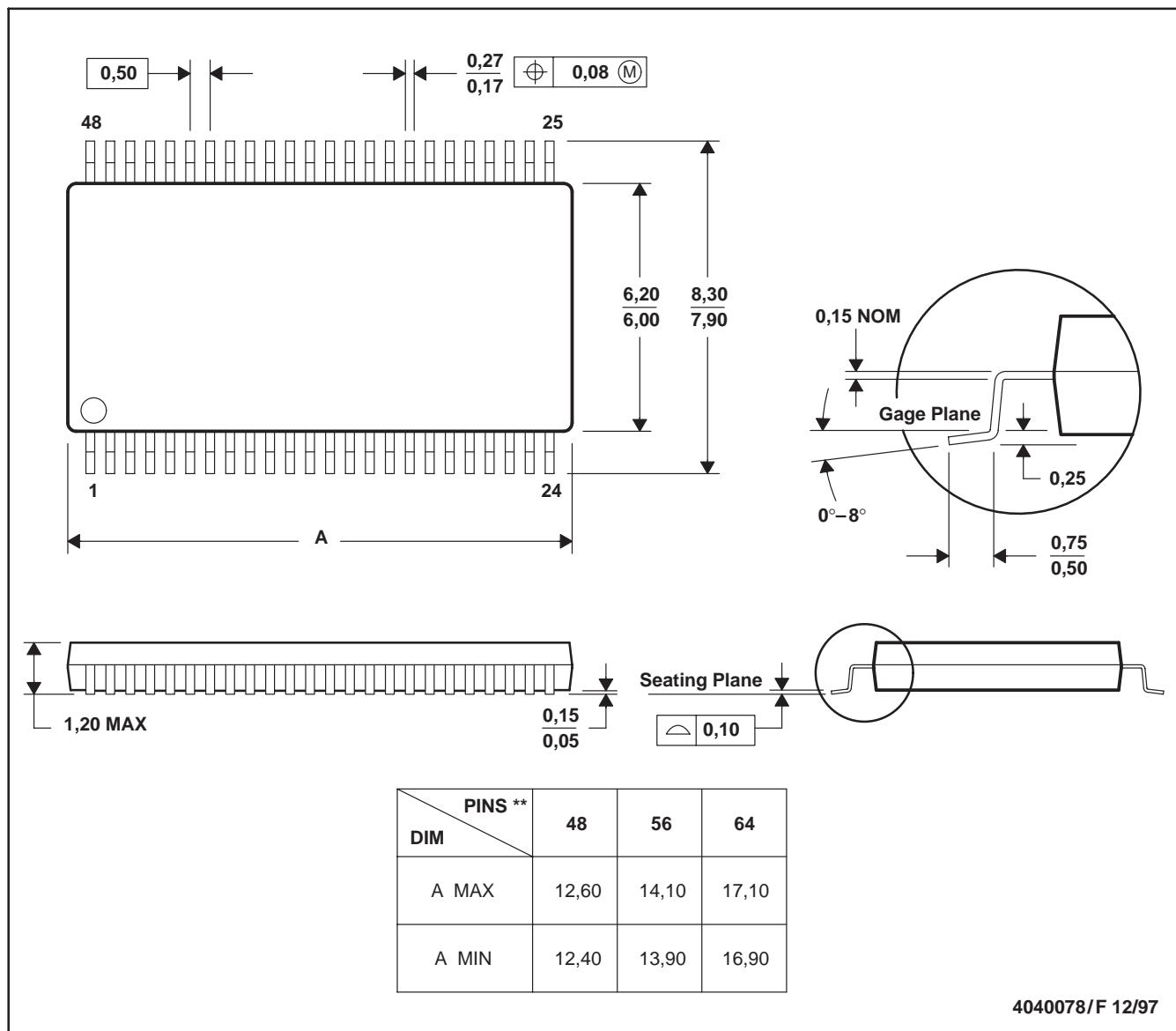


NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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