16-Bit, 500ksps, Low Power SAR ADC with Serial Interface

FEATURES

- **500ksps Throughput Rate**
- **±2LSB INL (Max)**
- **Guaranteed 16-Bit No Missing Codes**
- **Low Power: 6.5mW at 500ksps, 13µW at 1ksps**
- **92dB SNR (typ) at f_{IN} = 20kHz**
- **Extended Acquisition Time of 1.25µs Allows Use of Lower Power Drivers**
- Guaranteed Operation to 125°C
- 2.5V Supply
- Fully Differential Input Range ±2.5V
- External 2.5V Reference Input
- No Pipeline Delay, No Cycle Latency
- 1.8V to 5V I/O Voltages
- SPI-Compatible Serial I/O with Daisy-Chain Mode
- Internal Conversion Clock
- 16-pin MSOP and 4mm × 3mm DFN Packages

APPLICATIONS

- Medical Imaging
- High Speed Data Acquisition
- Portable or Compact Instrumentation
- Industrial Process Control
- Low Power Battery-Operated Instrumentation
- ATE

DESCRIPTION

The LTC®2382-16 is a low noise, low power, high speed 16-bit successive approximation register (SAR) ADC. Operating from a 2.5V supply, the LTC2382-16 has a ±2.5V fully differential input range. The LTC2382-16 consumes only 6.5mW and achieves ±2LSB INL max, no missing codes at 16-bits and 92dB SNR.

The LTC2382-16 has a high speed SPI-compatible serial interface that supports 1.8V, 2.5V, 3.3V and 5V logic while also featuring a daisychain mode. The fast 500ksps throughput with no cycle latency makes the LTC2382-16 ideally suited for a wide variety of high speed applications. An internal oscillator sets the conversion time, easing external timing considerations. The LTC2382-16 automatically powers down between conversions, leading to reduced power dissipation that scales with the sampling rate.

The LTC2382-16 features a proprietary sampling architecture that enables the ADC to begin acquiring the next sample during the current conversion. The resulting extended acquisition time of 1.25µs allows the use of extremely low power ADC drivers.

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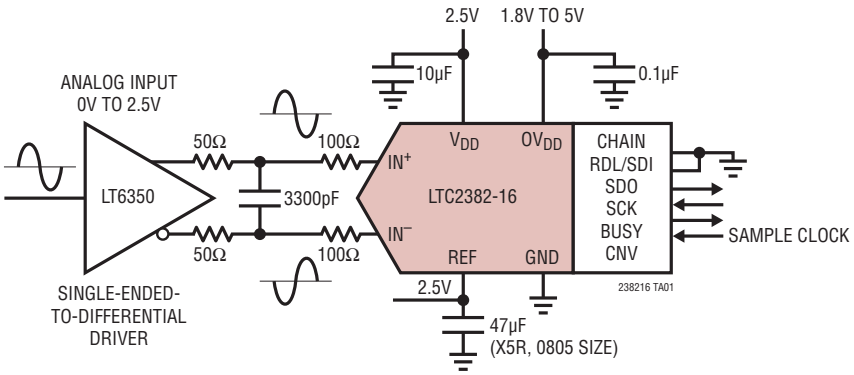
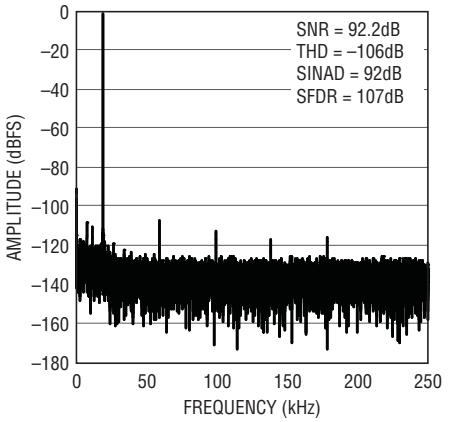
TYPICAL APPLICATION



32k Point FFT f_S = 500ksps, f_{IN} = 20kHz



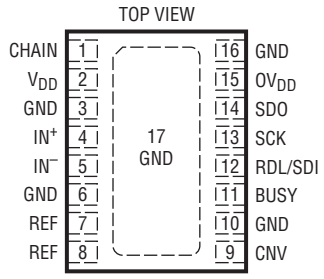
238216 TA02a

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

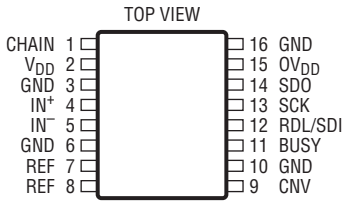
Supply Voltage (V_{DD}) 2.8V
Supply Voltage (OV_{DD}) 6V
Reference Input (REF) 2.8V
Analog Input Voltage (Note 3)
  IN^+, IN^- ..... (GND –0.3V) to (REF + 0.3V)
Digital Input Voltage
(Note 3) ..... (GND –0.3V) to (OV_{DD} + 0.3V)
Digital Output Voltage
(Note 3) ..... (GND –0.3V) to (OV_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range
  LTC2382C ..... 0°C to 70°C
  LTC2382I ..... –40°C to 85°C
  LTC2382H ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DE PACKAGE
16-LEAD (4mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB



MS PACKAGE
16-LEAD (4mm × 5mm) PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2382CMS-16#PBF	LTC2382CMS-16#TRPBF	238216	16-Lead Plastic MSOP	0°C to 70°C
LTC2382IMS-16#PBF	LTC2382IMS-16#TRPBF	238216	16-Lead Plastic MSOP	–40°C to 85°C
LTC2382HMS-16#PBF	LTC2382HMS-16#TRPBF	238216	16-Lead Plastic MSOP	–40°C to 125°C
LTC2382CDE-16#PBF	LTC2382CDE-16#TRPBF	23826	16-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC2382IDE-16#PBF	LTC2382IDE-16#TRPBF	23826	16-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN}+$	Absolute Input Range (IN^+)	(Note 5)	●	–0.05		V_{REF}	V
$V_{IN}–$	Absolute Input Range ($IN^–$)	(Note 5)	●	–0.05		V_{REF}	V
$V_{IN}+ – V_{IN}–$	Input Differential Voltage range	$V_{IN} = V_{IN}+ – V_{IN}–$	●	$–V_{REF}$		$+V_{REF}$	V
V_{CM}	Common-Mode Input Range		●	$V_{REF}/2–$ 0.05	$V_{REF}/2$	$V_{REF}/2+$ 0.05	V
I_{IN}	Analog Input Leakage Current		●			±1	µA
C_{IN}	Analog Input Capacitance	Sample Mode Hold Mode			45 5		pF pF
CMRR	Input Common Mode Rejection Ratio				70		dB

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution		●	16			Bits
	No Missing Codes		●	16			Bits
	Transition Noise				0.6		LSB_{RMS}
INL	Integral Linearity Error	(Note 6)	●	–2	±0.9	2	LSB
DNL	Differential Linearity Error		●	–1	±0.4	1	LSB
BZE	Bipolar Zero-Scale Error	(Note 7)	●	–6	±0.25	6	LSB
	Bipolar Zero-Scale Error Drift				3		mLSB/°C
FSE	Bipolar Full-Scale Error	(Note 7)	●	–14	±3	14	LSB
	Bipolar Full-Scale Error Drift				±0.1		ppm/°C

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and A_{IN} = –1dBFS. (Notes 4, 8)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	f_{IN} = 20kHz	●	88.5	92		dB
SNR	Signal-to-Noise Ratio	f_{IN} = 20kHz	●	89	92		dB
THD	Total Harmonic Distortion	f_{IN} = 20kHz, First 5 Harmonics	●		–106	–99	dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 20kHz			107		dB
	–3dB Input Bandwidth				30		MHz
	Aperture Delay				2		ns
	Aperture Jitter				30		ps
	Transient Response	Full-Scale Step			250		ns

REFERENCE INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	(Note 5)	●	2.4		2.6	V
I_{REF}	Load Current	(Note 9)	●			495	µA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		●	0.8 • OV_{DD}			V
V_{IL}	Low Level Input Voltage		●			0.2 • OV_{DD}	V
I_{IN}	Digital Input Current	V_{IN} = 0V to OV_{DD}	●	–10		10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	I_O = –500 µA	●	OV_{DD} – 0.2			V
V_{OL}	Low Level Output Voltage	I_O = 500 µA	●			0.2	V
I_{OZ}	Hi-Z Output Leakage Current	V_{OUT} = 0V to OV_{DD}	●	–10		10	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = OV_{DD}			10		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		●	2.375	2.5	2.625	V
OV_{DD}	Supply Voltage			1.71		5.25	V
I_{DD}	Supply Current Power Down Mode Power Down Mode	500ksps Sample Rate Conversion Done Conversion Done (H-Grade)	● ● ●		2.6 0.5 0.5	3.3 40 110	mA µA µA
P_D	Power Dissipation Power Down Mode Power Down Mode	500ksps Sample Rate Conversion Done Conversion Done (H-Grade)			6.5 1.25 1.25	8.25 100 275	mW µW µW

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SMPL}	Maximum Sampling Frequency		●			500	ksps
t_{CONV}	Conversion Time		●	1		1.5	µs
t_{ACQ}	Acquisition Time	$t_{ACQ} = t_{CYC} – t_{HOLD}$ (Note 10)	●	1.25			µs
t_{HOLD}	Maximum Time Between Acquisitions		●			750	ns
t_{CYC}	Time Between Conversions		●	2			µs
t_{CNVH}	CNV High Time		●	20			ns
t_{BUSYLH}	CNV ↑ to BUSY Delay	C_L = 20pF (Note 11)	●			20	ns
t_{CNVL}	Minimum Low Time for CNV	(Note 11)	●	200			ns

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SCK}	SCK Period	(Notes 11, 12)	●	10			ns
t_{SCKH}	SCK High Time		●	4			ns
t_{SCKL}	SCK Low Time		●	4			ns
$t_{SSDISCK}$	SDI Setup Time From SCK ↑	(Note 11)	●	4			ns
$t_{HSDISCK}$	SDI Hold Time From SCK ↑	(Note 11)	●	1			ns
t_{SCKCH}	SCK Period in Chain Mode	$t_{SCKCH} = t_{SSDISCK} + t_{DSDO}$ (Note 11)	●	13.5			ns
t_{DSDO}	SDO Data Valid Delay from SCK ↑	C_L = 20pF (Note 11)	●			9.5	ns
t_{HSDO}	SDO Data Remains Valid Delay from SCK ↑	C_L = 20pF (Note 10)	●	1			ns
$t_{DSDOBUSYL}$	SDO Data Valid Delay from BUSY ↓	C_L = 20pF (Note 10)	●			5	ns
t_{EN}	Bus Enable Time After RDL ↓	(Note 11)	●			16	ns
t_{DIS}	Bus Relinquish Time After RDL ↑	(Note 11)	●			13	ns
$t_{SSCKRDL}$	SCK Setup Time from RDL/SDI ↓	(Note 10)	●	1			ns
$t_{HSCKRDL}$	SCK Hold Time from RDL/SDI ↓	(Note 10)	●	16			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground.

Note 3: When these pin voltages are taken below ground or above REF or OV_{DD}, they will be clamped by internal diodes. This product can handle input currents up to 100mA below ground or above REF or OV_{DD} without latch-up.

Note 4: V_{DD} = 2.5V, OV_{DD} = 2.5V, REF = 2.5V, f_{SMPL} = 500kHz.

Note 5: Recommended operating conditions.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Bipolar zero-scale error is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111. Full-scale bipolar error is the worst-case of –FS or +FS untrimmed deviation from ideal first and last code transitions and includes the effect of offset error.

Note 8: All specifications in dB are referred to a full-scale ±2.5V input with a 2.5V reference voltage.

Note 9: f_{SMPL} = 500kHz, I_{REF} varies proportionately with sample rate.

Note 10: Guaranteed by design, not subject to test.

Note 11: Parameter tested and guaranteed at OV_{DD} = 1.71V, OV_{DD} = 2.5V and OV_{DD} = 5.25V.

Note 12: t_{SCK} of 10ns maximum allows a shift clock frequency up to 100MHz for rising capture.

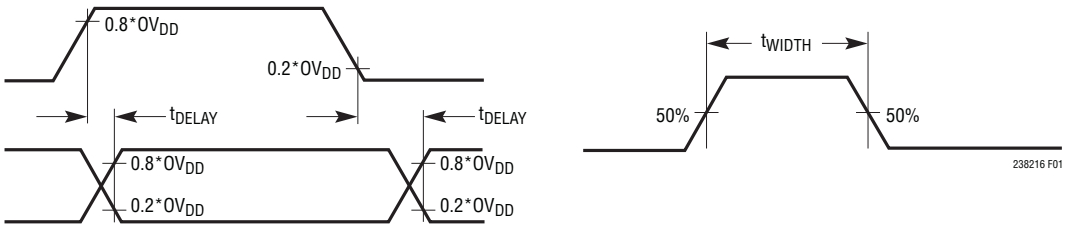
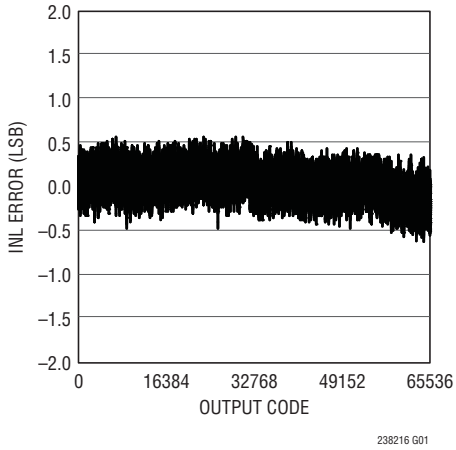


Figure 1. Voltage Levels for Timing Specifications

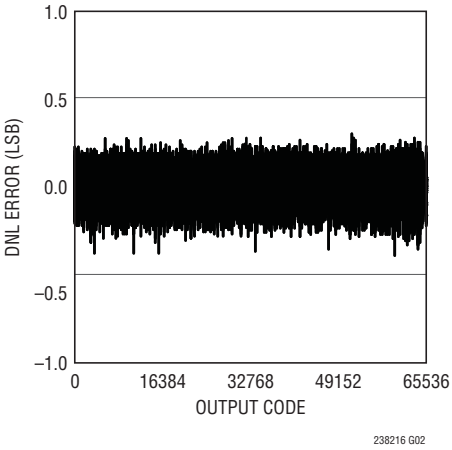
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 2.5V, OV_{DD} = 2.5V, REF = 2.5V, f_{SMPL} = 500ksps, unless otherwise noted.

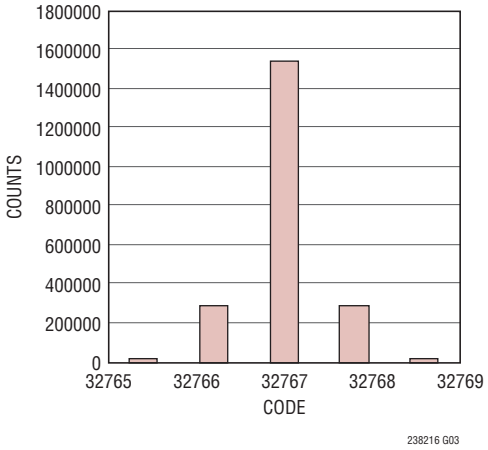
Integral Nonlinearity vs Output Code



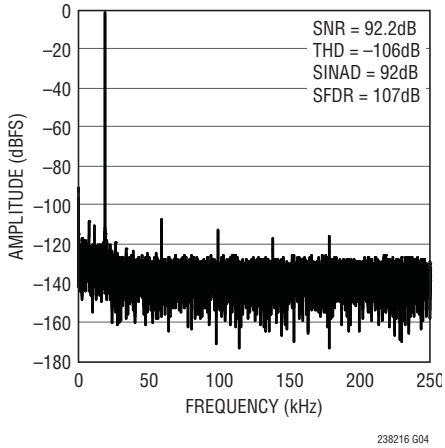
Differential Nonlinearity vs Output Code



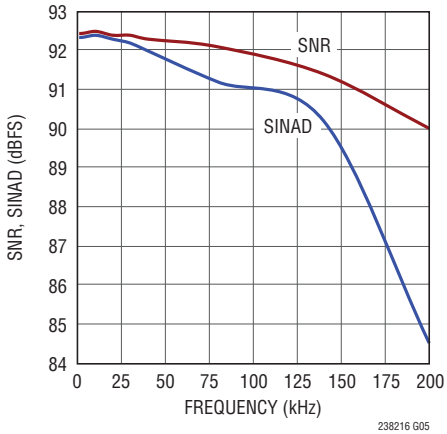
DC Histogram



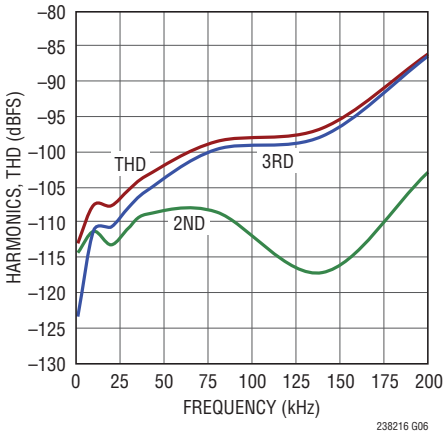
32k Point FFT f_S = 500Ksps, f_{IN} = 20kHz



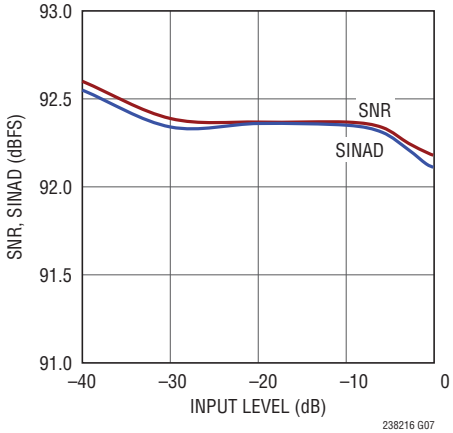
SNR, SINAD vs Input Frequency



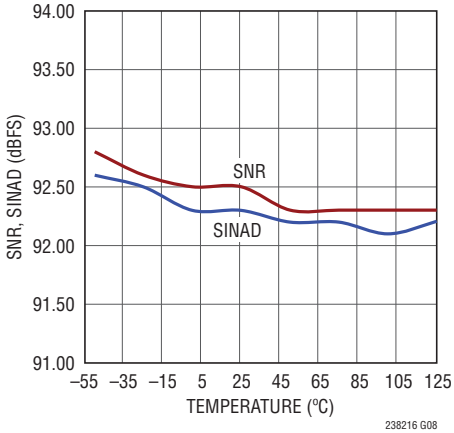
THD, Harmonics vs Input Frequency



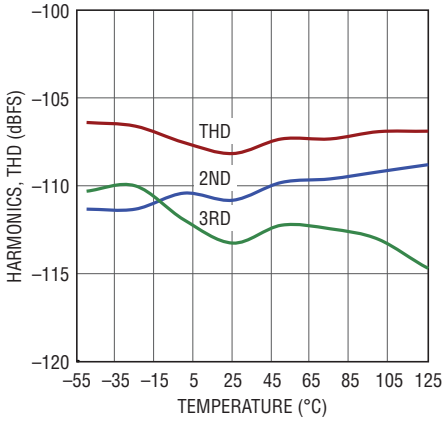
SNR, SINAD vs Input level, f_{IN} = 20kHz



SNR, SINAD vs Temperature



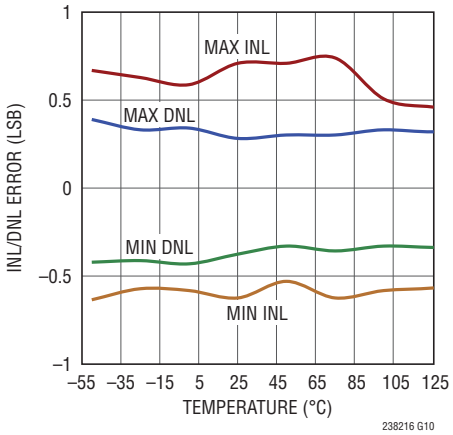
THD, Harmonics vs Temperature



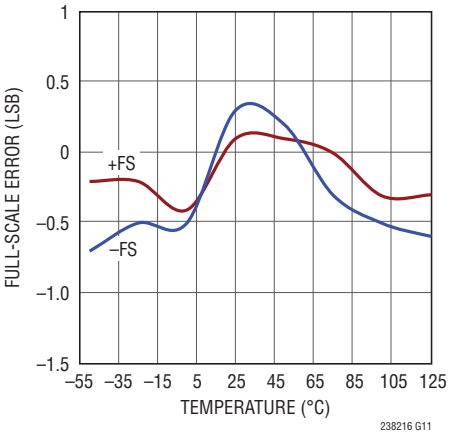
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 2.5V, OV_{DD} = 2.5V, REF = 2.5V, f_{SMPL} = 500ksps, unless otherwise noted.

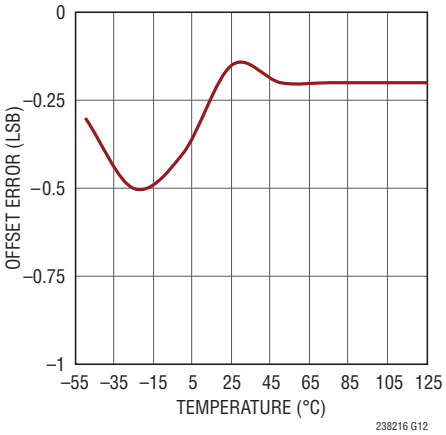
INL/DNL vs Temperature



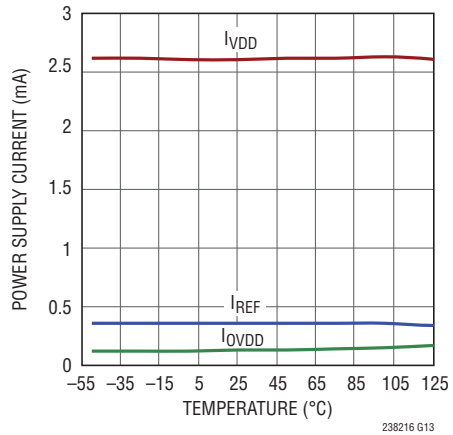
Full-Scale Error vs Temperature



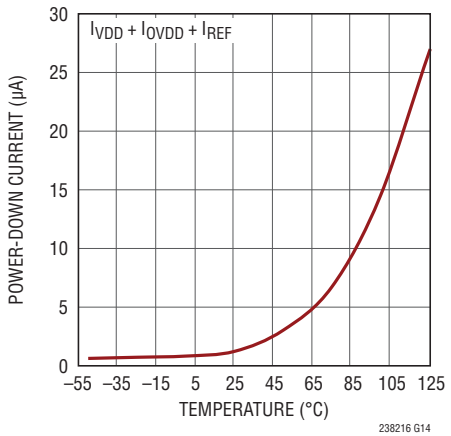
Offset Error vs Temperature



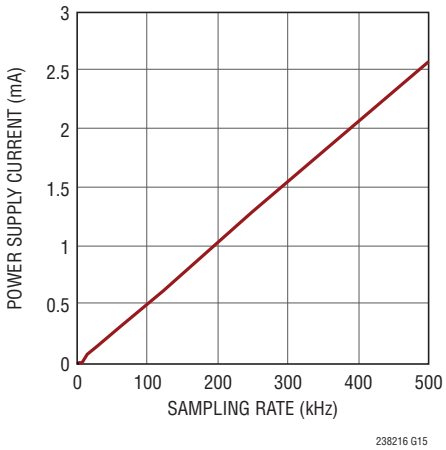
Supply Current vs Temperature



Shutdown Current vs Temperature



Supply Current vs Sampling Rate



PIN FUNCTIONS

CHAIN (Pin 1): Chain Mode Selector Pin. When low, the LTC2382-16 operates in Normal Mode and the RDL/SDI input pin functions to enable or disable SDO. When high, the LTC2382-16 operates in Chain Mode and the RDL/SDI pin functions as SDI, the daisychain serial data input.

V_{DD} (Pin 2): 2.5V Digital Power Supply. The range of V_{DD} is 2.375V to 2.625V. Bypass V_{DD} to GND with a 10µF ceramic capacitor.

GND (Pins 3, 6, 10 and 16): Ground.

IN^+, IN^- (Pins 4, 5): Positive and Negative Differential Analog Inputs.

REF (Pins 7, 8): Reference Input. The range of REF is 2.4V to 2.6V. This pin is referred to the GND pin and should be decoupled closely to the pin with a 47µF ceramic capacitor (X5R, 0805 size).

CNV (Pin 9): Convert Input. A rising edge on this input initiates a new conversion. When the conversion is done, the part powers down as long as CNV is held high. When CNV is returned low, the part powers up in preparation for the next conversion.

BUSY (Pin 11): BUSY indicator. Goes high at the start of a new conversion and returns low when the conversion has finished.

RDL/SDI (Pin 12): When CHAIN is low, the part is in Normal Mode and the pin is treated as a bus enabling input. When CHAIN is high, the part is in chain mode and the pin is treated as a serial data input pin where data from another ADC in the daisychain is input.

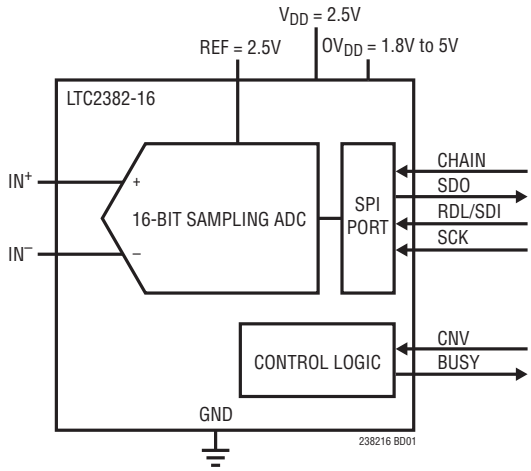
SCK (Pin 13): Serial Data Clock Input. When SDO is enabled, the conversion result or daisychain data from another ADC is shifted out on the rising edges of this clock MSB first.

SDO (Pin 14): Serial Data Output. The conversion result or daisychain data is output on this pin on each rising edge of SCK MSB first. The output data is in 2's complement format.

OV_{DD} (Pin 15): I/O Interface Digital Power. The range of OV_{DD} is 1.71V to 5.25V. This supply is nominally set to the same supply as the host interface (1.8V, 2.5V, 3.3V, or 5V). Bypass OV_{DD} to GND with a 0.1µF capacitor.

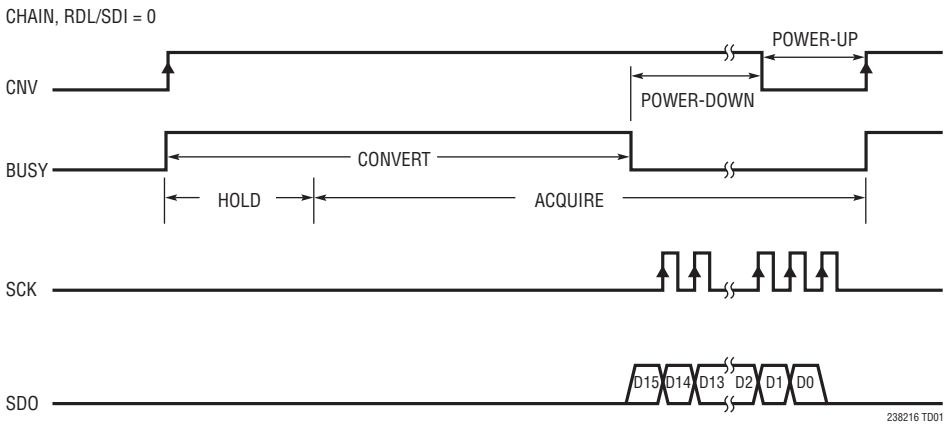
GND (Exposed Pad Pin 17 – DFN Package Only): Ground. Exposed pad must be soldered directly to the ground plane.

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAM

Conversion Timing Using the Serial Interface



APPLICATIONS INFORMATION

OVERVIEW

The LTC2382-16 is a low noise, low power, high speed 16-bit successive approximation register (SAR) ADC. Operating from a single 2.5V supply, the LTC2382-16 supports a large ±2.5V fully differential input range, making it ideal for high performance applications which require a wide dynamic range. The LTC2382-16 achieves ±2LSB INL max, no missing codes at 16-bits and 92dB SNR.

Fast 500ksps throughput with no cycle latency makes the LTC2382-16 ideally suited for a wide variety of high speed applications. An internal oscillator sets the conversion time, easing external timing considerations. The LTC2382-16 dissipates only 6.5mW at 500ksps, while an auto power-down feature is provided to further reduce power dissipation during inactive periods.

The LTC2382-16 features a proprietary sampling architecture that enables the ADC to begin acquiring the next sample during the current conversion. The resulting extended acquisition time of 1.25µs allows the use of extremely low power ADC drivers.

CONVERTER OPERATION

A rising edge on the CNV pin initiates a conversion. During the conversion phase, the 16-bit CDAC is sequenced through a successive approximation algorithm, effectively comparing the sampled input with binary-weighted fractions of the reference voltage (e.g. $V_{REF}/2$, $V_{REF}/4$ … $V_{REF}/65536$) using the differential comparator. At the end of conversion, the CDAC output approximates the sampled analog input. The ADC control logic then prepares the 16-bit digital output code for serial transfer.

TRANSFER FUNCTION

The LTC2382-16 digitizes the full-scale voltage of 2 × REF into 2^{16} levels, resulting in an LSB size of 76µV with REF = 2.5V. The ideal transfer function is shown in Figure 2. The output data is in 2's complement format.

ANALOG INPUT

The analog inputs of the LTC2382-16 are fully differential in order to maximize the signal swing that can be digitized. The analog inputs can be modeled by the equivalent

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circuit shown in Figure 3. The diodes at the input provide ESD protection. In the acquisition phase, each input sees approximately 45pF (C_{IN}) from the sampling CDAC in series with 40Ω (R_{ON}) from the on-resistance of the sampling switch. Any unwanted signal that is common to both inputs will be reduced by the common mode rejection of the ADC. The inputs draw a current spike while charging the C_{IN} capacitors during acquisition. When the LTC2382-16 is not acquiring the input, the analog inputs draw only a small leakage current.

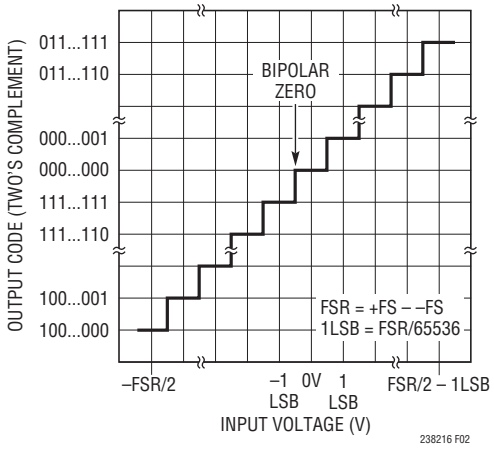

Figure 2. LTC2382-16 Transfer Function

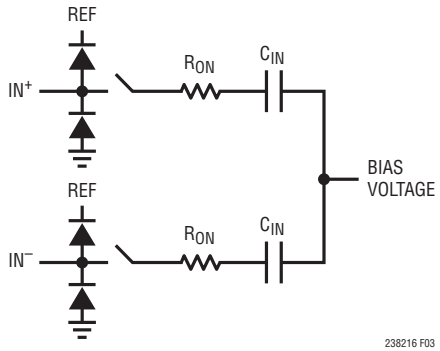

Figure 3. The Equivalent Circuit for the Differential Analog Input of the LTC2382-16

INPUT DRIVE CIRCUITS

A low impedance source can directly drive the high impedance inputs of the LTC2382-16 without gain error. A high impedance source should be buffered to minimize settling time during acquisition and to optimize the distortion performance of the ADC. Minimizing settling time is important even for DC inputs, because the ADC inputs draw a current spike when entering acquisition.

For best performance, a buffer amplifier should be used to drive the analog inputs of the LTC2382-16. The amplifier provides low output impedance which produces fast settling of the analog signal during the acquisition phase. It also provides isolation between the signal source and the current spike the ADC inputs draw.

Input Filtering

The noise and distortion of the buffer amplifier and signal source must be considered since they add to the ADC noise and distortion. Noisy input signals should be filtered prior to the buffer amplifier input with an appropriate filter to minimize noise. The simple 1-pole RC lowpass filter (LPF1) shown in Figure 4 is sufficient for many applications.

Another filter network consisting of LPF2 and the 100Ω series input resistors should be used between the buffer and ADC inputs to both minimize the noise contribution of the buffer and to help minimize disturbances reflected into the buffer from sampling transients. Long RC time constants at the analog inputs will slow down the settling of the analog inputs. Therefore, LPF2 requires a wider bandwidth than LPF1. A buffer amplifier with a low noise density must be selected to minimize degradation of the SNR. With the 482kHz lowpass filter shown in Figure 4, the LT6350 provides the full data sheet performance of the LTC2382-16.

High quality capacitors and resistors should be used in the RC filters since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

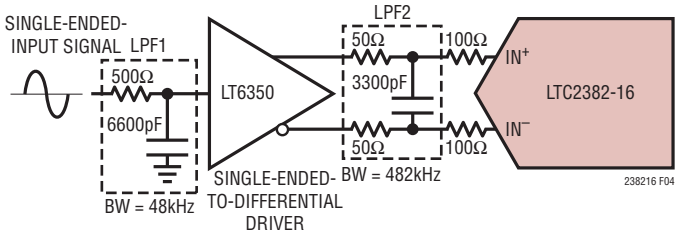

Figure 4. Input Signal Chain

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Single-to-Differential Conversion

For single-ended input signals, a single-ended to differential conversion circuit must be used to produce a differential signal at the inputs of the LTC2382-16. The LT6350 ADC driver is recommended for performing single-ended-to-differential conversions.The LT6350 is flexible and may be configured to convert single-ended signals of various amplitudes to the ±2.5V differential input range of the LTC2382-16. The LT6350 is also available in H-grade to complement the extended temperature operation of the LTC2382-16 up to 125°C.

Figure 5 shows the LT6350 being used to convert a 0V to 2.5V single-ended input signal. In this case, the first amplifier is configured as a unity gain buffer and the single-ended input signal directly drives the high-impedance input of the amplifier. As shown in the FFT of Figure 5a, the LT6350 drives the LTC2382-16 to full datasheet performance without degrading the SNR or THD.

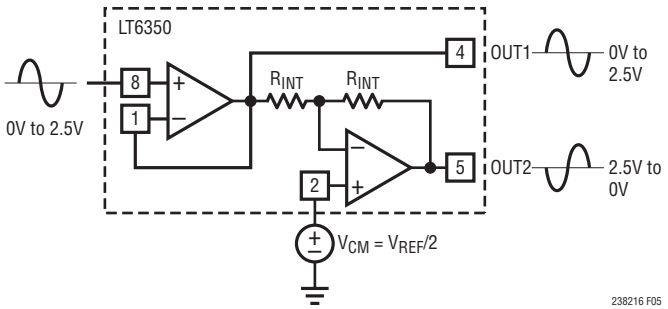

Figure 5. LT6350 Converting a 0V-2.5V Single-Ended Signal to a ±2.5V Differential Input Signal

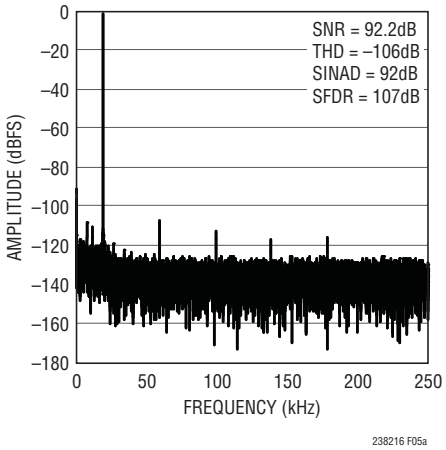

Figure 5a.32k Point FFT Plot for Circuit Shown in Figure 5

The LT6350 can also be used to buffer and convert single-ended signals larger than the input range of the LTC2382-16 in order to maximize the signal swing that can be digitized. Figure 6 shows the LT6350 converting a 0V-5V single-ended input signal to the ±2.5V differential input range of the LTC2382-16. In this case, the first amplifier in the LT6350 is configured as an inverting amplifier stage, which acts to attenuate the input signal down to the 0V-2.5V input range of the LTC2382-16. In the inverting amplifier configuration, the single-ended input signal source no longer directly drives a high impedance input of the first amplifier. The input impedance is instead set by resistor R_{IN}. R_{IN} must be chosen carefully based on the source impedance of the signal source. Higher values of R_{IN} tend to degrade both the noise and distortion of the LT6350 and LTC2382-16 as a system. R1, R2 and R3 must be selected in relation to R_{IN} to achieve the desired attenuation and to maintain a balanced input impedance in the first amplifier. Table 1 shows the resulting SNR and THD for several values of R_{IN}, R1, R2 and R3 in this configuration. Figure 6a shows the resulting FFT when using the LT6350 as shown in Figure 6.

The LT6350 can also be used to buffer and convert large, true bipolar signals which swing below ground to the ±2.5V differential input range of the LTC2382-16. Figure 7 shows the LT6350 being used to convert a ±10V true bipolar signal for use by the LTC2382-16. The input impedance is again set by resistor R_{IN}. Table 2 shows the resulting SNR and THD for several values of R_{IN}. Figure 7a shows the resulting FFT when using the LT6350 as shown in Figure 7.

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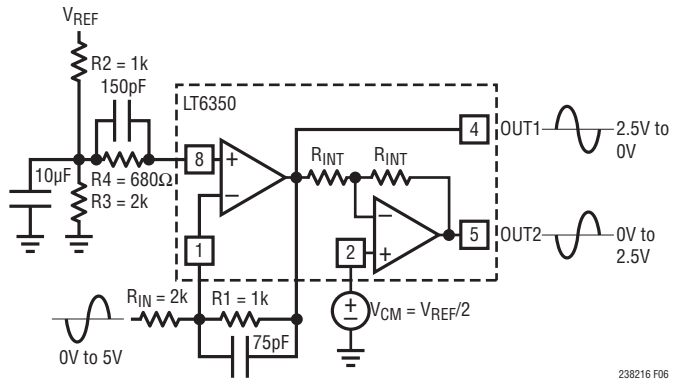

Figure 6. LT6350 Converting a 0V-5V Single-Ended Signal to a ±2.5V Differential Input Signal

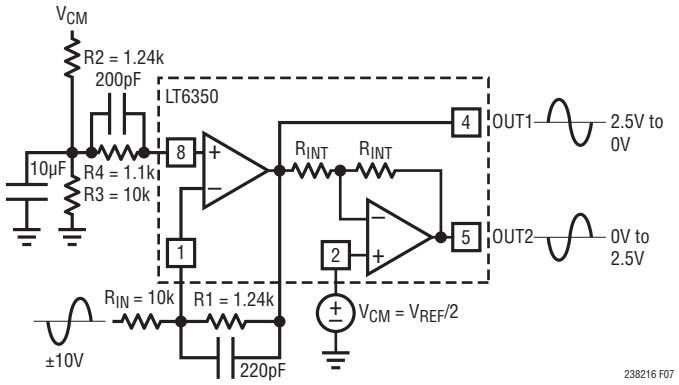

Figure 7. LT6350 Converting a ±10V Single-Ended Signal to a ±2.5V Differential Input Signal

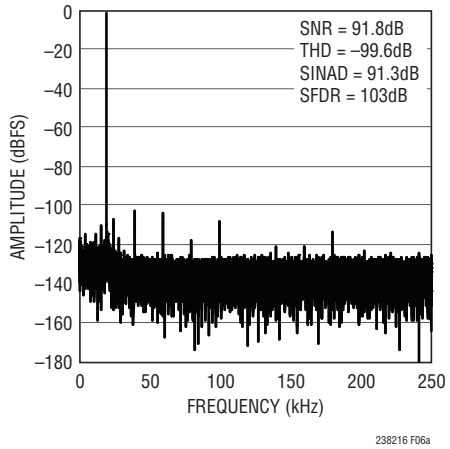

Figure 6a. 32k Point FFT Plot for Circuit Shown in Figure 6

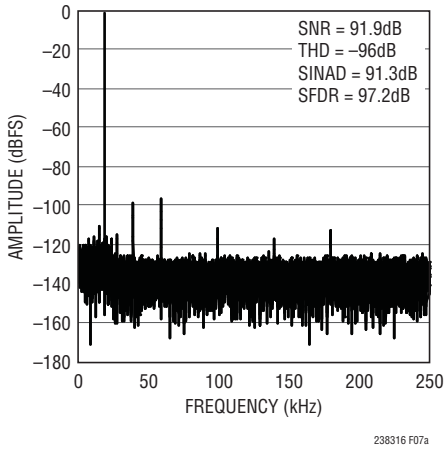

Figure 7a. 32k Point FFT Plot for Circuit Shown in Figure 7

Table 1. SNR, THD vs R_{IN} for 0-5V Single-Ended Input Signal

R_{IN} (Ω)	R1 (Ω)	R2 (Ω)	R3 (Ω)	R4 (Ω)	SNR (dB)	THD (dB)
2k	1k	1k	2k	680	92	–100
10k	5k	5k	10k	3.3k	91	–100
50k	25k	25k	50k	16.5k	91	–97

Table 2. SNR, THD vs R_{IN} for ±10V Single-Ended Input Signal

R_{IN} (Ω)	R1 (Ω)	R2 (Ω)	R3 (Ω)	R4 (Ω)	SNR (dB)	THD (dB)
10k	1.24k	1.24k	10k	1.1k	92	–96
50k	6.19k	6.19k	50k	5.49k	91	–96
100k	12.4k	12.4k	100k	11k	91	–97

ADC REFERENCE

The LTC2382-16 requires an external reference to define its input range. A low noise, low temperature drift reference is critical to achieving the full datasheet performance of the ADC. Linear Technology offers a portfolio of high performance references designed to meet the needs of many applications. With its small size, low power and high accuracy, the LTC6652-2.5 is particularly well suited for use with the LTC2382-16. The LTC6652-2.5 offers 0.05% (max) initial accuracy and 5ppm/°C (max) temperature coefficient for high precision applications. The LTC6652-2.5 is fully specified over the H-grade temperature range and complements the extended temperature operation of the LTC2382-16 up to 125°C. We recommend bypassing the LTC6652-2.5 with a 47µF ceramic capacitor (X5R, 0805 size) close to the REF pin. All performance curves shown in this datasheet were obtained using the LTC6652-2.5.

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The REF pin of the LTC2382-16 draws charge (Q_{CONV}) from the 47µF bypass capacitor during each conversion cycle. The reference replenishes this charge with a DC current, $I_{REF} = Q_{CONV}/t_{CYC}$. The DC current draw of the REF pin, I_{REF}, depends on the sampling rate and output code. If the LTC2382-16 is used to continuously sample a signal at a constant rate, the LTC6652-2.5 will keep the deviation of the reference voltage over the entire code span to less than 0.5LSBs.

When idling, the REF pin on the LTC2382-16 draws only a small leakage current (< 1µA). In applications where a burst of samples is taken after idling for long periods as shown in Figure 8, I_{REF} quickly goes from approximately 0µA to a maximum of 495µA at 500ksps. This step in DC current draw triggers a transient response in the reference that must be considered since any deviation in the reference output voltage will affect the accuracy of the output code. In applications where the transient response of the reference is important, the fast settling LTC6655-2.5 reference is recommended. Inserting a 1Ω resistor between the 47µF bypass capacitor and reference output as shown in Figure 9 helps to improve the transient settling time and minimize the reference voltage deviation.

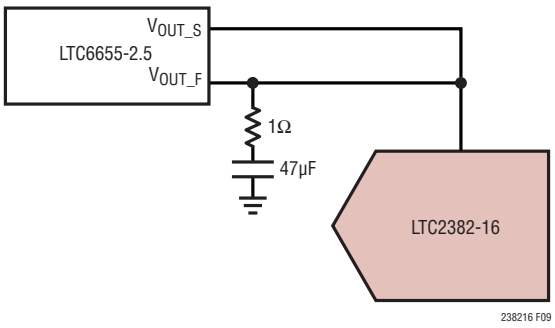

Figure 9. LTC6655-2.5 Driving REF of LTC2382-16

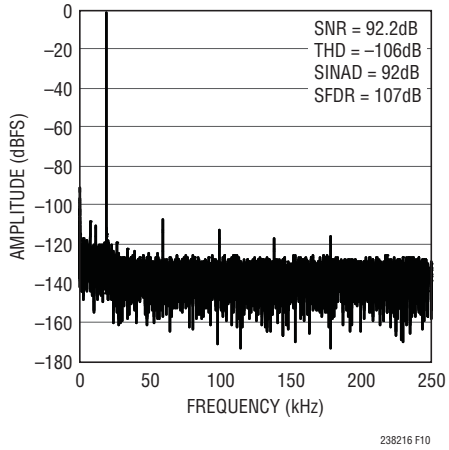

Figure 10. 32k Point FFT of the LTC2382-16

DYNAMIC PERFORMANCE

Fast Fourier Transform (FFT) techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. The LTC2382-16 provides guaranteed tested limits for both AC distortion and noise measurements.

Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the A/D output. The output is band-limited to frequencies from above DC and below half the sampling frequency. Figure 10 shows that the LTC2382-16 achieves a typical SINAD of 92dB at a 500kHz sampling rate with a 20kHz input.

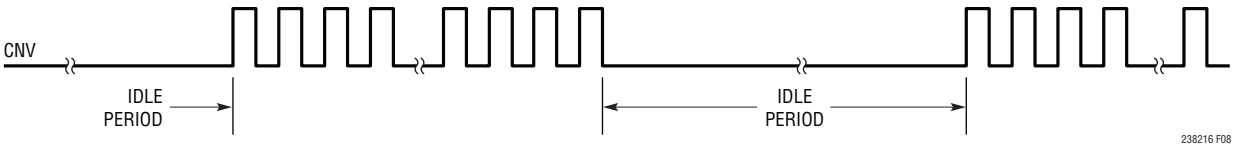

Figure 8. CNV Waveform Showing Burst Sampling

APPLICATIONS INFORMATION

Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC. Figure 10 shows that the LTC2382-16 achieves a typical SNR of 92dB at a 500kHz sampling rate with a 20kHz input.

Total Harmonic Distortion (THD)

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ($f_{SMPL}/2$). THD is expressed as:

$$THD = 20\log\frac{\sqrt{V2^2 + V3^2 + V4^2 + \ldots + V_N{}^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through V_N are the amplitudes of the second through Nth harmonics.

POWER CONSIDERATIONS

The LTC2382-16 provides two power supply pins: the 2.5V power supply (V_{DD}), and the digital input/output interface power supply (OV_{DD}). The flexible OV_{DD} supply allows the LTC2382-16 to communicate with any digital logic operating between 1.8V and 5V, including 2.5V and 3.3V systems.

Power Supply Sequencing

The LTC2382-16 does not have any specific power supply sequencing requirements. Care should be taken to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section. The LTC2382-16 has a power-on-reset (POR) circuit that will reset the LTC2382-16 at initial power-up or whenever the power supply voltage drops below 1V. Once the supply voltage reenters the nominal supply voltage range, the POR will reinitialize the ADC. No conversions should be initiated until 20µs after a POR event to ensure the reinitialization period has ended. Any conversions initiated before this time will produce invalid results.

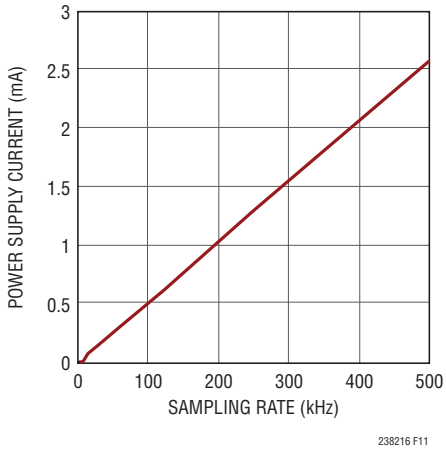

Figure 11. Power Supply Current of the LTC2382-16 vs Sampling Rate

TIMING AND CONTROL

CNV Timing

The LTC2382-16 conversion is controlled by CNV. A rising edge on CNV will start a conversion. Once a conversion has been initiated, it cannot be restarted until the conversion is complete. For optimum performance, CNV should be driven by a clean low jitter signal. Converter status is indicated by the BUSY output which remains high while the conversion is in progress. To ensure that no errors occur in the digitized results, any additional transitions on CNV should occur within 40ns from the start of the conversion or after the conversion has been completed.

ACQUISITION

A proprietary sampling architecture allows the LTC2382-16 to begin acquiring the input signal for the next conversion 750ns after the start of the current conversion. This extends the acquisition time to 1.25µs, easing settling requirements and allowing the use of extremely low power ADC drivers. (Refer to the Timing Diagram.)

Internal Conversion Clock

The LTC2382-16 has an internal clock that is trimmed to achieve a maximum conversion time of 1.5µs.

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Auto Power-Down

The LTC2382-16 automatically powers down after a conversion has been completed as long as CNV remains high. During power-down, the data from the last conversion can be clocked out. To minimize power dissipation during power-down, disable SDO and turn off SCK. To power up the part, bring CNV low at least 200ns (t_{CONVL}) before the initiation of the next conversion. The auto power-down feature will reduce the power dissipation of the LTC2382-16 as the sampling frequency is reduced. Since the time required to power up the part does not change at lower sample rates, the LTC2382-16 can remain powered-down for a larger fraction of the conversion cycle (t_{CYC}), thereby reducing the average power dissipation which scales linearly with sampling rate as shown in Figure 11.

DIGITAL INTERFACE

The LTC2382-16 has a serial digital interface. The flexible OV_{DD} supply allows the LTC2382-16 to communicate with any digital logic operating between 1.8V and 5V, including 2.5V and 3.3V systems.

The serial output data is clocked out on the SDO pin when an external clock is applied to the SCK pin if SDO is enabled. Clocking out the data after the conversion will yield the best performance. With a shift clock frequency of at least 30MHz, a 500ksps throughput is still achieved. The serial output data changes state on the rising edge of SCK and can be captured on the falling edge or next rising edge of SCK. D15 remains valid till the first rising edge of SCK.

The serial interface on the LTC2382-16 is simple and straightforward to use. The following sections describe the operation of the LTC2382-16. Several modes are provided depending on whether a single or multiple ADCs share the SPI bus or are daisy-chained.

TIMING DIAGRAM

Normal Mode, Single Device

When CHAIN = 0, the LTC2382-16 operates in Normal mode. In Normal mode, RDL/SDI enables or disables the serial data output pin SDO. If RDL/SDI is high, SDO is in high-impedance. If RDL/SDI is low, SDO is driven.

Figure 12 shows a single LTC2382-16 operated in Normal Mode with CHAIN and RDL/SDI tied to ground. With RDL/SDI grounded, SDO is enabled and the MSB(D15) of the new conversion data is available at the falling edge of BUSY. This is the simplest way to operate the LTC2382-16.

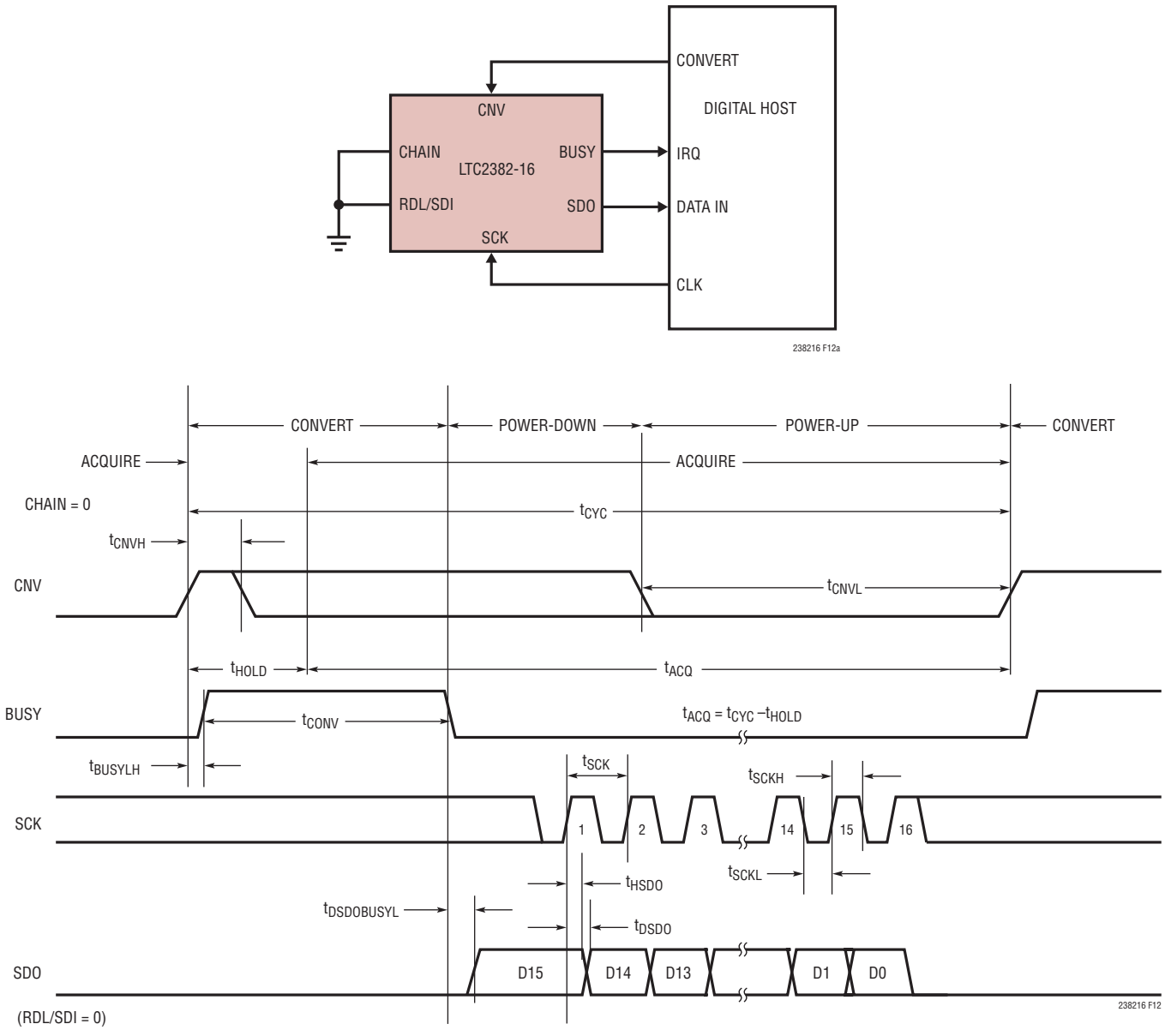


Figure 12. Using a Single LTC2382-16 in Normal Mode

TIMING DIAGRAM

Normal Mode, Multiple Devices

Figure 13 shows multiple LTC2382-16 devices operating in Normal Mode(CHAIN = 0) sharing CNV, SCK and SDO. By sharing CNV, SCK and SDO, the number of required signals to operate multiple ADCs in parallel is reduced. Since SDO is shared, the RDL/SDI input of each ADC must be used to allow only one LTC2382-16 to drive SDO at a time in order to avoid bus conflicts. As shown in Figure 13, the RDL/SDI inputs idle high and are individually brought low to read data out of each device between conversions. When RDL/SDI is brought low, the MSB of the selected device is output onto SDO. To ensure the MSB is properly output and captured, SCK must be held low at least 1ns before and 16ns after bringing RDL/SDI low.

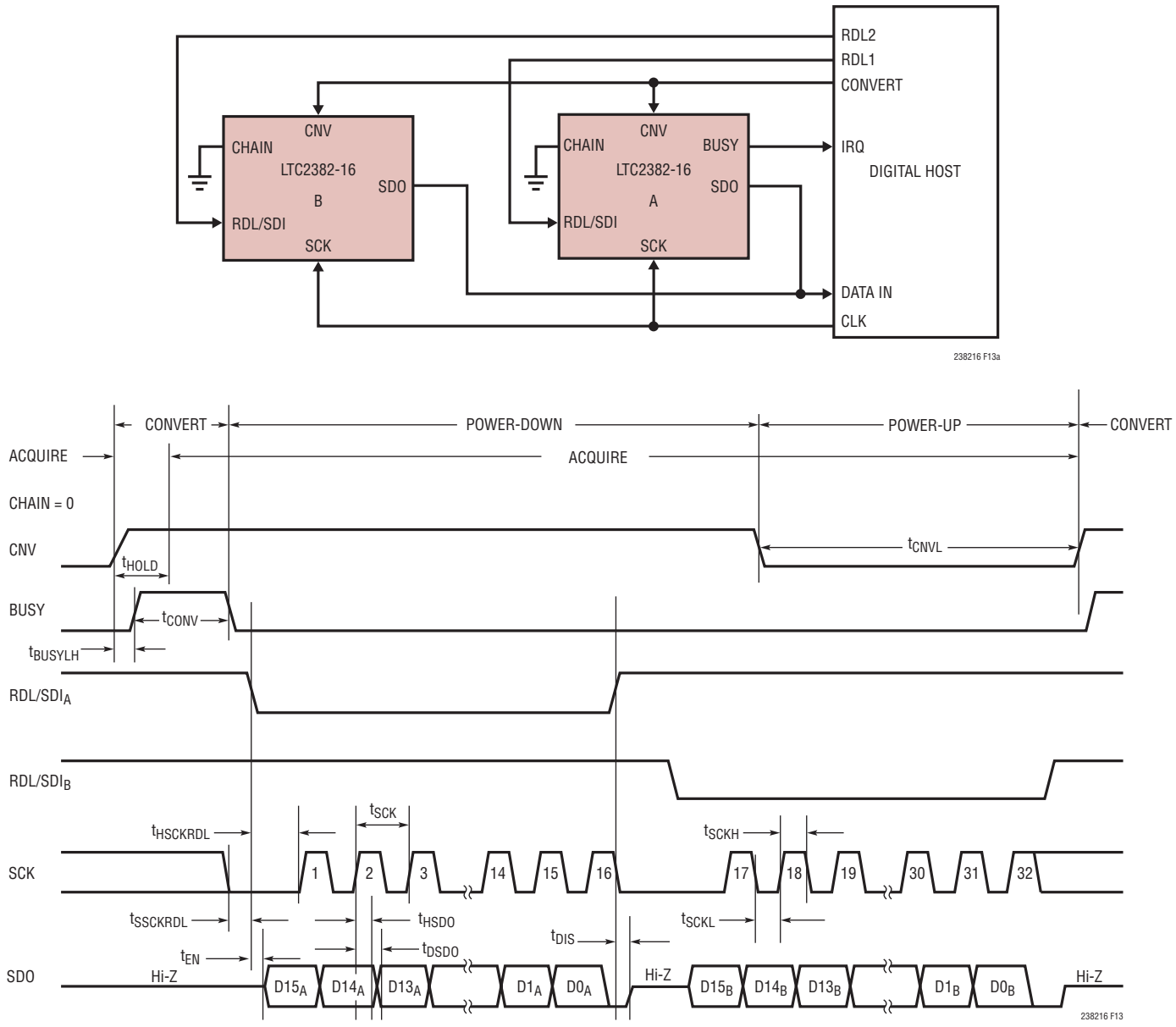


Figure 13. Normal Mode with Multiple Devices Sharing CNV, SCK and SDO

TIMING DIAGRAM

When CHAIN = OV_{DD}, the LTC2382-16 operates in Chain Mode. In Chain Mode, SDO is always enabled and RDL/SDI serves as the serial data input pin (SDI) where daisychain data output from another ADC can be input.

This is useful for applications where hardware constraints may limit the number of lines needed to interface to a large number of converters. Figure 14 shows an example with two daisy chained devices. The MSB of converter A will appear at SDO of converter B after 16 SCK cycles. The MSB of converter A is clocked in at the SDI/RDL pin of converter B on the rising edge of the first SCK.

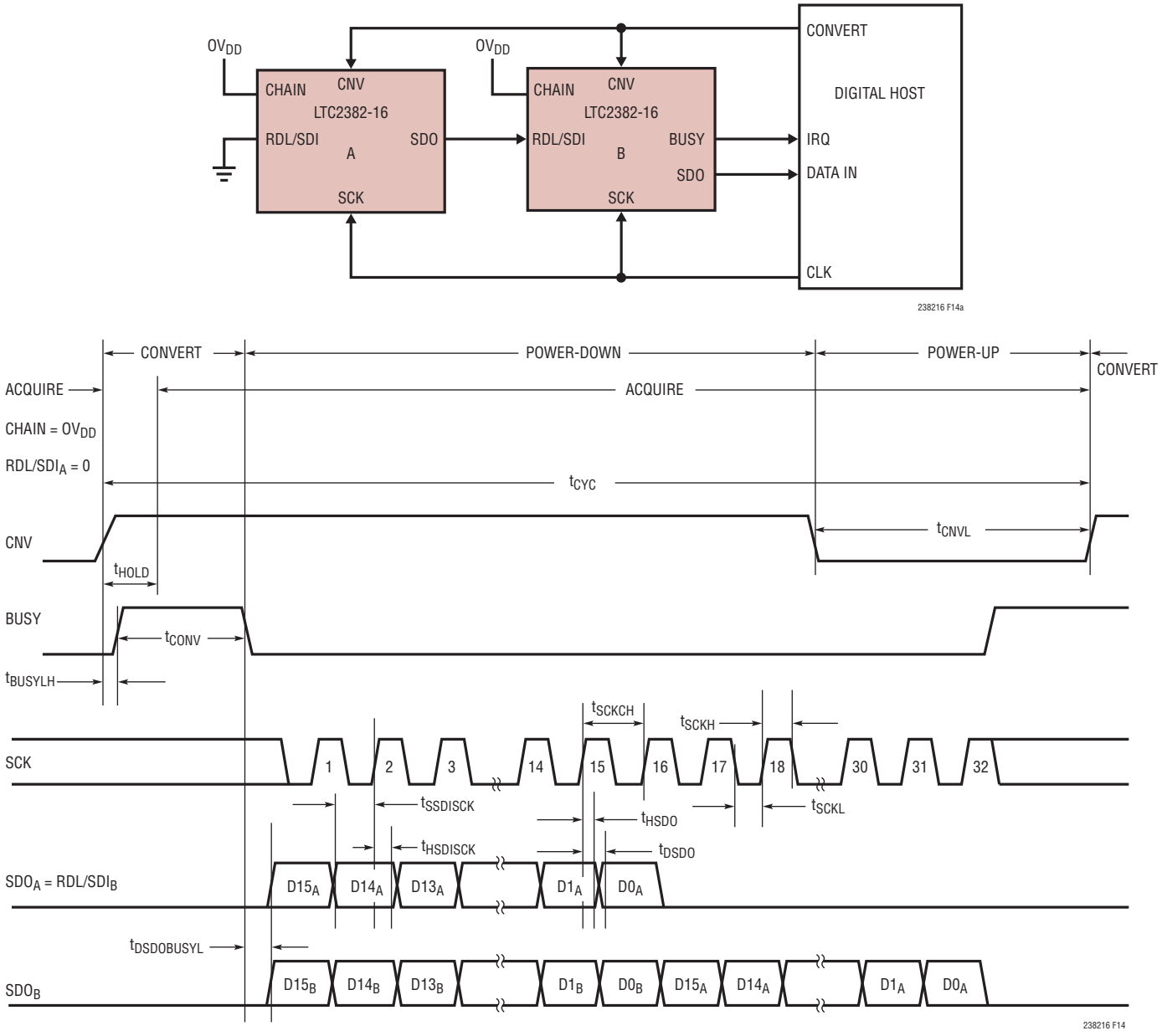


Figure 14. Chain Mode Timing Diagram

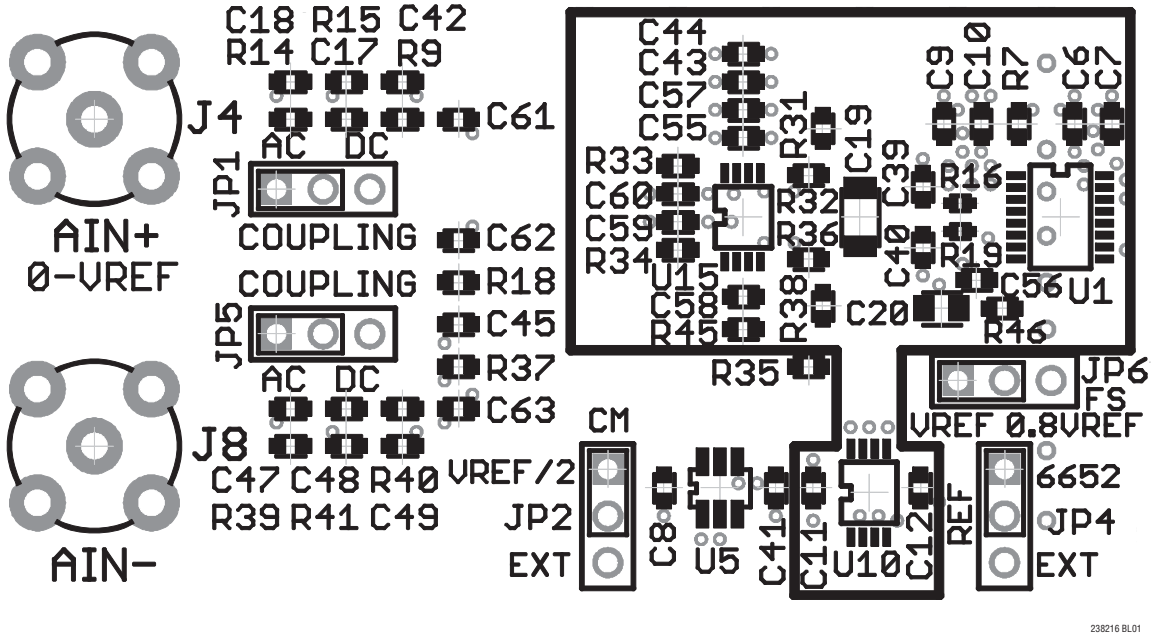
BOARD LAYOUT

To obtain the best performance from the LTC2382-16 a printed circuit board is recommended. Layout for the printed circuit board (PCB) should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital clocks or signals alongside analog signals or underneath the ADC.

Recommended Layout

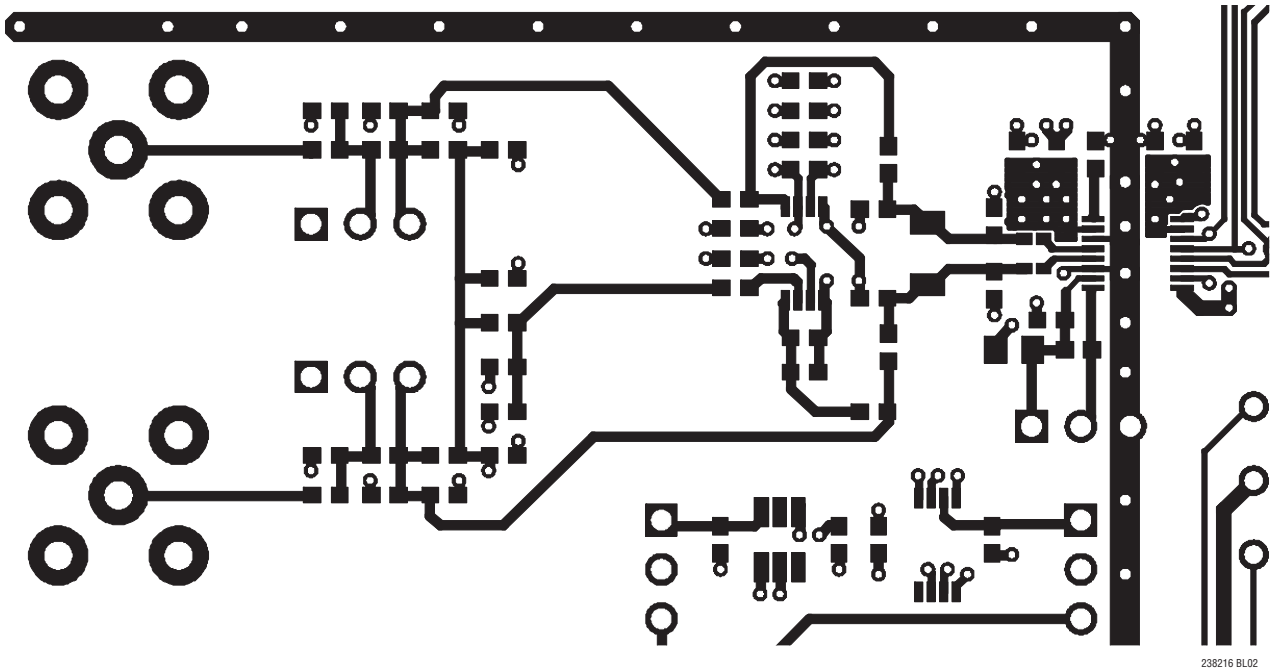
The following is an example of a recommended PCB layout. A single solid ground plane is used. Bypass capacitors to the supplies are placed as close as possible to the supply pins. Low impedance common returns for these bypass capacitors are essential to the low noise operation of the ADC. The analog input traces are screened by ground. For more details and information refer to DC1571A, the evaluation kit for the LTC2382-16.

Partial Top Silkscreen

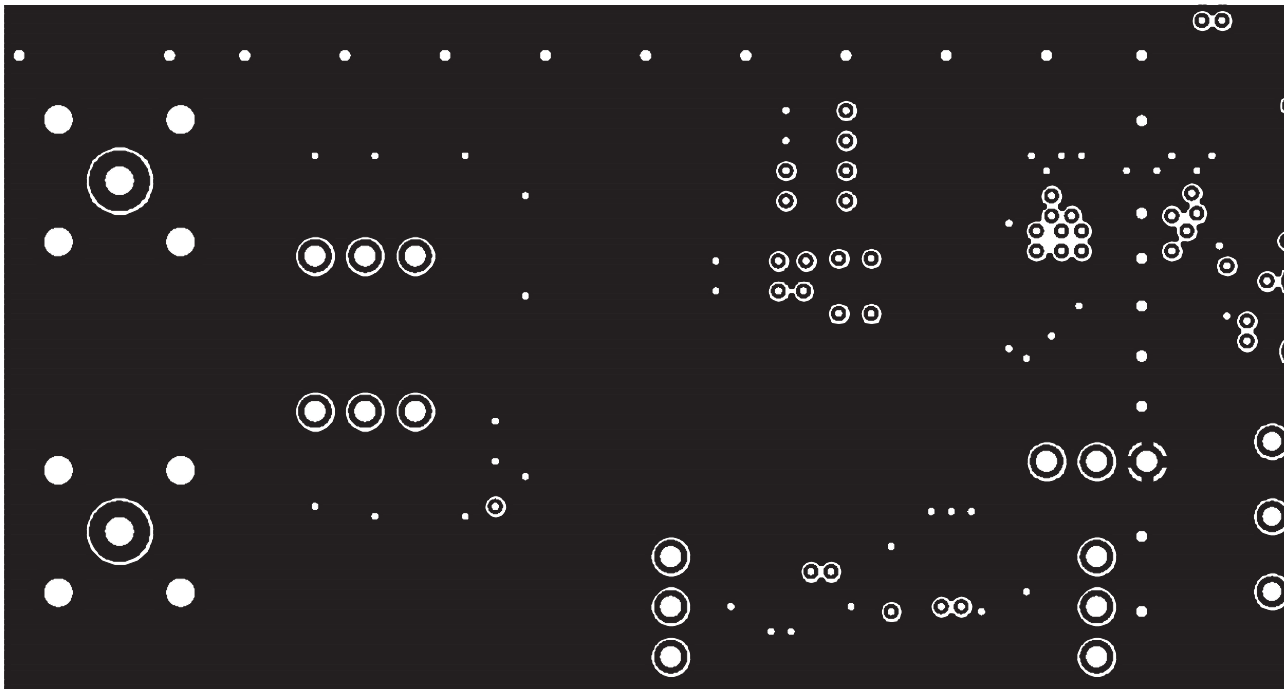


BOARD LAYOUT

Partial Layer 1 Component Side

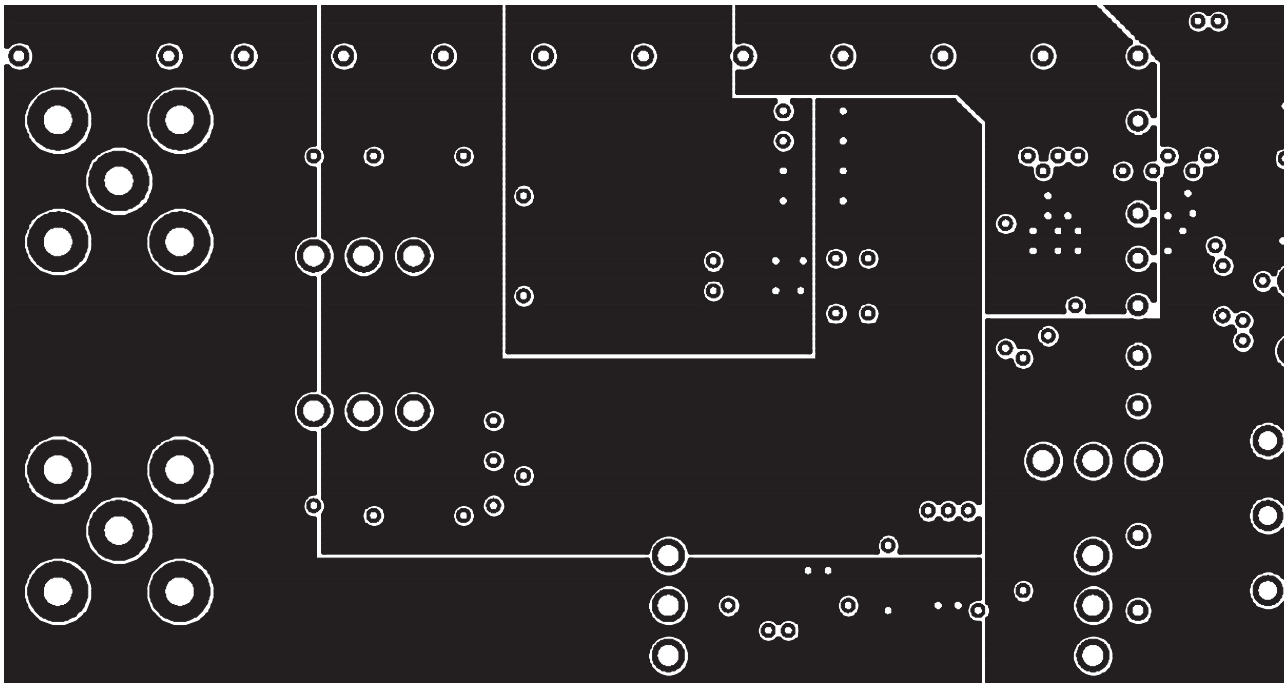


Partial Layer 2 Ground Plane



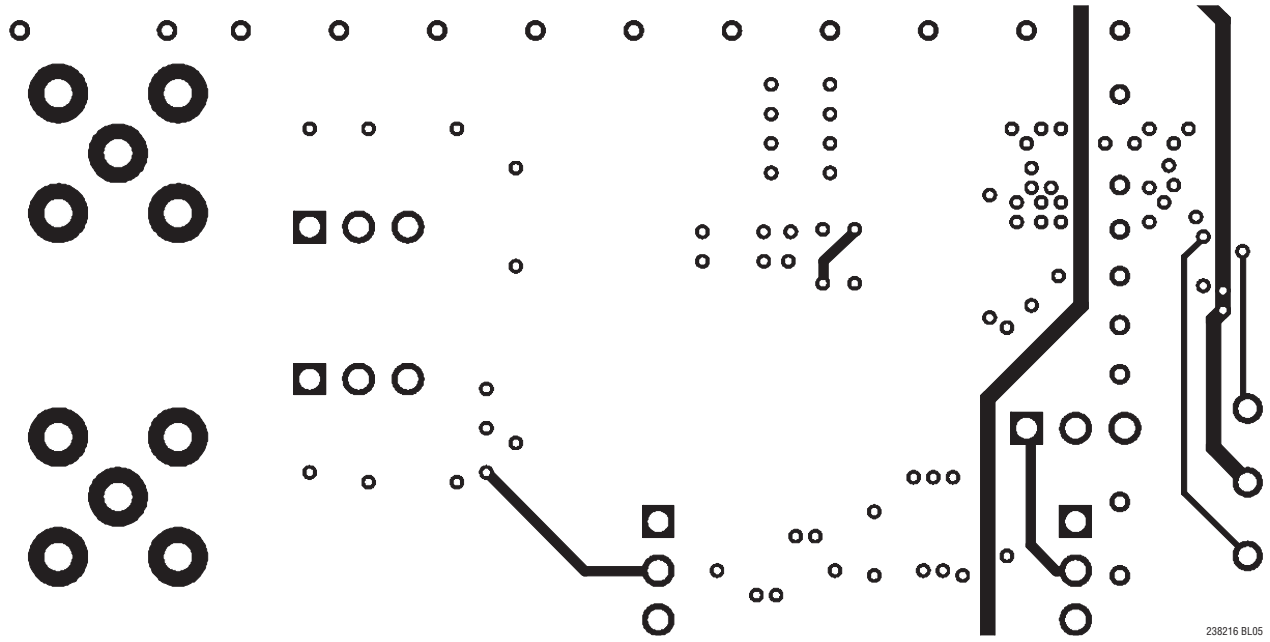
BOARD LAYOUT

Partial Layer 3 PWR Plane



238216 BL04

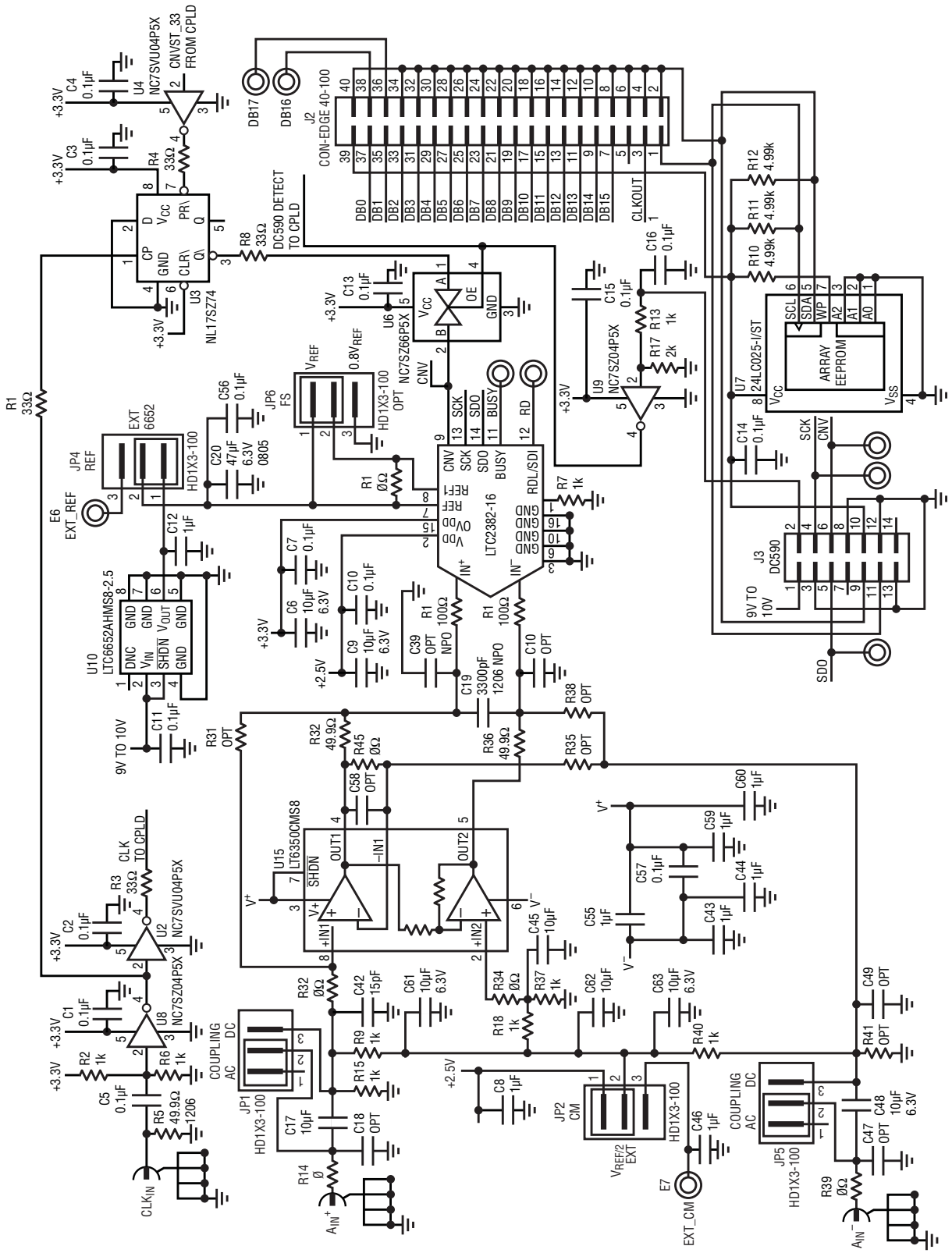
Partial Layer 4 Bottom Layer



238216 BL05

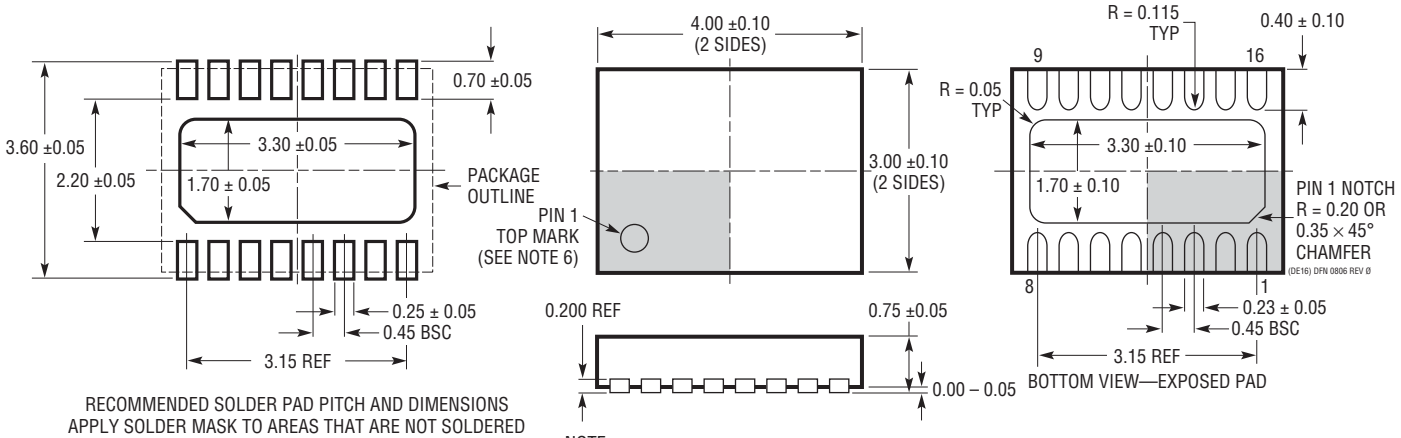
BOARD LAYOUT

Partial Schematic of Demoboard



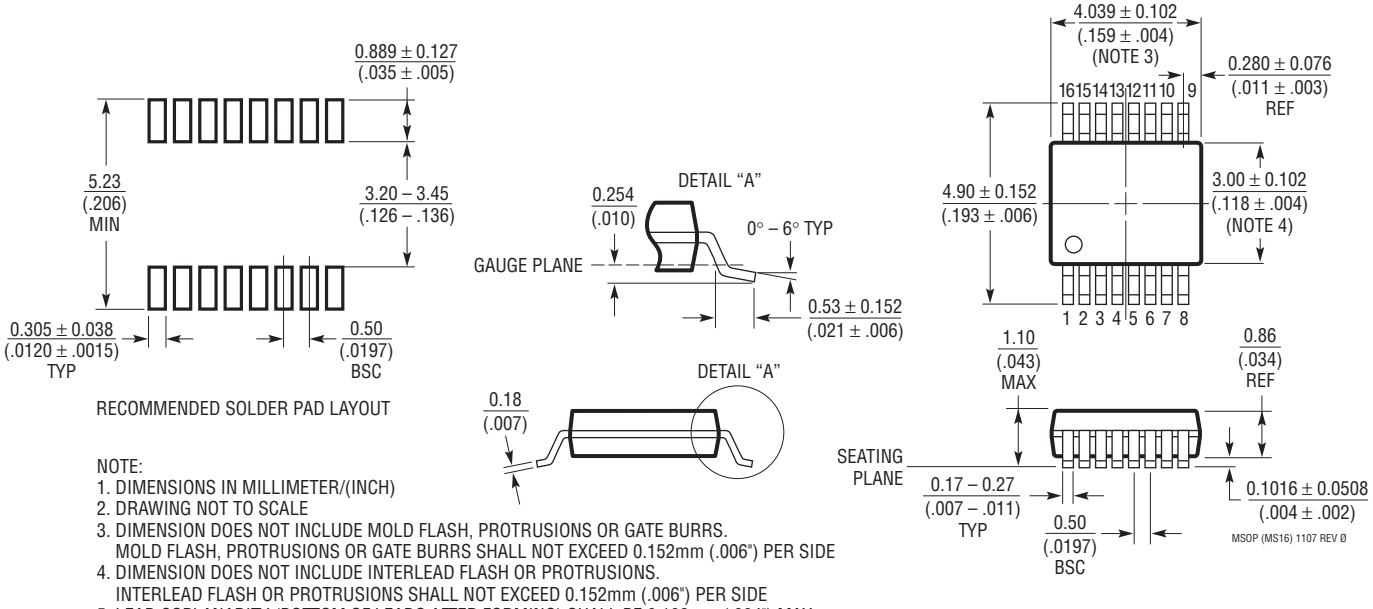
PACKAGE DESCRIPTION

DE Package
16-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1732 Rev Ø)



NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

MS Package
16-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1669 Rev Ø)

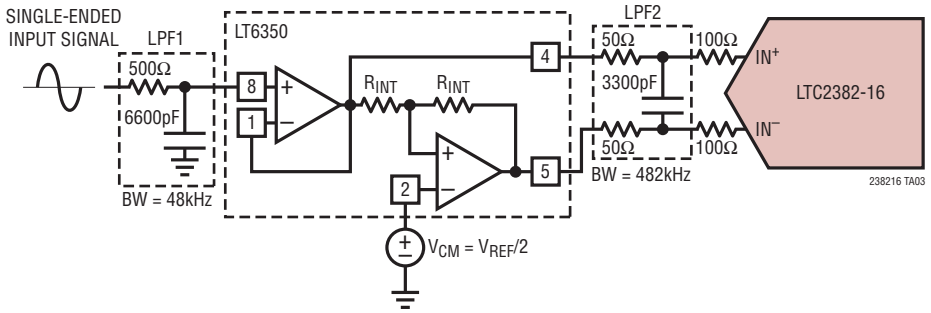


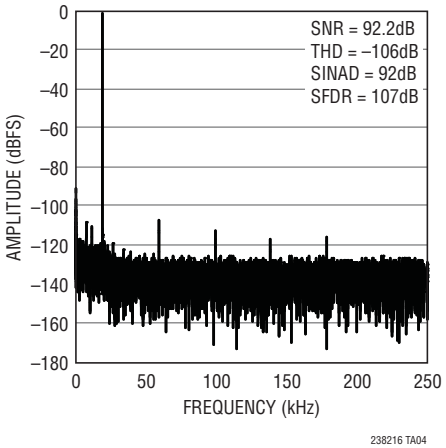
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

ADC Driver: Single-Ended Input to Differential Output with Filter





RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LT2383/LTC2381	16-Bit, 1Msps/250ksps Serial ADC	2.5V Supply, Differential Input, 92dB SNR, ±2.5V Input Range,16-Pin MSOP and 4mmx3mm16-Pin DFN Packages,Pin compatible with the LTC2382-16
LTC2393-16	16-Bit, 1Msps Parallel/Serial ADC	5V Supply, Differential Input, 94dB SNR, 4.096V Input Range, 48-Pin LQFP Package, Pin compatible with the LTC2392-16, LTC2391-16
LTC2392-16	16-Bit, 500Ksps Parallel/Serial ADC	5V Supply, Differential Input, 94dB SNR, 4.096V Input Range, 48-Pin LQFP Package, Pin compatible with the LTC2393-16, LTC2391-16
LTC2391-16	16-Bit, 250Ksps Parallel/Serial ADC	5V Supply, Differential Input, 94dB SNR, 4.096V Input Range, 48-Pin LQFP Package, Pin compatible with the LTC2393-16, LTC2392-16
LTC1864/LTC1864L	16-bit, 250ksps/150ksps 1-channel µPower, ADC	5V/3V Supply, 1-Channel, 4.3mW/1.3mW, MSOP-8 Package
LTC1865/LTC1865L	16-bit, 250ksps 2-channel µPower ADC	5V/3V Supply, 1-Channel, 4.3mW/1.3mW, MSOP-8 Package
LTC2302/LTC2306	12-Bit, 500ksps, 1-/2-Channel, Low Noise, ADC	5V Supply, 14mW at 500ksps, 10-pin DFN Package
LTC2355-14/LTC2356-14	14-Bit, 3.5Msps Serial ADC	3.3V Supply, 1-Channel, Unipolar/Bipolar, 18mW, MSOP-10 Package
LTC1417	14-Bit 400ksps Serial ADC	5V/±5V Supply, 1-Channel, Unipolar/Bipolar, 20mW, 16-Pin Narrow SSOP Package
DACs		
LTC2641	16-Bit Single Serial V_{OUT} DACs	±1LSB INL, ±1LSB DNL, MSOP-8 Package, 0V to 5V Output
LTC2630	12-/10-/8-Bit Single V_{OUT} DACs	SC70 6-Pin Package, Internal Reference, ±1LSB INL (12Bits)
REFERENCES		
LTC6652	Precision Low Drift Low Noise Buffered Reference	2.5V, 5ppm/°C Max Tempco, 2.1ppm Peak-to-Peak Noise, MSOP-8 Package
LTC6655	Precision Low Drift Low Noise Buffered Reference	2.5V, 5ppm/°C Max Tempco, 0.25ppm Peak-to-Peak Noise, MSOP-8 Package
AMPLIFIERS		
LT6350	Low Noise Single-Ended-To-Differential ADC Driver	Rail-to-Rail Input and Outputs, 240ns 0.01% Settling Time, DFN-8 or MSOP-8 Packages
LT6200/LT6200-5/ LT6200-10	165MHz/800MHz/1.6GHz Op Amp with Unity Gain/AV = 5/AV = 10	Low Noise Voltage: 0.95nV/√Hz (100kHz), Low Distortion: –80dB at 1MHz, TSOT23-6 Package
LT6202/LT6203	Single/Dual 100MHz Rail-to-Rail Input/Output Noise Low Power Amplifiers	1.9nV√Hz, 3mA Maximum, 100MHz Gain Bandwidth
LTC1992	Low Power, Fully Differential Input/Output Amplifier/Driver Family	1mA Supply Current

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