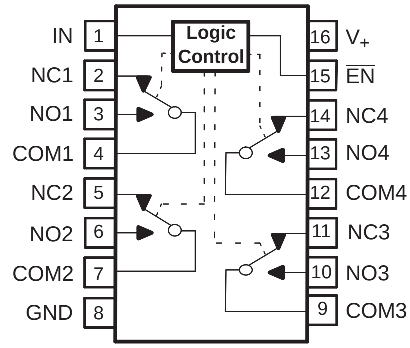
10-Ω QUAD SPDT ANALOG SWITCH

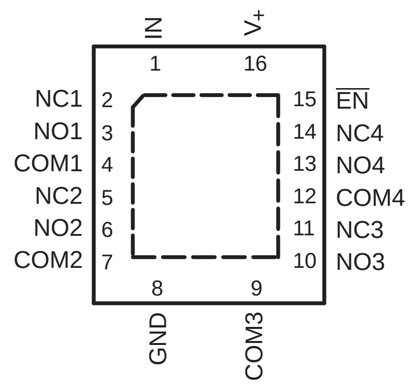
FEATURES

- Low ON-State Resistance (10 Ω)
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 2.3-V to 3.6-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

D, DBQ, DGV, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



APPLICATIONS

- Sample-and-Hold Circuits
- Battery-Powered Equipment
- Audio and Video Signal Routing
- Communication Circuits

DESCRIPTION/ORDERING INFORMATION

The TS3A5018 is a quad single-pole double-throw (SPDT) analog switch that is designed to operate from 2.3 V to 3.6 V. This device can handle both digital and analog signals, and signals up to V_+ can be transmitted in either direction.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Tube of 40	TS3A5018D	TS3A5018
		Reel of 2500	TS3A5018DR	
	SSOP (QSOP) – DBQ	Reel of 2500	TS3A5018DBQR	YA018
	TSSOP – PW	Tube of 90	TS3A5018PW	YA018
		Reel of 2000	TS3A5018PWR	
	TVSOP – DGV	Reel of 2000	TS3A5018DGVR	YA018
	QFN – RGY	Reel of 1000	TS3A5018RGYR	YA018
			TS3A5018RGYRG4	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

SUMMARY OF CHARACTERISTICS(1)

Configuration	Quad Single-Pole, Double Throw (4 × SPDT)
Number of channels	4
ON-state resistance (r_{on})	7 Ω
ON-state resistance match (Δr_{on})	0.3 Ω
ON-state resistance flatness ($r_{on(flat)}$)	5 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	3.5 ns/2 ns
Charge injection (Q_C)	2 pC
Bandwidth (BW)	300 MHz
OFF isolation (O_{ISO})	–48 dB at 10 MHz
Crosstalk (X_{TALK})	–48 dB at 10 MHz
Total harmonic distortion (THD)	0.2%
Leakage current ($I_{COM(OFF)}$	±5 μA
Power-supply current (I_+)	2.5 μA
Package options	16-pin QFN, SOIC, SSOP, TSSOP, or TVSOP

(1) $V_+ = 3.3$ V, $T_A = 25°C$

FUNCTION TABLE

$\overline{EN}$	IN	NO TO COM, COM TO NO	NC TO COM, COM TO NC
L	L	OFF	ON
L	H	ON	OFF
H	X	OFF	OFF

Absolute Minimum and Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range(3)		–0.5	4.6	V
V_{NC} V_{NO} V_{COM}	Analog voltage range(3)(4)		–0.5	4.6	V
I_K	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0	–50		mA
I_{NC} I_{NO} I_{COM}	On-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to 7 V	–64	64	mA
V_I	Digital input voltage range(3)(4)		–0.5	4.6	V
I_{IK}	Digital input clamp current	V_I < 0	–50		mA
I_+	Continuous current through V_+		–100	100	mA
I_{GND}	Continuous current through GND		–100	100	mA
θ_{JA}	Package thermal impedance(5)	D package		73	°C/W
		DBQ package		90	
		DGV package		120	
		PW package		108	
		RGY package		51	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Characteristics for 3.3-V Supply[(1)]

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	$0 \le (V_{NC}$ or $V_{NO}) \le V_+$, I_{COM} = –32 mA,	Switch ON, See Figure 13	25°C	3 V		7	10	Ω
				Full				12	
ON-state resistance match between channels	Δr_{on}	V_{NC} or V_{NO} = 2.1 V, I_{COM} = –32 mA,	Switch ON, See Figure 13	25°C	3 V		0.3	0.8	Ω
				Full				1	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le (V_{NC}$ or $V_{NO}) \le V_+$, I_{COM} = –32 mA,	Switch ON, See Figure 13	25°C	3 V		5	7	Ω
				Full				8	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = 3 V, or V_{NC} or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
		V_{NC} or V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0, or V_{NC} or V_{NO} = 3.6 V to 0, V_{COM} = 0 to 3.6 V,	Switch OFF, See Figure 14	25°C	0 V	–2	0.05	2	
				Full		–10		10	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NC} or V_{NO} = 3 V, or V_{COM} = 3 V, V_{NC} or V_{NO} = 3 V,	Switch OFF, See Figure 14	25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
		V_{COM} = 0 to 3.6 V, V_{NC} or V_{NO} = 3.6 V to 0, or V_{COM} = 3.6 V to 0, V_{NC} or V_{NO} = 0 to 3.6 V,	Switch OFF, See Figure 14	25°C	0 V	–2	0.05	2	
				Full		–10		10	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = Open, or V_{NC} or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NC} or V_{NO} = Open, or V_{COM} = 3 V, V_{NC} or V_{NO} = Open,	Switch ON, See Figure 15	25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
Digital Control Inputs (IN, $\overline{EN}$)[(2)]									
Input logic high	V_{IH}			Full		2		V_+	V
Input logic low	V_{IL}			Full		0		0.8	V
Input leakage current	I_{IH}, I_{IL}	$V_I = V_+$ or 0		25°C	3.6 V	–1	0.05	1	µA
				Full		–1		1	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 3.3-V Supply (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 2 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	3.3 V	2.5	3.5	8	ns
				Full	3 V to 3.6 V	2.5		9	
Turn-off time	t_{OFF}	V_{COM} = 2 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	3.3 V	0.5	2	6.5	ns
				Full	3 V to 3.6 V	0.5		7	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 22	25°C	3.3 V		2		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		4.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_+ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		9		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 16	25°C	3.3 V		16		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	3.3 V		16		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	3.3 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	3.3 V		300		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	3.3 V		–48		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25°C	3.3 V		–48		dB
Crosstalk adjacent	$X_{TALK(ADJ)}$	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 21	25°C	3.3 V		–81		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 23	25°C	3.3 V		0.21		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	3.6 V		2.5	7	µA
				Full				10	

Electrical Characteristics for 2.5-V Supply[1]

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NC}, V_{NO}					0		V_+	V
ON-state resistance	r_{on}	$0 \le (V_{NC}$ or $V_{NO}) \le V_+$, I_{COM} = –24 mA,	Switch ON, See Figure 13	25°C	2.3 V		12	20	Ω
				Full				22	
ON-state resistance match between channels	Δr_{on}	V_{NC} or V_{NO} = 1.6 V, I_{COM} = –24 mA,	Switch ON, See Figure 13	25°C	2.3 V		0.3	1	Ω
				Full				2	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le (V_{NC}$ or $V_{NO}) \le V_+$, I_{COM} = –24 mA,	Switch ON, See Figure 13	25°C	2.3 V		14	18	Ω
				Full				20	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0.5 V, V_{COM} = 2.2 V, or V_{NC} or V_{NO} = 2.2 V, V_{COM} = 0.5 V,	Switch OFF, See Figure 14	25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
		V_{NC} or V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0, or V_{NC} or V_{NO} = 3.6 V to 0, V_{COM} = 0 to 3.6 V,	Switch OFF, See Figure 14	25°C	0 V	–2	0.05	2	
				Full		–10		10	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 0.5 V, V_{NC} or V_{NO} = 2.2 V, or V_{COM} = 2.2 V, V_{NC} or V_{NO} = 0.5 V,	Switch OFF, See Figure 14	25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
		V_{COM} = 0 to 3.6 V, V_{NC} or V_{NO} = 3.6 V to 0, or V_{COM} = 3.6 V to 0, V_{NC} or V_{NO} = 0 to 3.6 V,	Switch OFF, See Figure 14	25°C	0 V	–2	0.05	2	
				Full		–10		10	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0.5 V, V_{COM} = Open, or V_{NC} or V_{NO} = 2.2 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 0.5 V, V_{NC} or V_{NO} = Open, or V_{COM} = 2.2 V, V_{NC} or V_{NO} = Open,	Switch ON, See Figure 15	25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
Digital Control Inputs (IN, $\overline{EN}$)[2]									
Input logic high	V_{IH}			Full		1.7		V_+	V
Input logic low	V_{IL}			Full		0		0.7	V
Input leakage current	I_{IH}, I_{IL}	$V_I = V_+$ or 0		25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–1		1	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 2.5-V Supply (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 1.5 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	2.5 V	2.5	5	9.5	ns
				Full	2.3 V to 2.7 V	2.5		10.5	
Turn-off time	t_{OFF}	V_{COM} = 1.5 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	2.5 V	0.5	3	7.5	ns
				Full	2.3 V to 2.7 V	0.5		9	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 22	25°C	2.5 V		1		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		3		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_+ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		9		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 16	25°C	2.5 V		16		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	2.5 V		16		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	2.5 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	2.5 V		300		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	2.5 V		–48		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25°C	2.5 V		–48		dB
Crosstalk adjacent	$X_{TALK(ADJ)}$	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 21	25°C	3.3 V		–81		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 23	25°C	2.5 V		0.33		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	2.7 V		2.5	7	µA
				Full				10	

TYPICAL PERFORMANCE

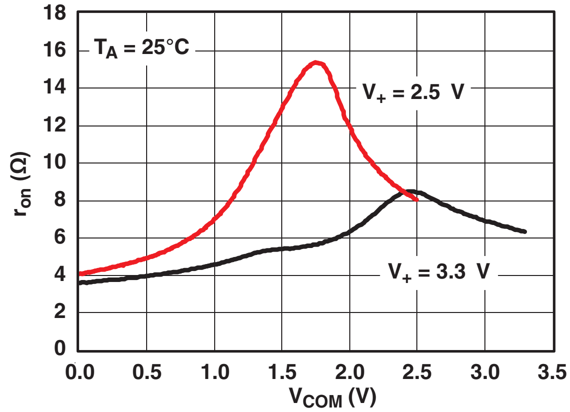


Figure 1. r_{on} vs V_{COM}

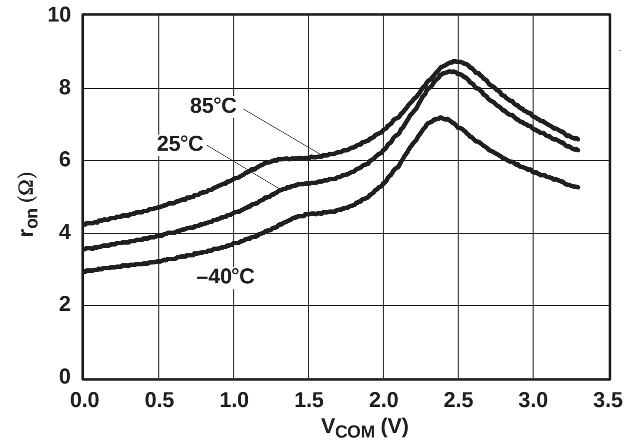


Figure 2. r_{on} vs V_{COM} (V_+ = 2.5 V)

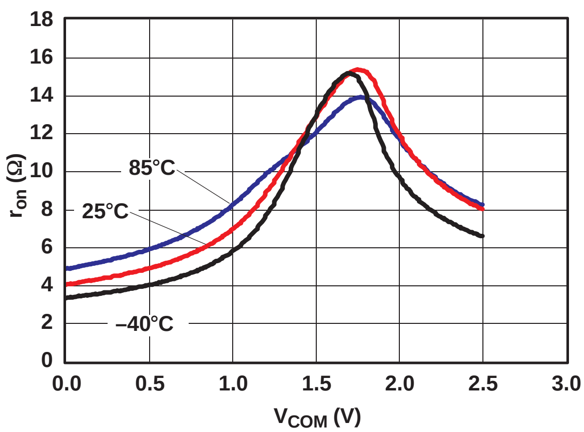


Figure 3. r_{on} vs V_{COM} (V_+ = 2.5 V)

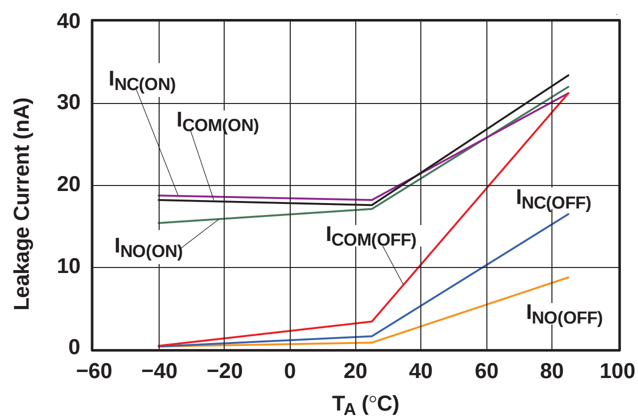


Figure 4. Leakage Current vs Temperature (V_+ = 3.6 V)

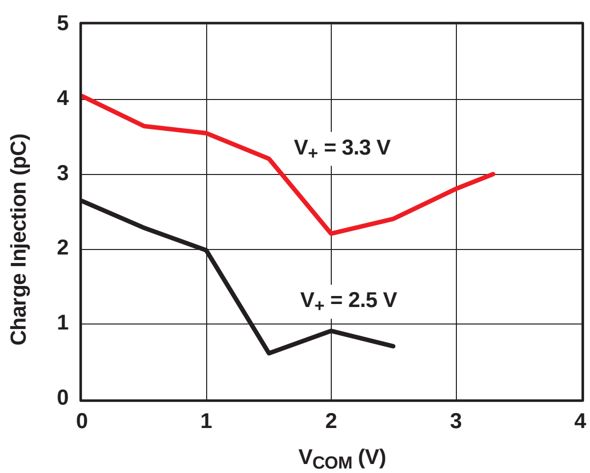


Figure 5. Charge Injection (Q_C) vs V_{COM}

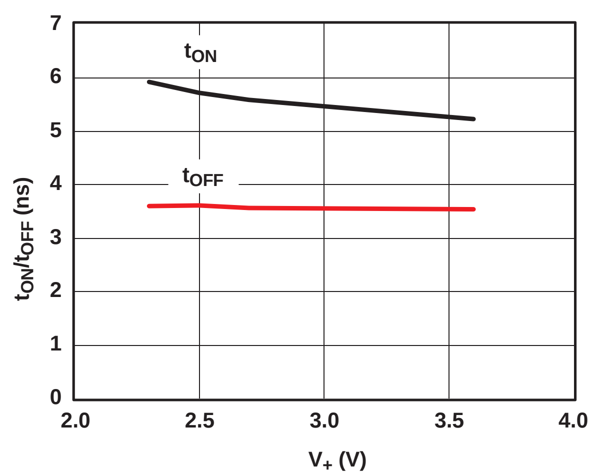


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

TYPICAL PERFORMANCE (continued)

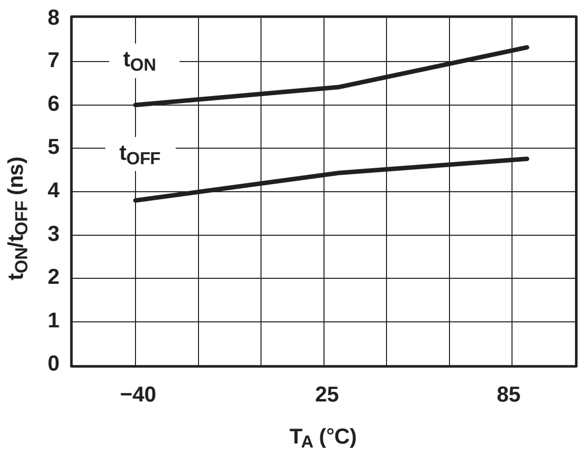


Figure 7. t_{ON} and t_{OFF} vs Temperature (V_+ = 3.3 V)

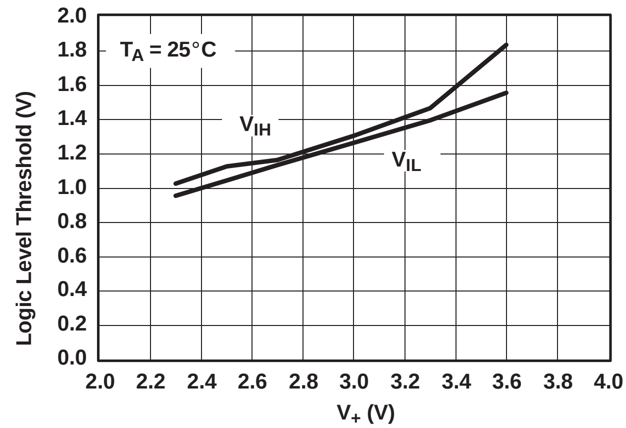


Figure 8. Logic-Level Threshold vs V_+

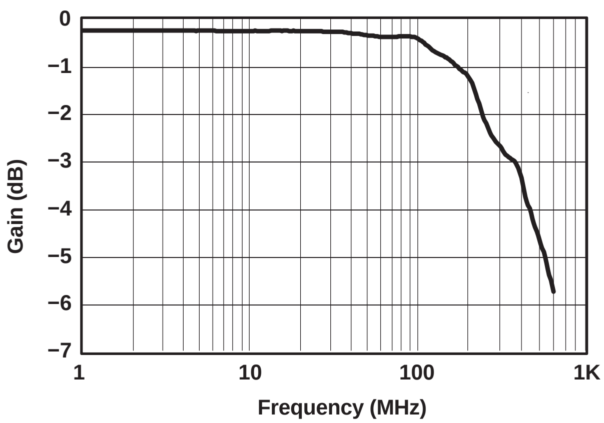


Figure 9. Gain vs Frequency Bandwidth (V_+ = 3.3 V)

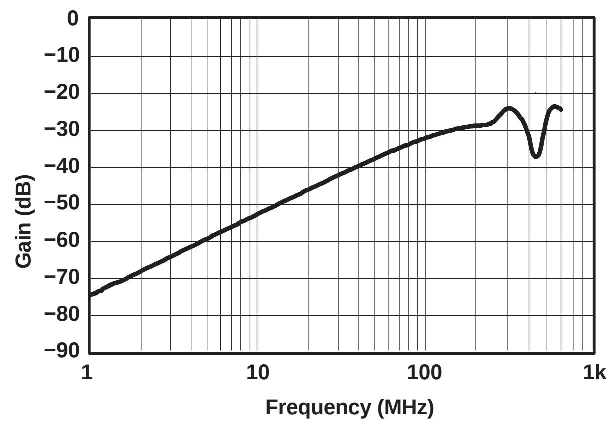


Figure 10. OFF Isolation and Crosstalk vs Frequency (V_+ = 3.3 V)

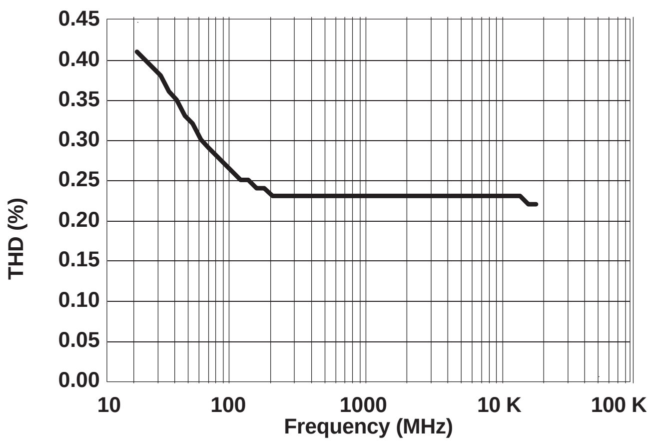


Figure 11. Total Harmonic Distortion vs Frequency

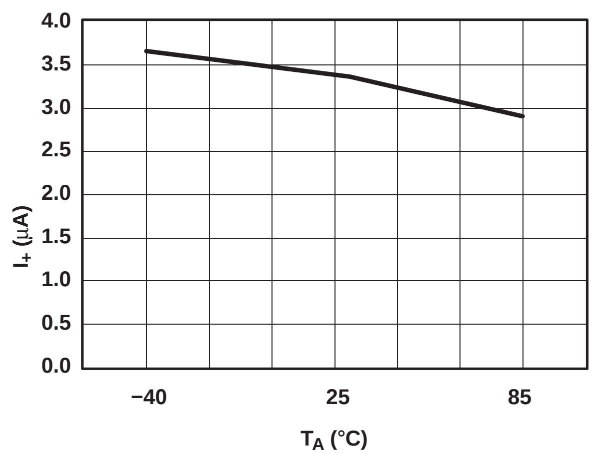


Figure 12. Power-Supply Current vs Temperature (V_+ = 3.3 V)

PIN DESCRIPTION

PIN NO.	NAME	DESCRIPTION
1	IN	Digital control pin to select between NC and NO
2	NC1	Normally closed
3	NO1	Normally open
4	COM1	Common
5	NC2	Normally closed
6	NO2	Normally open
7	COM2	Common
8	GND	Digital ground
9	COM3	Common
10	NO3	Normally open
11	NC3	Normally closed
12	COM4	Common
13	NO4	Normally open
14	NC4	Normally closed
15	$\overline{EN}$	Chip enable (active low)
16	V_+	Power supply

PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or NO ports when the channel is ON
Δr_{on}	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC or NO) in the OFF state
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC or NO) in the ON state and the output (NC or NO) open
V_{IH}	Minimum input voltage for logic high for the control input (IN, $\overline{EN}$)
V_{IL}	Maximum input voltage for logic low for the control input (IN, $\overline{EN}$)
V_I	Voltage at the control input (IN, $\overline{EN}$)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN, $\overline{EN}$)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output NC or NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (NC or NO) signal when the switch is turning OFF.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC or NO) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(OFF)}$	Capacitance at the NC port when the corresponding channel (NO to COM) is OFF
$C_{NO(ON)}$	Capacitance at the NC port when the corresponding channel (NO to COM) is ON
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is OFF
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is ON
C_I	Capacitance of control input (IN, $\overline{EN}$)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC1 to NO1). Adjacent crosstalk is a measure of unwanted signal coupling from an ON channel to an adjacent ON channel (NC1 to NC2) .This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

PARAMETER MEASUREMENT INFORMATION

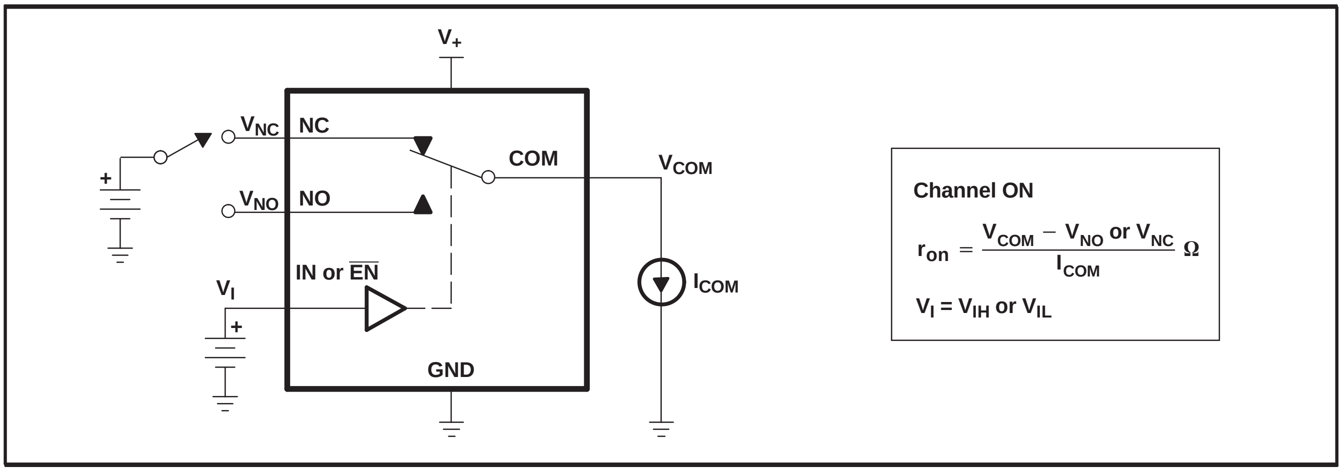


Figure 13. ON-State Resistance (r_{on})

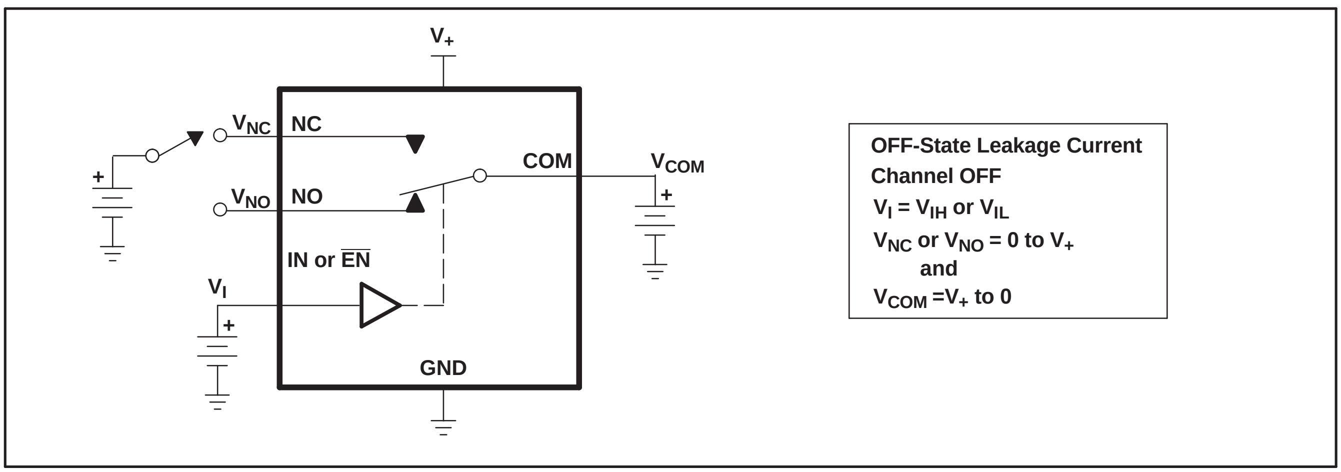


Figure 14. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$, $I_{NO(OFF)}$)

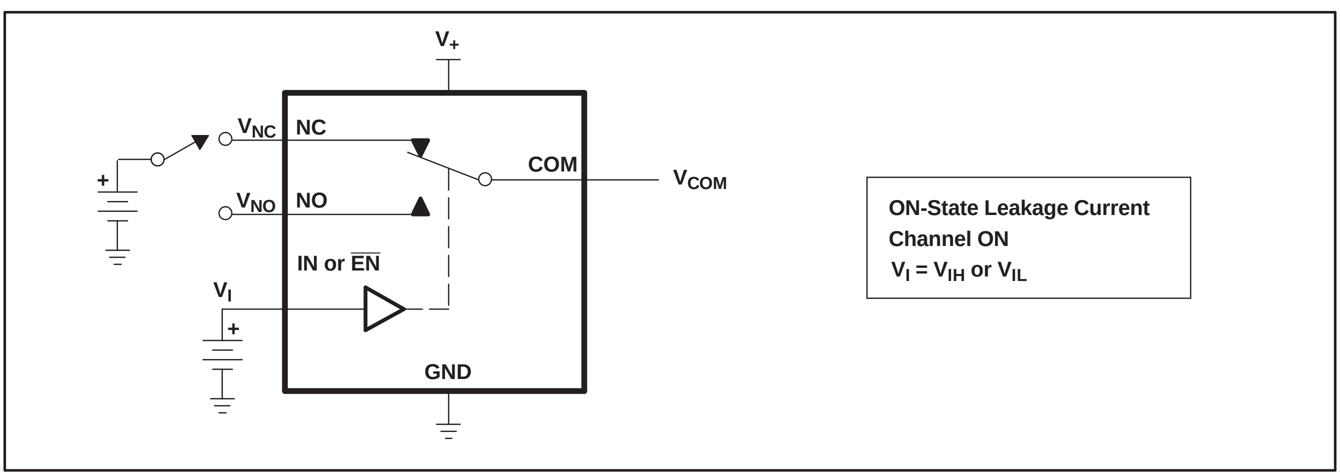


Figure 15. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

PARAMETER MEASUREMENT INFORMATION (continued)

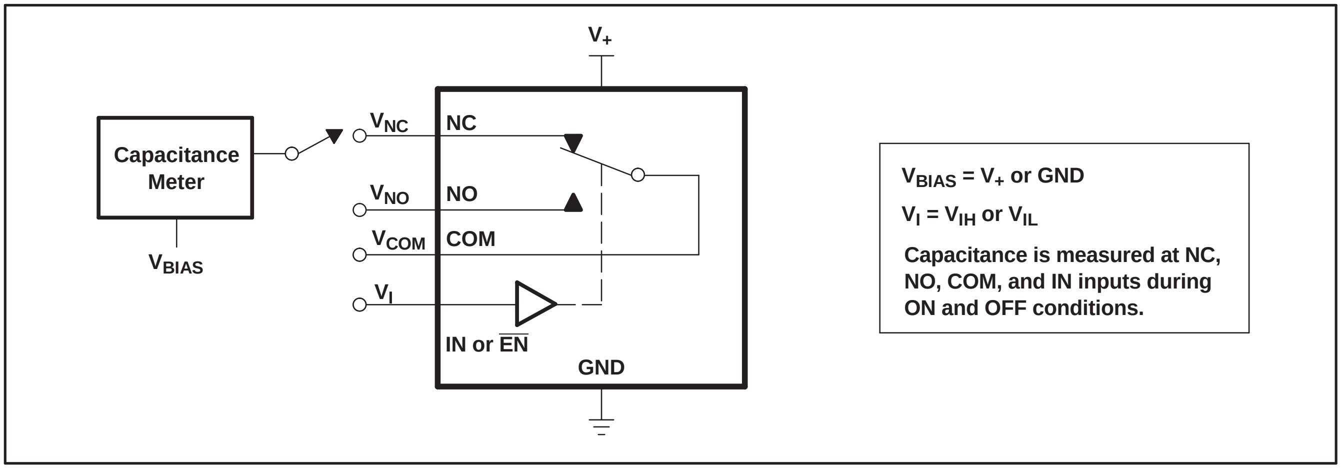
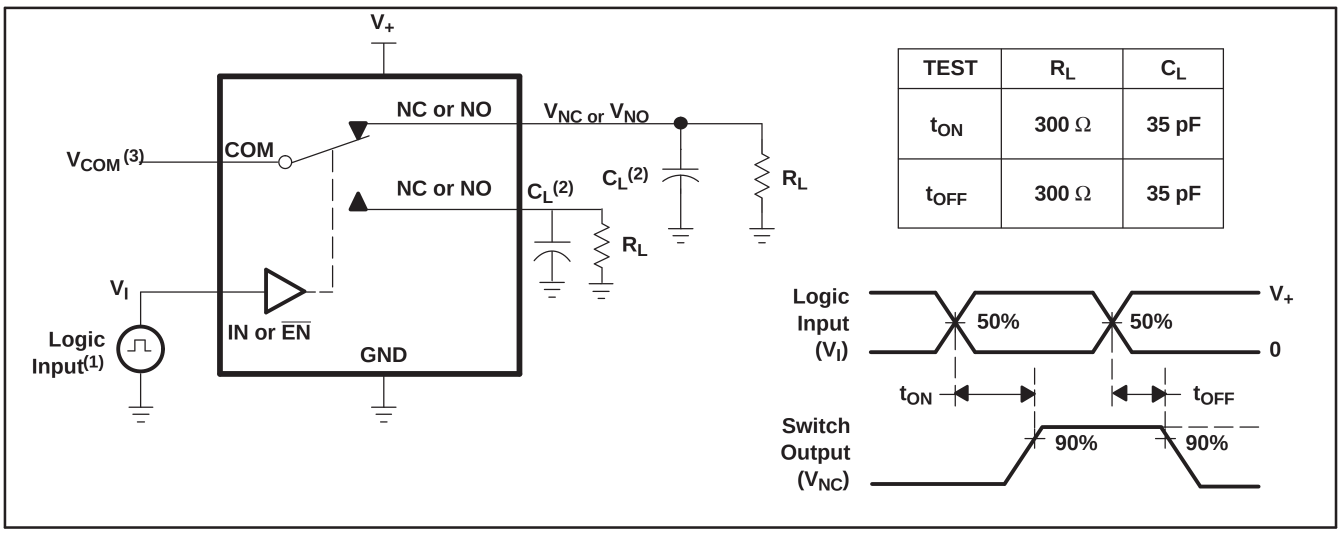


Figure 16. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)



TEST	R_L	C_L
t_{ON}	300 Ω	35 pF
t_{OFF}	300 Ω	35 pF

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

C. See Electrical Characteristics for V_{COM}.

Figure 17. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

PARAMETER MEASUREMENT INFORMATION (continued)

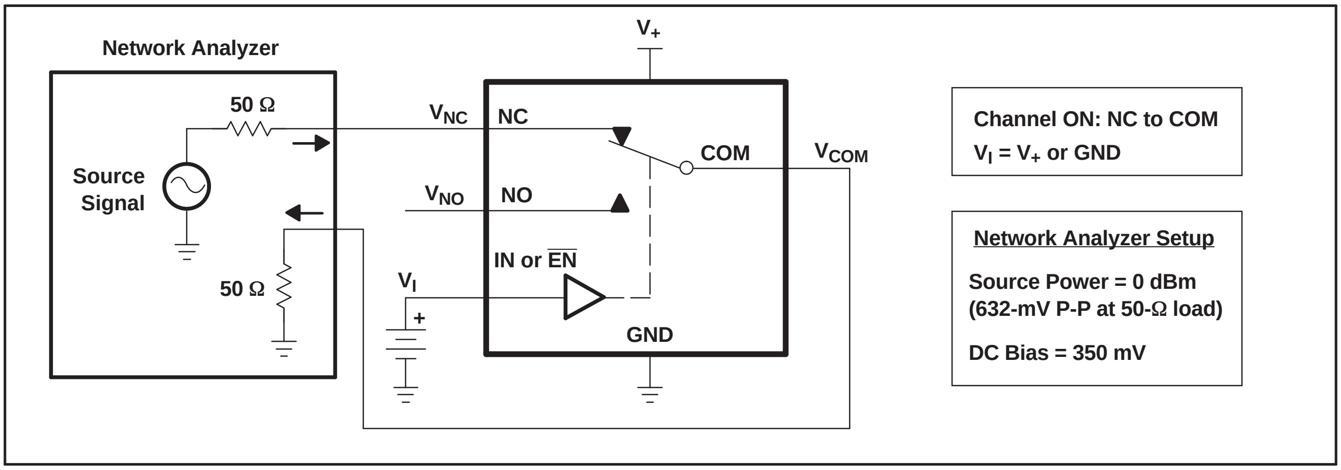


Figure 18. Bandwidth (BW)

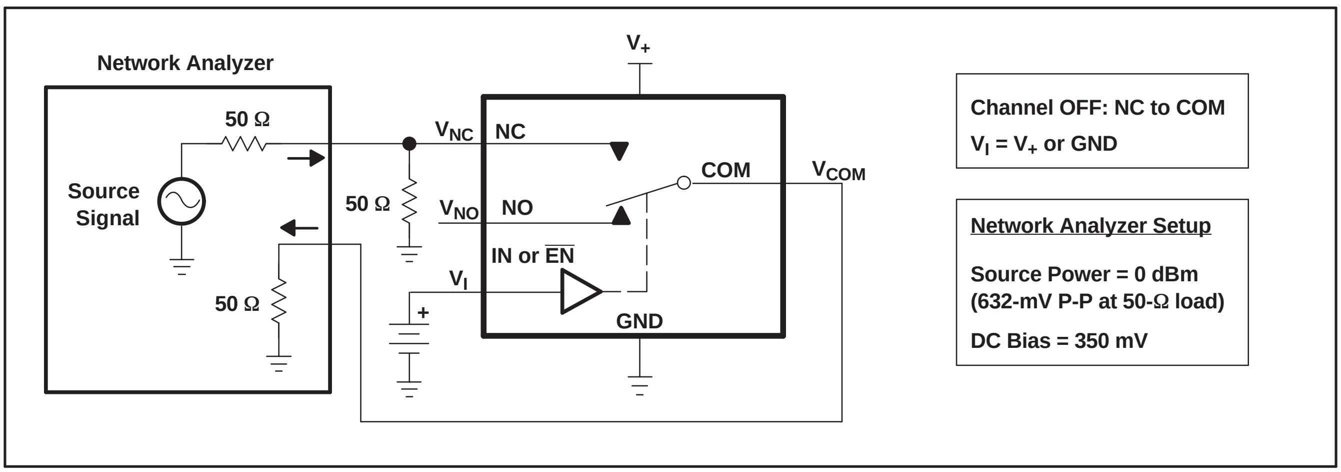


Figure 19. OFF Isolation (O_{ISO})

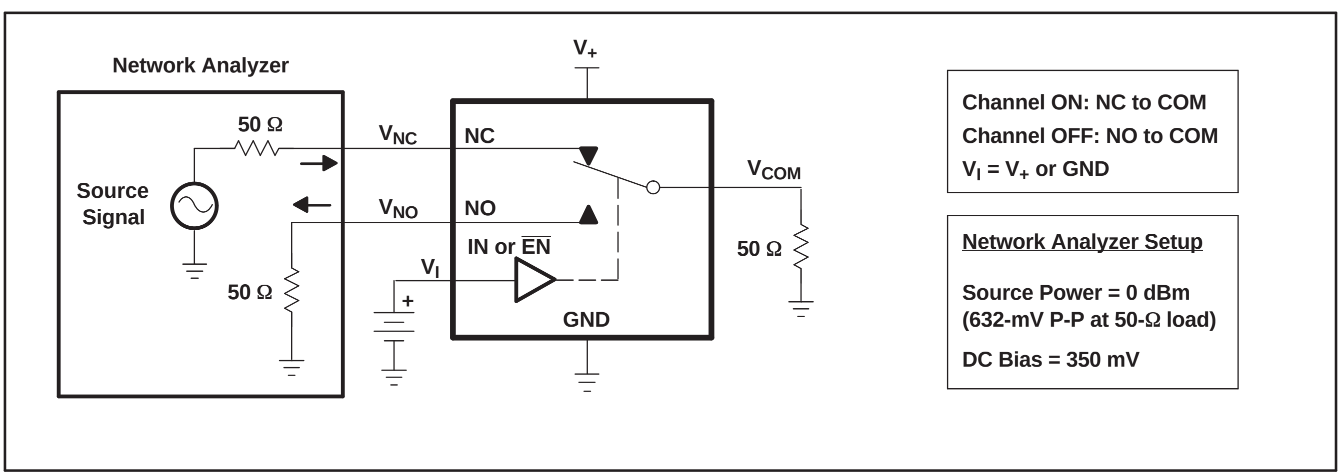


Figure 20. Crosstalk (X_{TALK})

PARAMETER MEASUREMENT INFORMATION (continued)

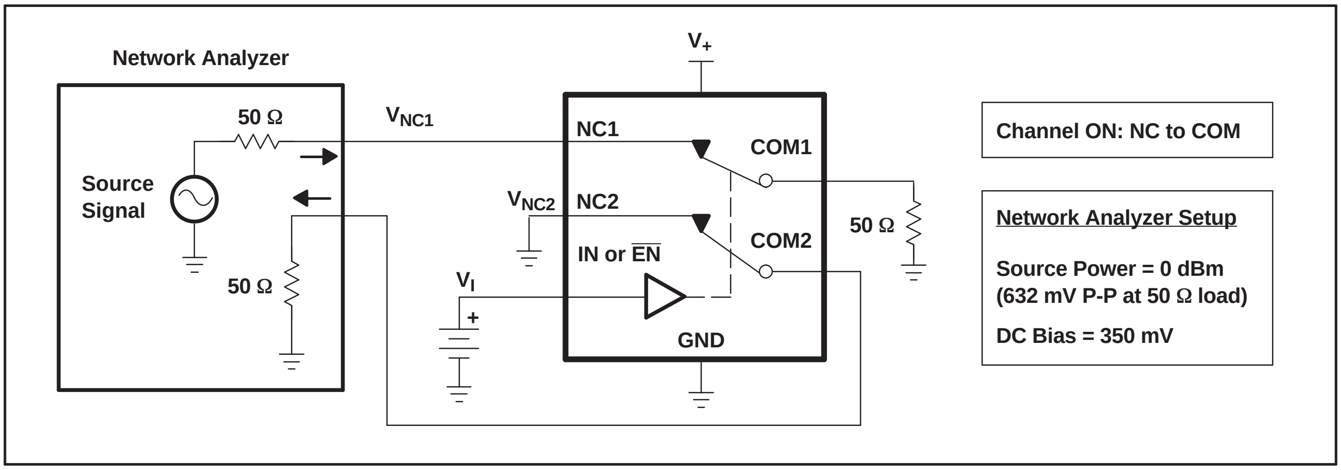
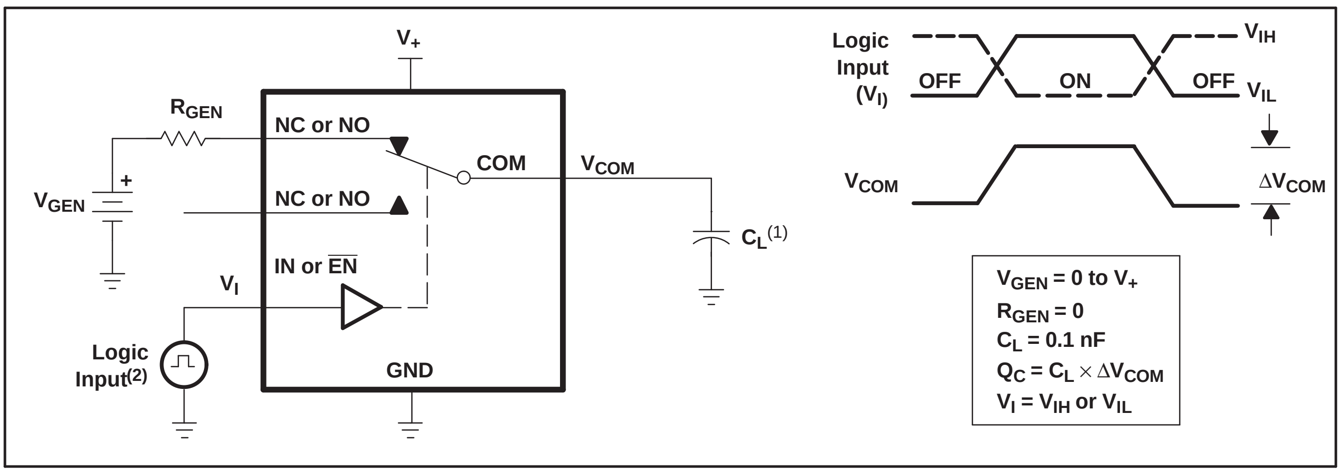


Figure 21. Crosstalk Adjacent

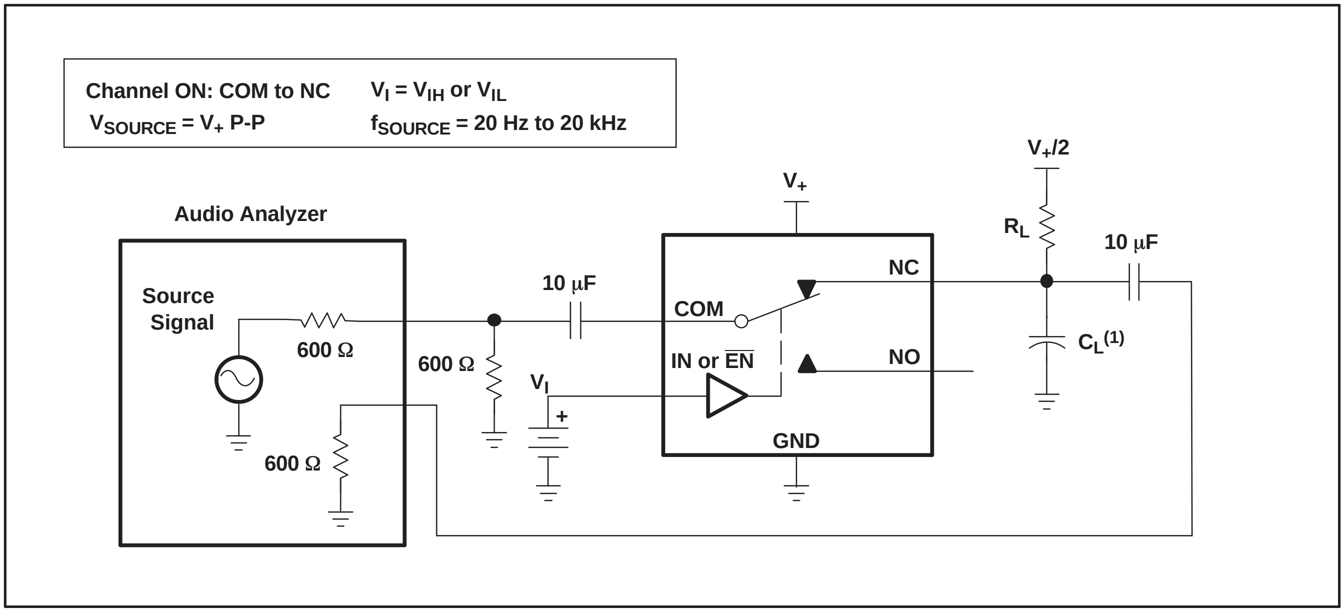


A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

Figure 22. Charge Injection (Q_C)

PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L includes probe and jig capacitance.

Figure 23. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TS3A5018D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5018DBQR	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TS3A5018DBQRE4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TS3A5018DBQRG4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TS3A5018DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5018DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5018DGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5018DGVRE4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5018DGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5018DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5018DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5018DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5018PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5018PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5018PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5018PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5018PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5018PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5018RGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TS3A5018RGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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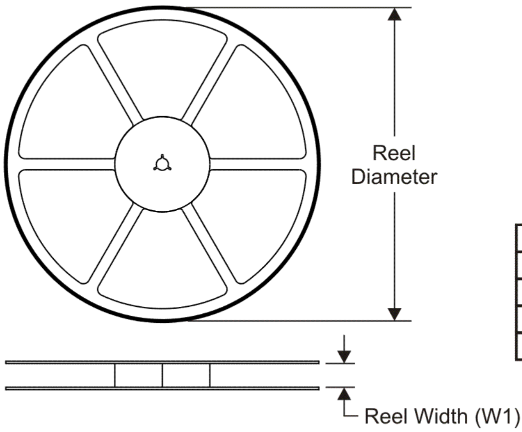
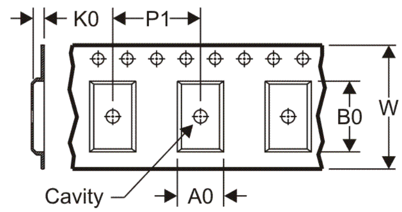
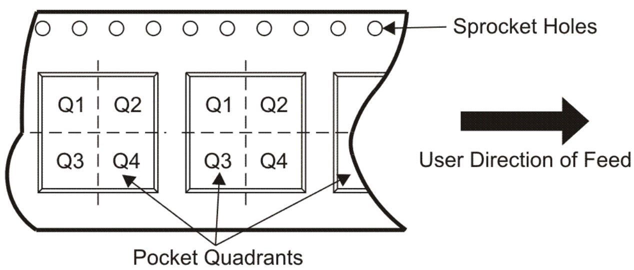
TAPE AND REEL INFORMATION





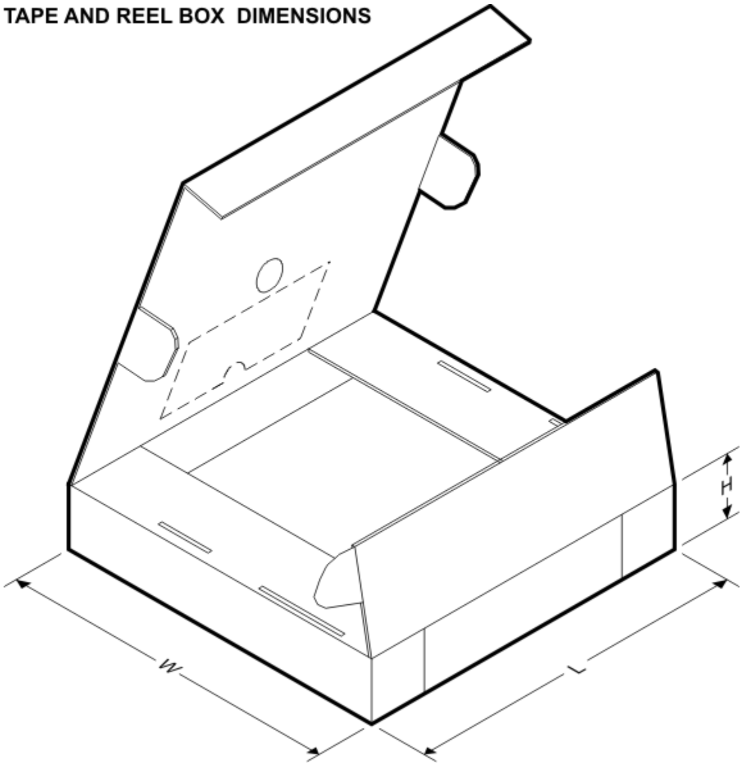
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A5018DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
TS3A5018DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TS3A5018PWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
TS3A5018RGYR	VQFN	RGY	16	3000	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

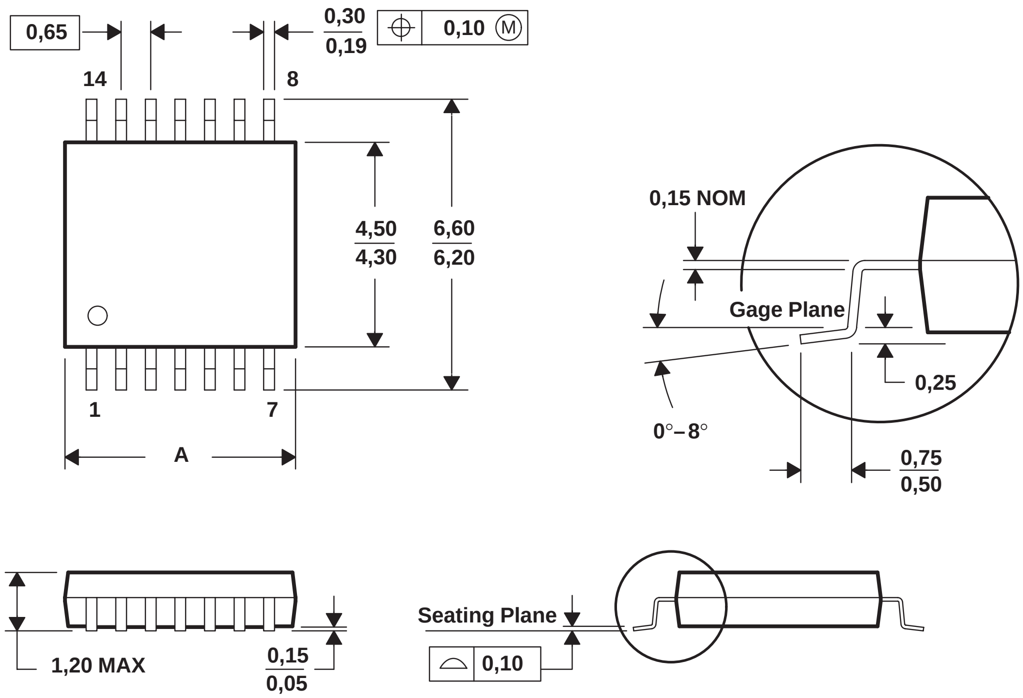


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A5018DGVR	TVSOP	DGV	16	2000	346.0	346.0	29.0
TS3A5018DR	SOIC	D	16	2500	333.2	345.9	28.6
TS3A5018PWR	TSSOP	PW	16	2000	346.0	346.0	29.0
TS3A5018RGYR	VQFN	RGY	16	3000	190.5	212.7	31.8

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

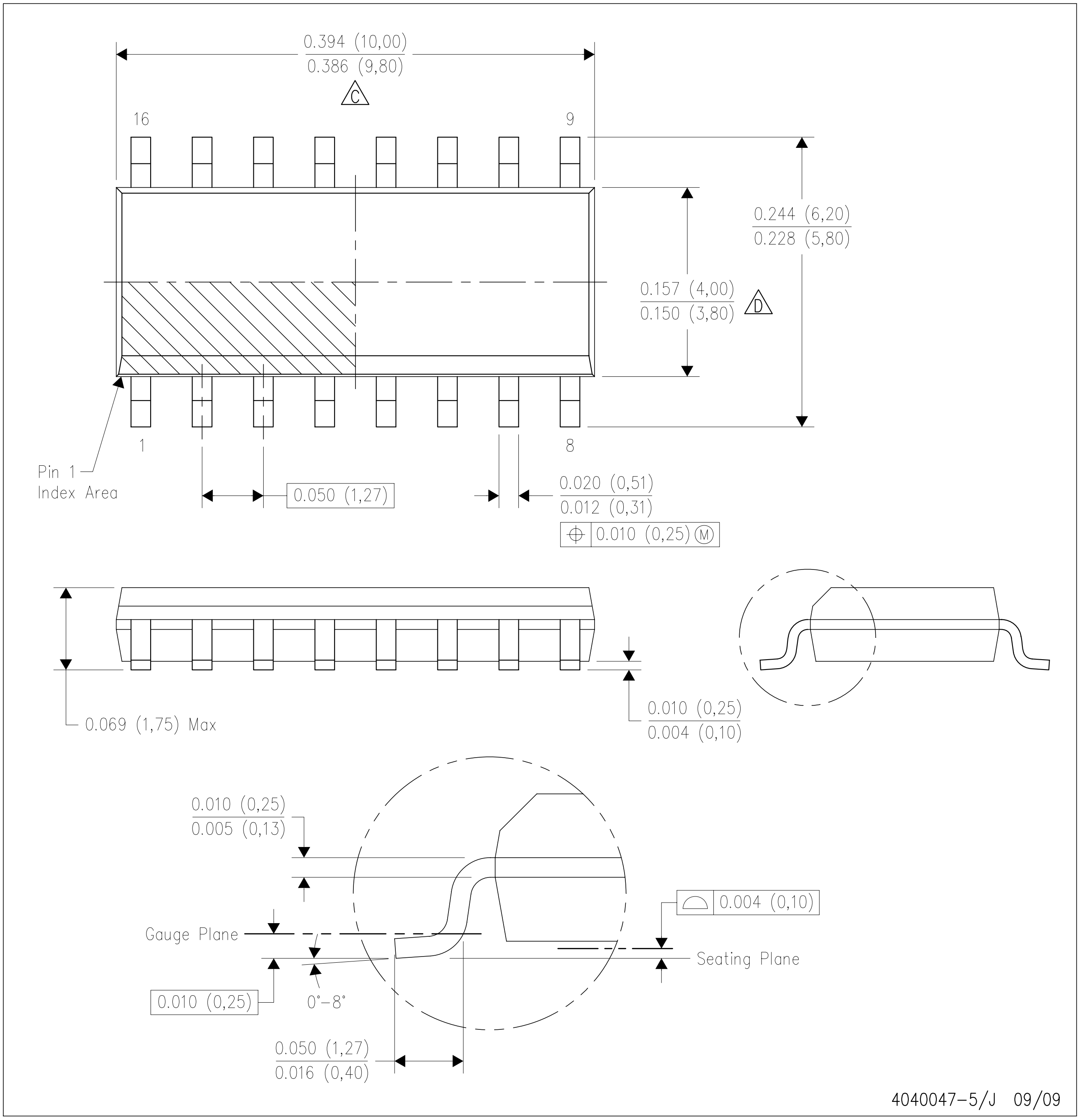


PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

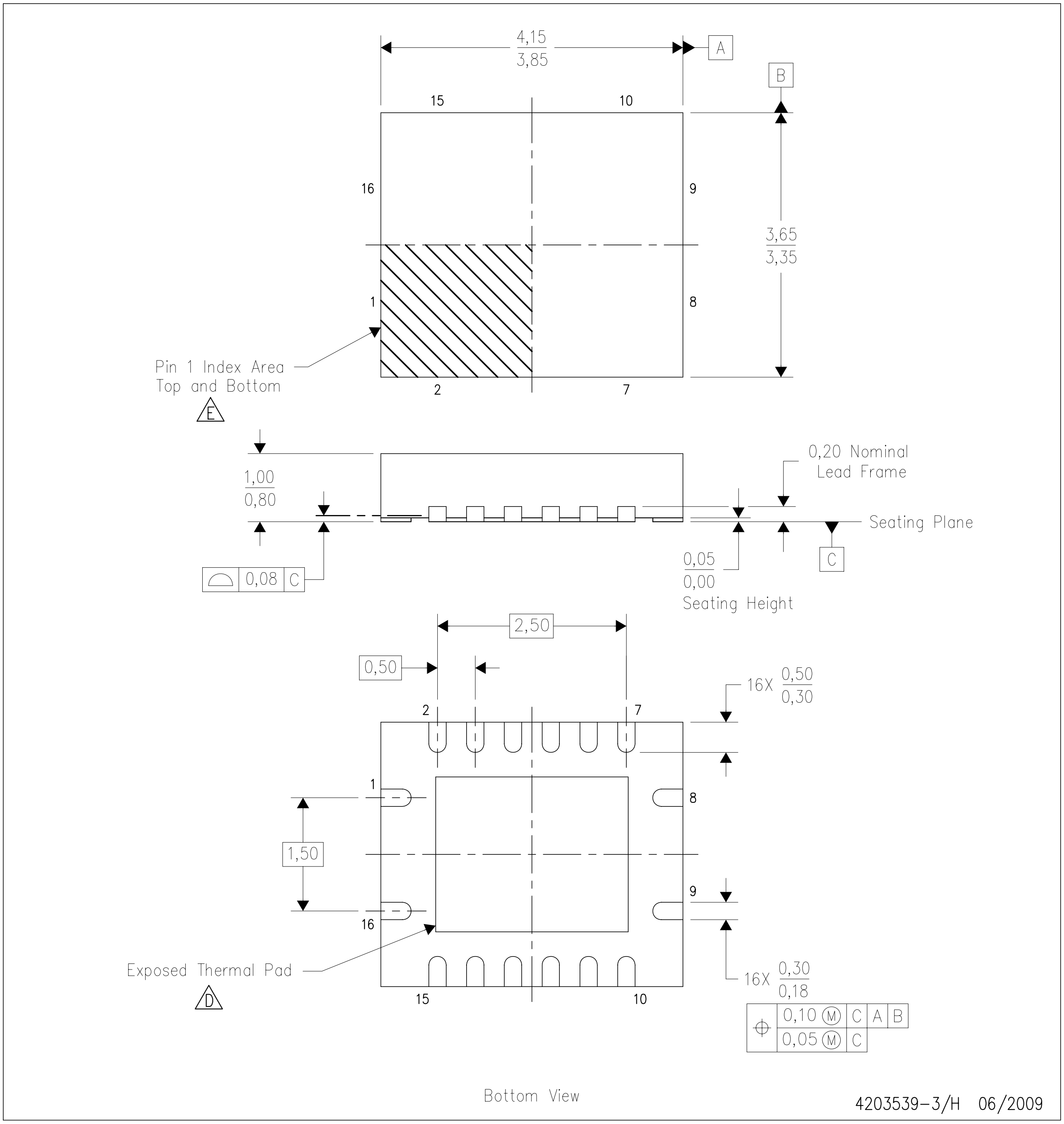
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



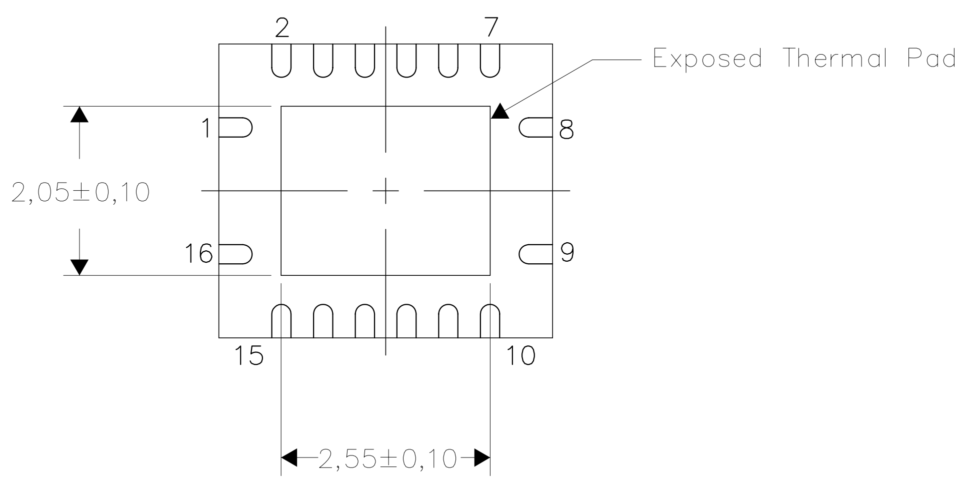
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
F. Package complies to JEDEC MO–241 variation BB.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

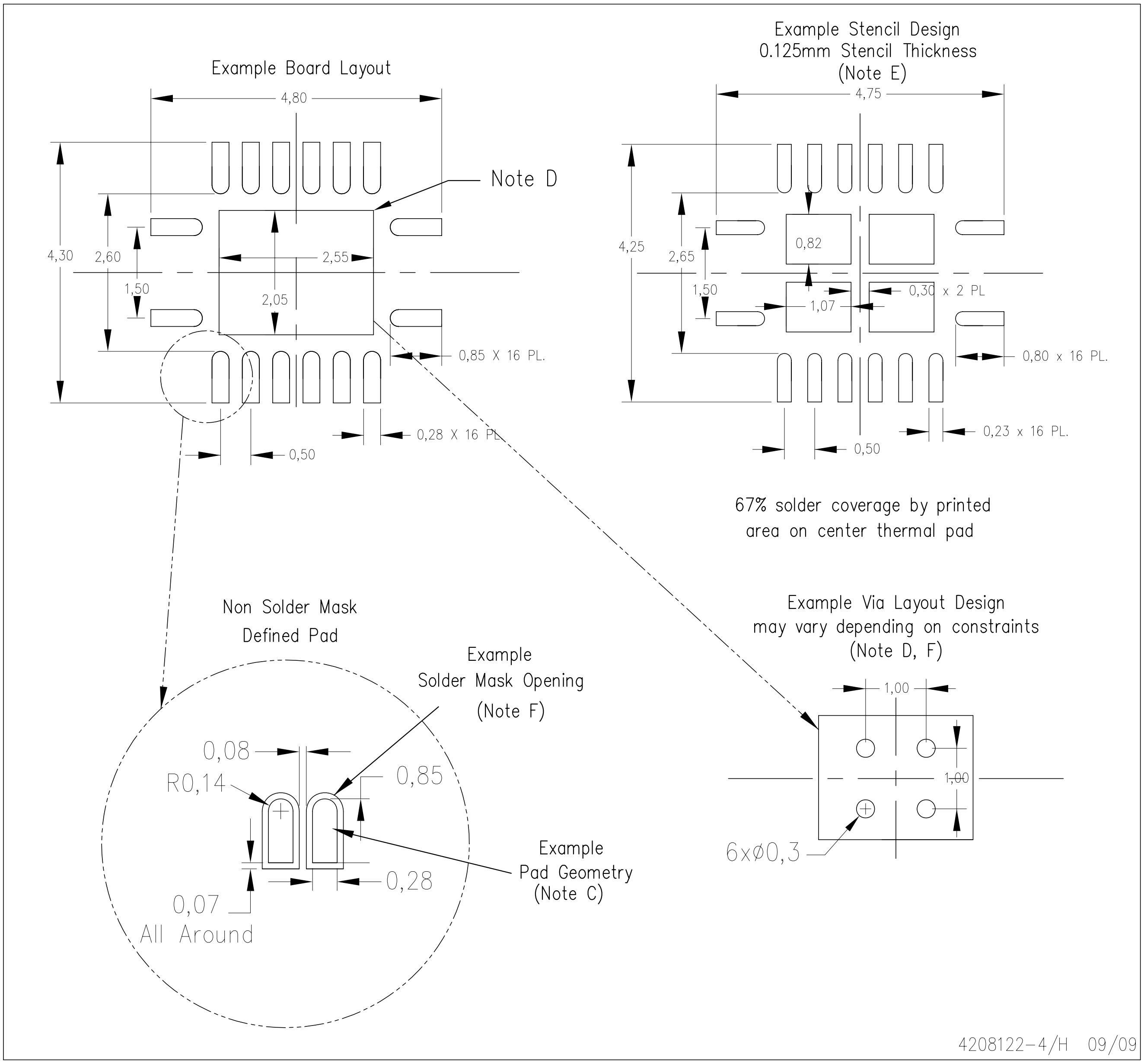


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGY (R–PVQFN–N16)



NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

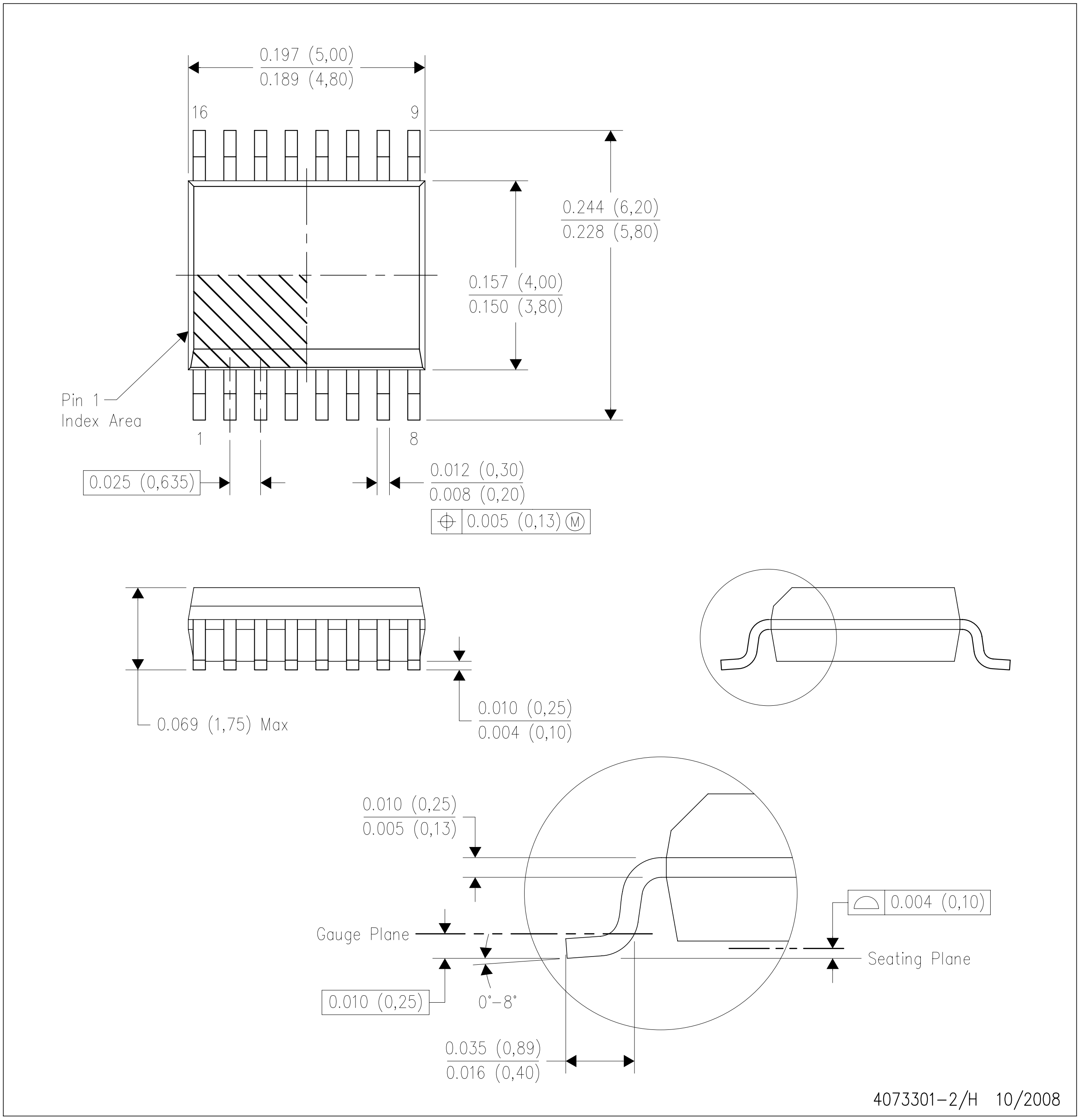
C. Publication IPC–7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

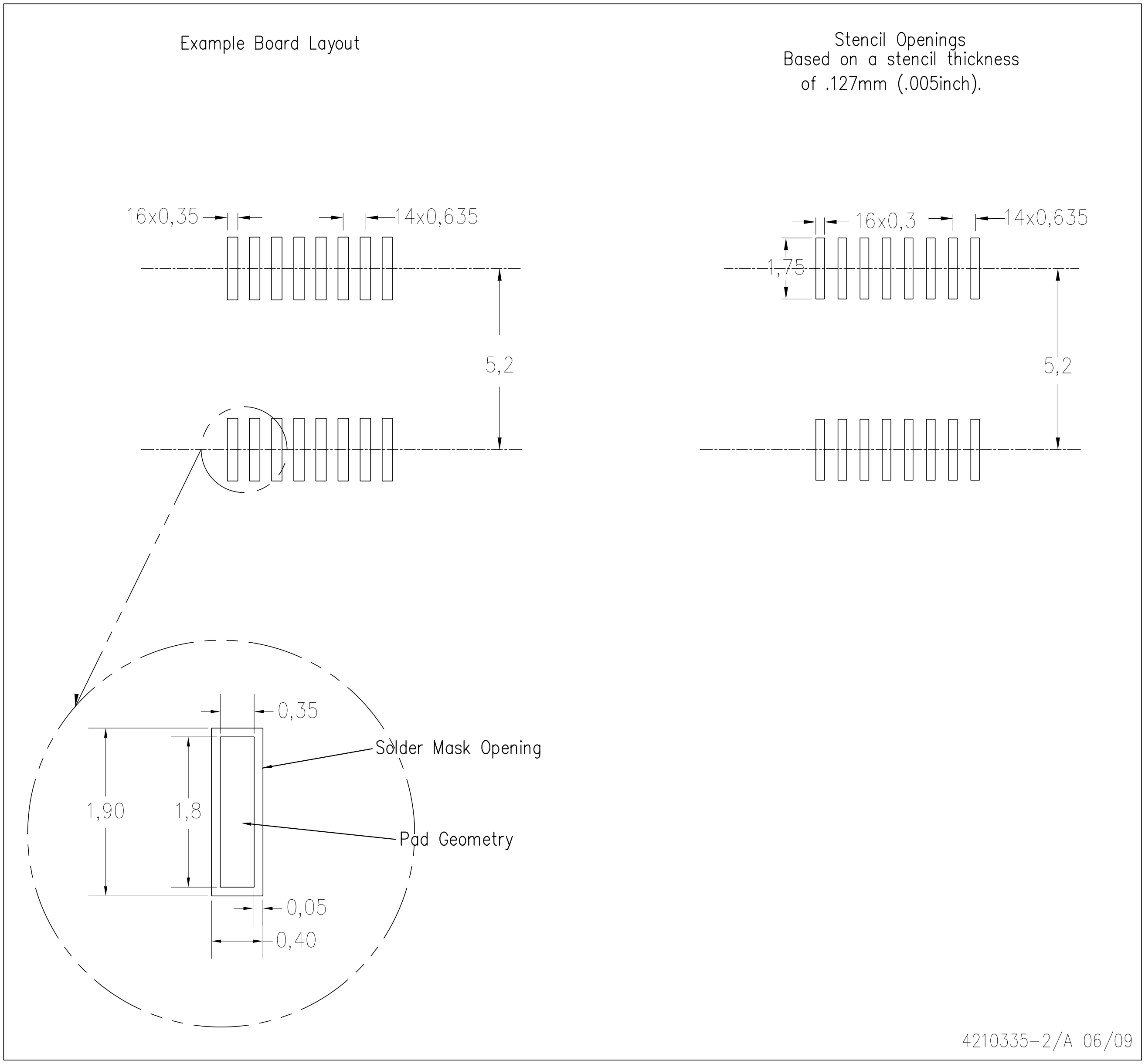
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

DBQ (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AB.

DBQ (R–PDSO–G16)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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