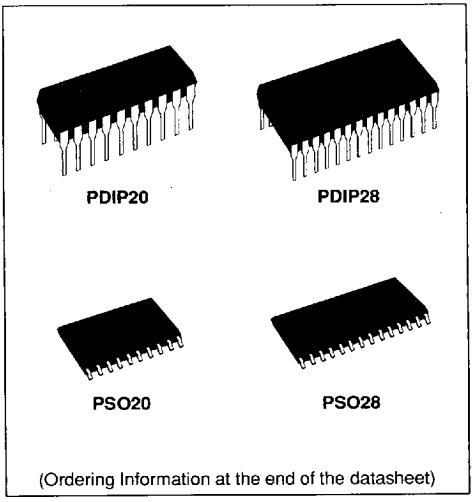
SGS-THOMSON MICROELECTRONICS

ST62E60B, T60B
ST62E65B, T65B

8-BIT OTP/EPROM HCMOS MCUs WITH A/D CONVERTER, EEPROM & AUTORELOAD TIMER

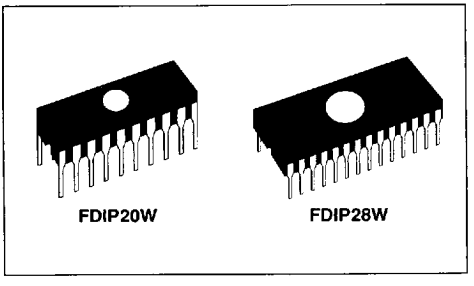
PRELIMINARY DATA

- 3.5 to 6.0V Supply Operating Range
- 8 MHz Maximum Clock Frequency
- -40 to +85°C Operating Temperature Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in ROM
- User EPROM: 3884 bytes
  Data ROM: User selectable size (in program EPROM)
  Data RAM: 128 bytes
  EEPROM: 128 bytes
- PDIP20, PSO20 (ST62T60B) packages
- PDIP28, PSO28 (ST62T65B) packages
- FDIP20W (ST62E60B) packages
- FDIP28W (ST62E65B) packages
- 13/21 fully software programmable I/O as:
  – Input with pull-up resistor
  – Input without Pull-up resistor
  – Input with interrupt generation
  – Open-drain or push-pull outputs
  – Analog Inputs
- 6/8 I/O lines can sink up to 20mA for direct LED or TRIAC driving
- 8 bit counter with a 7-bit programmable prescaler (Timer1)
- 8 bit Autoreload timer with 7-bit programmable prescaler (AR Timer)
- Digital Watchdog
- 8 bit A/D Converter with up to 7 (ST62E60B,T60B) and up to 13 (ST62E65B,T65B) analog inputs
- 8 bit Synchronous Peripheral Interface (SPI)
- On-chip clock oscillator driven by Quartz or Ceramic or RC network
- User configurable Power-on Reset
- One external not maskable interrupt
- 9 powerful addressing modes



(Ordering Information at the end of the datasheet)

EPROM PACKAGES



The ST62E60B and ST62E65B are the EPROM versions; ST62T60B and ST62T65B are the OTP versions; both are fully compatible with ST6260B and ST6265B ROM resonator versions.

Figure 1. ST62E60B/T60B Pin Configuration

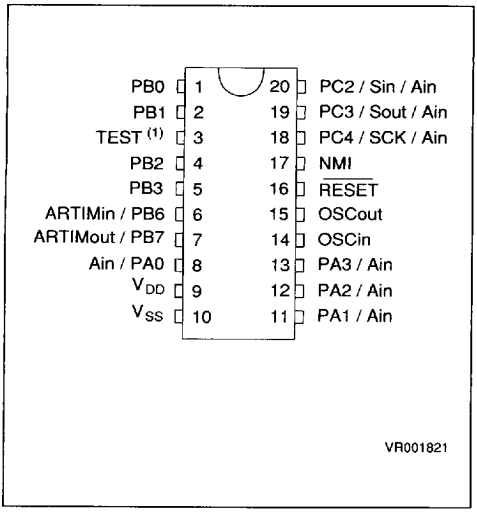
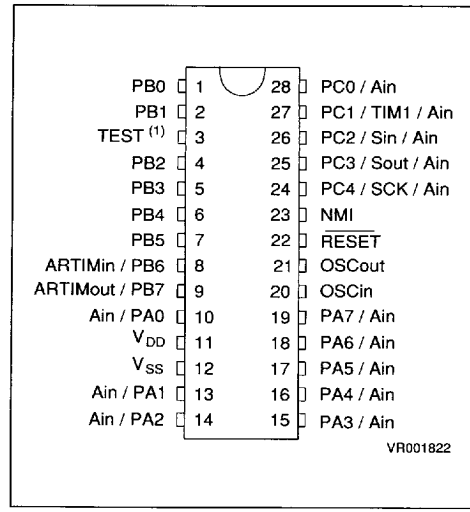
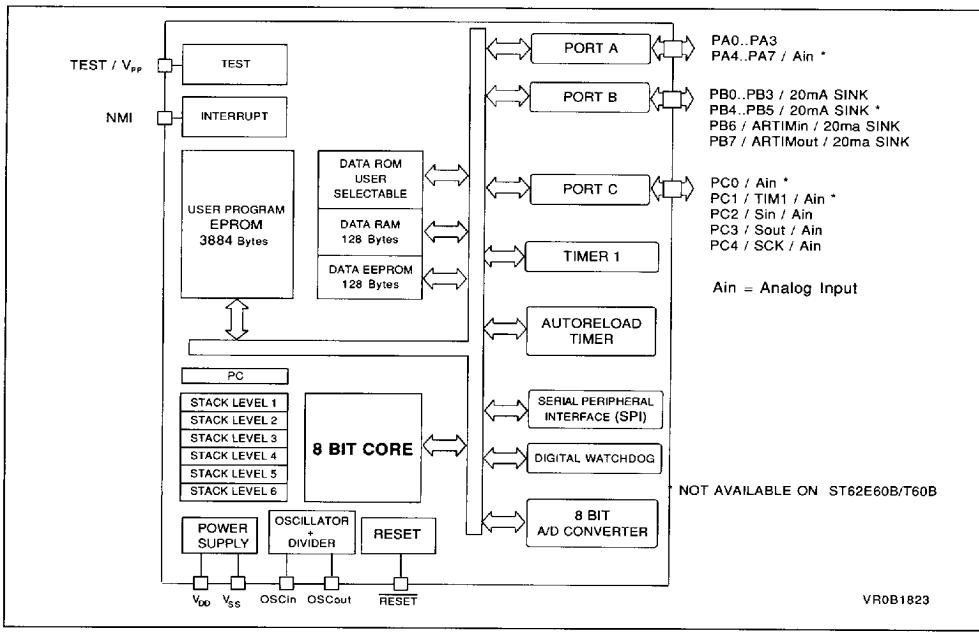


Figure 2. ST62E65B/T65B Pin Configuration



Note 1. This pin is also the V_{PP} input for EPROM based devices

Figure 3. ST62E60B,E65B Block Diagram



GENERAL DESCRIPTION

The ST62E60B,T60B,E65B,T65B microcontrollers are members of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications.

They are the EPROM and OTP versions of the ST6260B and ST6265B devices. EPROM are suited for development. OTPs are suited for prototyping, preseries, low to mid volume series and inventory optimization for customer having several applications using the same MCU. All ST62xx members are based on a building block approach: a common core is surrounded by a combination of on-chip peripherals (macrocells).

The macrocells of the ST62E60B, T60B, E65B and T65B are: the timer peripheral that includes an 8-bit counter with a 7-bit software programmable prescaler (Timer1), the 8-bit Auto-reload Timer with 7 bit programmable prescaler (AR Timer), the 8-bit A/D Converter with up to 7 (ST62E60B,T60B) and up to 13 (ST62E65B,T65B) analog inputs (A/D inputs are alternate functions of I/O pins), the Digital Watchdog (DWD) and an 8-bit Serial synchronous Peripheral Interface (SPI). In addition, these devices offer 128 bytes of EEPROM for non volatile data storage.

The ST62E60B, T60B, E65B and T65B are upward compatible with the ST62E60, T60, E65, T65. They in addition feature RC network, user configurable Power-on Reset Delay and an External STOP Mode Control option to enlarge the range of power consumption/safety trade-offs.

ST62E60B ,T60B, E65B and T65B are well suited for automotive, appliance and industrial applications.

PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. Depending on the Option Byte, either a quartz crystal, a ceramic resonator, an external clock signal or an RC network can be connected in order to allow the correct operation of the MCU with various stability/cost trade-offs. The oscillator frequency is internally divided by 1, 2 or 4 by a software controlled divider.The OSCin pin is the input pin, the OSCout pin is the output pin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller to the beginning of its program.

TEST/V_{PP}. The TEST must be held at V_{SS} for normal operation. If TEST pin is connected to a +12.5V level during the reset phase, the EPROM programming Mode is entered.

NMI. The NMI pin provides the capability for asynchronous interrupt applying an external not maskable interrupt to the MCU. The NMI is falling edge sensitive. It is provided with an on-chip pull-up resistor and Schmitt trigger characteristics.

When the External STOP Mode Control option is enabled, the NMI pin in addition enables a control of the way the STOP instruction is processed.

PC1/TIM1/Ain. This pin can be used as a Port C I/O bit, as Timer 1 I/O pin or as analog input for the on-chip A/D converter. This pin is available only on the ST62E65B and T65B (28 pin version). If programmed to be the Timer 1 pin, in input mode it is connected to the prescaler and acts as external timer clock or as control gate for the internal timer clock. In the output mode the timer pin outputs the data bit when a time out occurs.
To use this pin as Timer 1 output a dedicated bit in the TIMER 1 Status/Control Register must be set. To use this pin as input pin the I/O pin has to be programmed as input. The analog mode should be programmed to use the line as an analog input.

PB6/ARTIMin, PB7/ARTIMout. These pins are either Port B I/O bits or the Input and Output pins of the Auto-reload Timer. To be used as timer input function PB6 has to be programmed as input with or without pull-up. A dedicated bit in the AR TIMER Mode Control Register sets PB7 as timer output function.

PA0-PA7. These 8 lines are organized as one I/O port (A). PA4-PA7 are not available on ST62E60B and T60B (20 pin version). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, analog input, open-drain or push-pull output.

PB0-PB3, PB4, PB5. These 6 lines are organized as one I/O port (B). PB4, PB5 are available only on the ST62E65B and T65B (28 pin version). When the External STOP Mode Control is disabled, each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output. In output mode these lines can also sink 20mA for direct LED and TRIAC driving. When the External STOP Mode Control is enabled, PB0 is forced as open drain output. The other lines are unchanged.

PC0-PC4. These 5 lines are organized as one I/O port (C). PC0 and PC1 are not available on ST62E60B, T60B (20 pin version). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, analog input for the A/D converter, open-drain or push-pull output. PC2-PC4 can also be used as respectively Data in, Data out and Clock I/O pins for the on-chip SPI to carry the synchronous serial I/O signals.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST6260B,65B ROM DEVICE FOR FURTHER DETAILS.

EPROM/OTP DESCRIPTION

The ST62E60B/E65B are the EPROM versions of the ST6260B/65B products. They are intended for use during the development of an application and for pre-production and small volume production. ST62T60B/T65B OTP have the same characteristics. They all include EPROM memory instead of the ROM memory of the corresponding ST6260B/65B, and so the program can be easily modified by the user with the ST62E6xB EPROM programming tools from SGS-THOMSON.

From a user point of view (with the following exceptions) the ST62E60B/E65B and ST62T60B/T65B products have exactly the same software and hardware features as the ROM version. An additional mode is used to configure the part for programming of the EPROM, this is set by a +12.5V voltage appiied to the TEST/V_{PP} pin. The programming of the ST62E60B, T60B, E65B, T65B is described in the User Manual of the EPROM Programming Board.

The supply operating range is 3.5V to 6.0Von the OTP and the EPROM parts.
On the ROM version, the supply operating range is 3.0V to 6.0V.

Other than this exception, the OTP, EPROM and ROM parts are fully compatible. This datasheet thus provides only information specific to the EPROM based devices.

Note also the Low STOP mode consumption of ROM devices can not be emulated on EPROM or OTP devices

ROM Option Emulation

The ROM mask options that can be selected by the user in the ROM devices can be selected on the EPROM/OTP devices by an EPROM CODE byte that can be programmed with the ST62E6xB EPROM programming tools available from SGS-THOMSON. This EPROM CODE byte is automatically read, and the selected options enabled, when the chip reset is activated.

The Option byte is written during programming either by using the PC menu (PC driven Mode) or automatically (stand-alone mode).

EPROM Programming Mode

An additional mode is used to configure the part for programming of the EPROM, this is set by a 12.5V voltage applied to the TEST/V_{PP} pin. The programming of the ST62E60B/E65B and ST62T60B/T65B is described in the User Manual of the EPROM Programming board.

EPROM ERASING

The EPROM of the windowed package of the ST62E60B/E65B may be erased by exposure to Ultra Violet light.

The erasure characteristic of the ST62E60B/E65B is such that erasure begins when the memory is exposed to light with a wave lengths shorter than approximately 4000Å. It should be noted that sunlights and some types of fluorescent lamps have wavelengths in the range 3000-4000Å. It is thus recommended that the window of the ST62E60B/E65B packages be covered by an opaque label to prevent unintentional erasure problems when testing the application in such an environment.

The recommended erasure procedure of the ST62E60B/E65B EPROM is the exposure to short wave ultraviolet light which have a wave-length 2537A. The integrated dose (i.e. U.V. intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000µW/cm^2 power rating. The ST62E60B/E65 should be placed within 2.5cm (1Inch) of the lamp tubes during erasure.

Table 1. ST62T60B/T65B OTP Memory Map

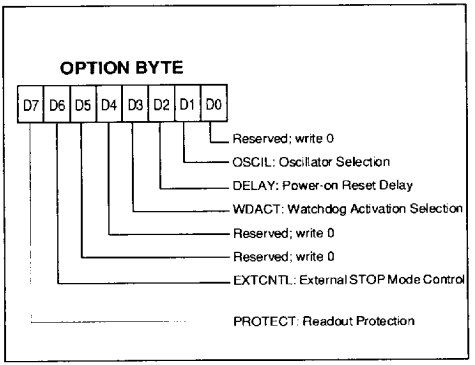
Device Address	Description
0000h-007Fh	Reserved
0080h-0F9Fh	User Program ROM 3856 Bytes
0FA0h-0FEFh	Reserved
0FF0h-0FF7h	Interrupt Vectors
0FF8h-0FFBh	Reserved
0FFCh-0FFDh	NMI Vector
0FFEh-0FFFh	User Reset Vector

Note. Reserved Areas should be filled with FFh

OPTION BYTE

The Option Byte enables emulation of the mask options of the ROM devices. It can only be accessed during the programming mode. This access is made either automatically (copy from a master device) or by selecting the "OPTION BYTE PROGRAMMING" mode of the programmer. The option byte is located in a non-user map. No address has to be specified.

Figure 4. EPROM Code Option Byte



PROTECT. This bit allows the protection of the software contents against piracy. When the bit PROTECT is set high, readout of the OTP contents is prevented by hardware. No programming equipment is able to gain access to the user program. When this bit is low, the user program can be read. This bit emulates the READOUT PROTECTION mask option of ROM devices.

EXTCNTL. This bit selects the External STOP Mode capability. When EXTCNTL is high, pin NMI controls if the STOP mode can be accessed when the watchdog is active. In addition, PB0 is forced as open drain output. When EXTCNTL is low, the STOP instruction is processed as a WAIT as soon as the watchdog is active. This bit emulates the EXTERNAL STOP MODE CONTROL of ROM devices.

D5-D4. Reserved. Must be cleared to zero.

WDACT. This bit controls the watchdog activation. When it is high, hardware activation is selected. The software activation is selected when WDACT is low.This bit emulates the WATCHDOG ACTIVATION mask option of ROM devices.

DELAY. This bit enables the selection of the delay internally generated after pin RESET is released. When DELAY is low, the delay is 2048 cycles of the oscillator, it is of 32768 cycles when DELAY is high. This bit emulates the POWER ON RESET DELAY mask option of ROM devices.

OSCIL. When this bit is low, the oscillator must be controlled by a quartz crystal, a ceramic resonator or an external frequency. When it is high, the oscillator must be controlled by an RC network, with only the resistor having to be externally provided. This bit emulates the OSCILLATOR mask option of ROM devices.

D0. Reserved. Must be cleared to zero.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages.

For proper operation it is recommended that V_I and V_O must be higher than V_{SS} and smaller V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Power Considerations. The average chip-junction temperature, Tj, in Celsius can be obtained from :

$Tj = T_A + PD \times RthJA$

Where : T_A = Ambient Temperature.

RthJA = Package thermal resistance (junction-to ambient).

PD = Pint + Pport.

Pint = $I_{DD} \times V_{DD}$ (chip internal power).

Pport = Port power dissipation (determinated by the user).

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7.0	V
V_I	Input Voltage	V_{SS} - 0.3 to V_{DD} + 0.3 (1)	V
V_O	Output Voltage	V_{SS} - 0.3 to V_{DD} + 0.3 (1)	V
I_O	Current Drain per Pin Excluding V_{DD}, V_{SS}	10	mA
I_{INJ+}	Pin Injection current (positive), All I/O, V_{DD} = 4.5V	+5	mA
I_{INJ-}	Pin Injection current (negative), All I/O, VDD = 4.5V	-5	mA
IV_{DD}	Total Current into V_{DD} (source)	50	mA
IV_{SS}	Total Current out of V_{SS} (sink)	50 (2)	mA
Tj	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-60 to 150	°C

Notes :

- Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device . This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

- (1) Within these limits, clamping diodes are guarantee to be not conductive. Voltages outside these limits are authorised as long as injection current is kept within the specification.

- (2) The total current through ports A and B combined may not exceed 50 mA. The total current through port C may not exceed 50 mA. If the application is designed with care and observing the limits stated above, total current may reach 100 mA.

THERMAL CHARACTERISTIC

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
RthJA	Thermal Resistance	PDIP28			55	°C/W
		PDIP20			60	
		PSO28			75	
		PSO20			80	

RECOMMENDED OPERATING CONDITIONS

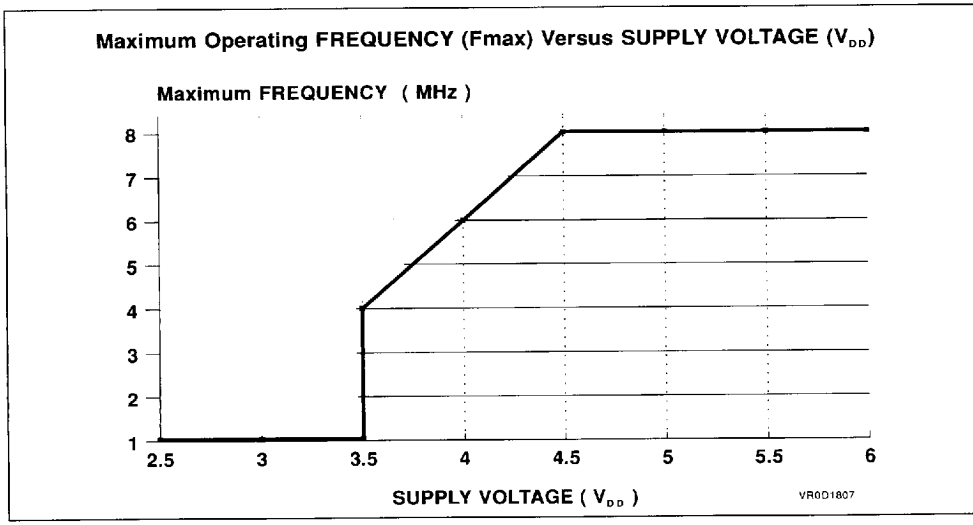
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_A	Operating Temperature	6 Suffix Version 1 Suffix Version	-40 0		85 70	°C
V_{DD}	Operating Supply Voltage	f_{OSC}= 4MHz f_{INT} = 4MHz f_{OSC} = 8MHz f_{INT} = 8MHz	3.5 4.5		6.0 6.0	V V
V_{PP}	EPROM Prog. Voltage		12	12.5	13	V
f_{INT}	Internal Frequency	V_{DD} = 3.5V V_{DD} = 4.5V	0 0		4.0 8.0	MHz MHz
I_{INJ+}	Pin Injection Current (positive) Digital Input (1) Analog Inputs(2)	V_{DD} = 4.5 to 5.5V			+5	mA
I_{INJ-}	Pin Injection Current (negative) Digital Input (1) Analog Inputs	V_{DD} = 4.5 to 5.5V			-5	mA

Notes :

1. A current of ± 5mA can be forced on each pin of the digital section without affecting the functional behaviour of the device. For a positive current injected into one pin, a part of this current (~ 10%) can be expected to flow from the neighbouring pins.

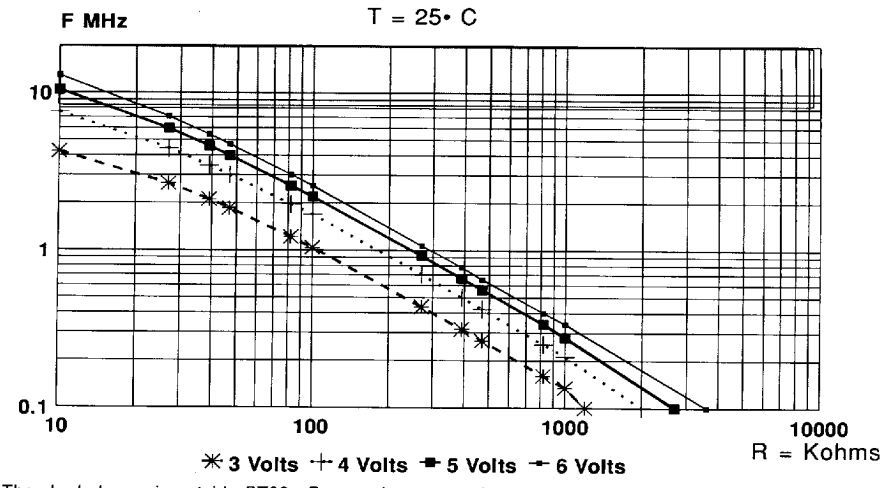
2. If a total current of +1 mA is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 1mA, all the resulting conversions are shifted by +1 LSB. If a total positive current is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 5mA, all the resulting conversions are shifted by +2 LSB.

3. An internal frequency above 1MHz is recommended for reliable A/D results.



The shaded area is outside the device operating range, device functionality is not guaranteed.

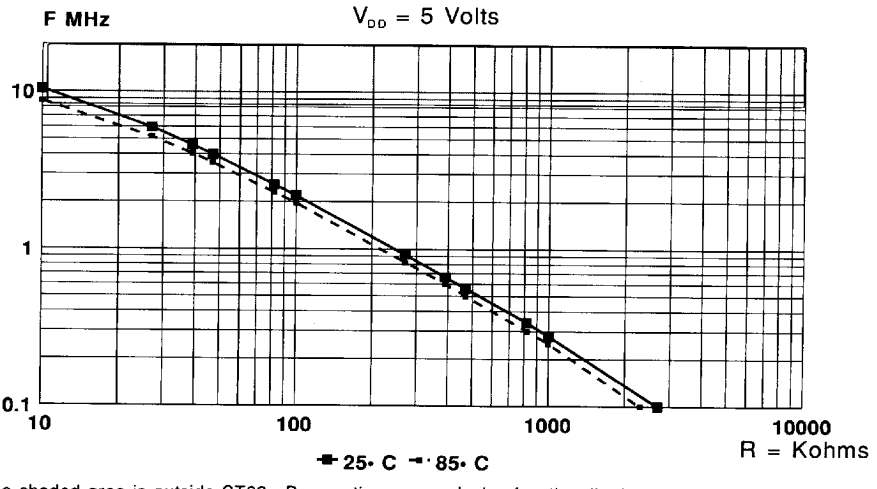
RC Oscillator. f_{OSC} Frequency versus RNET (Typical Values)



The shaded area is outside ST62xxB operating range, device functionality is not guaranteed

VR01935

RC Oscillator. f_{OSC} Frequency versus RNET (Typical Values)



The shaded area is outside ST62xxB operating range, device functionality is not guaranteed

VR01935A

DC ELECTRICAL CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage All inputs				V_{DD} x 0.3	V
V_{IH}	Input High Level Voltage All inputs		V_{DD} x 0.7			V
V_{Hys}	Hysteresis Voltage.(4) All Inputs	V_{DD}=5V V_{DD}=3V	0.2 0.2			V
V_{OL}	Low Level Output Voltage Port A, C	V_{DD}=4.5V I_{OL} = +1.6mA V_{DD}=4.5V I_{OL} = +5.0mA V_{DD}=3.0V I_{OL} = +0.7mA			0.4 1.3 0.4	V
V_{OL}	Low Level Output Voltage Port B	V_{DD}=4.5V I_{OL} = +1.6mA V_{DD}=4.5V I_{OL}=+20.0mA V_{DD}=3.0V I_{OL} = +0.7mA			0.4 1.3 0.4	V
V_{OH}	High Level Output Voltage Port A, B, C	V_{DD}=4.5V I_{OL} = -1.6mA V_{DD}=4.5V I_{OL} = -5.0mA V_{DD}=3.0V I_{OL} = -0.7mA	4.1 3.5 2.6			V
I_{PU}	Input Pull-up Current Input Mode with Pull-up Port A, B, C, NMI	V_{IN} = V_{SS}, V_{DD}=3-6V			100	µA
I_{IL} I_{IH}	Input Leakage Current(1)	V_{IN} = V_{SS} V_{IN} = V_{DD}			1.0	µA
I_{DD}	Supply Current in RESET Mode	V_{RESET}=V_{SS} f_{OSC}=8MHz			3.5	mA
	Supply Current in RUN Mode (2)	V_{DD}=5.0V f_{INT}=8MHz V_{DD}=3.0V f_{INT}=4MHz			6.6 TBD	mA
	Supply Current in WAIT Mode (3)	V_{DD}=5.0V f_{INT}=8MHz V_{DD}=3.0V f_{INT}=4MHz			1.50 TBD	mA
	Supply Current in STOP Mode(3)	I_{LOAD}=0mA V_{DD}=5.0V			10	µA

Notes :

1.Only when pull-ups are not inserted
2.All peripherals running
3.EEPROM and A/D Converter in Stand-by
4.Hysteresis voltage between switching levels

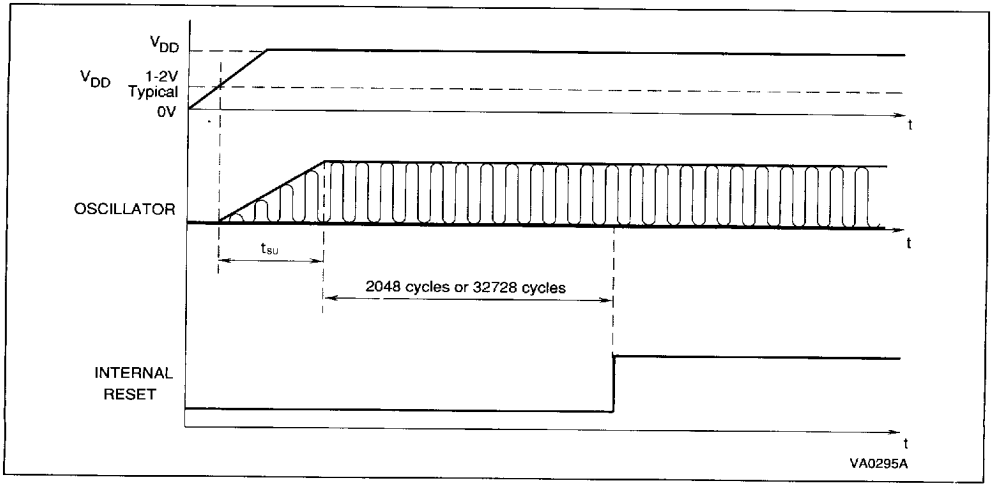
AC ELECTRICAL CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{OSC}	Oscillator Frequency	V_{DD} = 3.5V V_{DD} = 4.0V V_{DD} = 4.5V			4 6 8	MHz
t_{SU}	Oscillator Start-up Time at Power On (2)	Ceramic Resonator $C_{L1} = C_{L2}$ = 22pF		5	100	ms
t_{SUS}	Oscillator STOP mode Recovery Time (2)	8MHz Ceramic Resonator CL1=C_{L2}=22pF		0.2	100	ms
		8MHz Quartz CL1=C_{L2}=22pF		10	100	ms
t_{REC}	Supply Recovery Time (1)		100			ms
T_{WR}	Minimum Pulse Width (V_{DD} = 5V) RESET pin NMI pin		 100 100			ns
T_{WEE}	EEPROM Write Time	T_A = 25°C T_A = 85°C T_A = 125°C		5 10 20	10 20 30	ms
Endurance	EEPROM WRITE/ERASE Cycle	Q_A LOT Acceptance	300,000			cycles
Retention	EEPROM Data Retention	T_A = 55°C	10			years
C_{IN}	Input Capacitance	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance	All Outputs Pins			10	pF

Note:
1. Period for which V_{DD} has to be connected at 0V to allow internal Reset function at next power-up.
2. See Figure 59. This value is highly dependent on the Ceramic Resonator or Quartz Crystal used in the application.

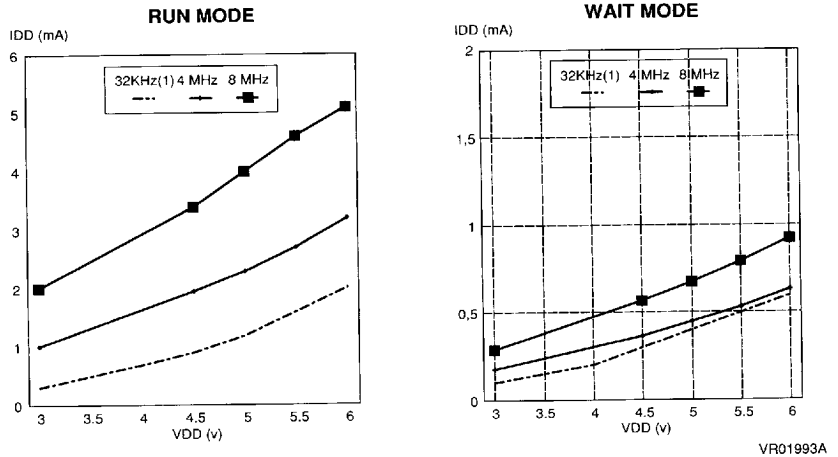
Figure 5. Power On Reset



ELECTRICAL CHARACTERISTICS (Continued)

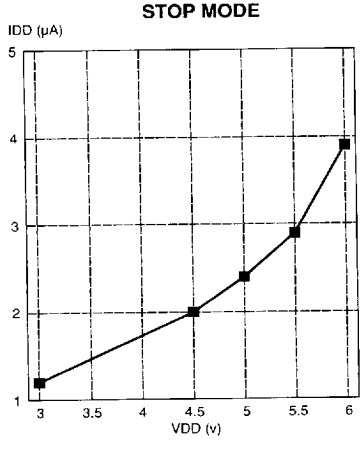
CURRENT CONSUMPTION

IDD Current Versus Supply Voltage
Typical Values (T_A : +85°C)



Note (1) : Using the network described in the Application Note AN673

IDD Current Versus Supply Voltage
Typical Values(T_A : +85°C)



I/O PORT CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage	I/O Pins			0.3x V_{DD}	V
V_{IH}	Input High Level Voltage	I/O Pins	0.7x V_{DD}			V
V_{OL}	Low Level Output Voltage	V_{DD}= 5.0V I_{OL}= 10µA , All I/O Pins I_{OL}= 5mA , Standard I/O I_{OL}= 10mA , Port B I_{OL}= 20mA , Port B			0.1 0.8 0.8 1.3	V
V_{OH}	High Level Output Voltage	I_{OH}= – 10µA I_{OH}= – 5mA, V_{DD}= 5.0V I_{OH}= – 1.5mA, V_{DD}= 3.0V	V_{DD}-0.1 3.5 2.0			V
I_{IL} I_{IH}	Input Leakage Current I/O Pins (pull-up resistor off)	Vin= V_{DD} or V_{SS} V_{DD}= 3.0V V_{DD}= 5.5V		0.1 0.1	1.0 1.0	µA
R_{PU}	Pull-up Resistor	Vin= 0V; All I/O Pins	50	100	200	KΩ

SPI CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{CL}	Clock Frequency at SCK				500	kHz
t_{SV}	Data Set up time on Sin			TBD		
t_H	Data hold time on Sin			TBD		
t_{TS}	Delay Transmission started on Sin	8MHz	0	Note 1		µs

Note :

1. Minimum time 0µs
Maximum time 1 instruction cycle

TIMER1 CHARACTERISTICS
(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{12}{f_{INT}}$			s
f_{IN}	Input Frequency on TIM1 Pin(1)				$\frac{f_{INT}}{4}$	MHz
t_W	Pulse Width at TIM1 Pin(1)	V_{DD} = 3.5V V_{DD} = 4.5V V_{DD} = 5.5V	1 125 125			µs ns ns

Note:
1.Not available for ST6260B

AR TIMER CHARACTERISTICS
(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{1}{f_{INT}}$			s
f_{ARin}	Input Frequency on ARTIMin pin	STOP Mode RUN and WAIT Modes			2 $\frac{f_{INT}}{4}$	MHz MHz
t_W	Pulse Width at ARTIMin Pin	V_{DD} = 3.5V V_{DD} = 4.5V V_{DD} = 5.5V	125 125 125			ns ns ns

A/D CONVERTER CHARACTERISTICS

(T_A= -40 to +85°C unless otherwise specified)

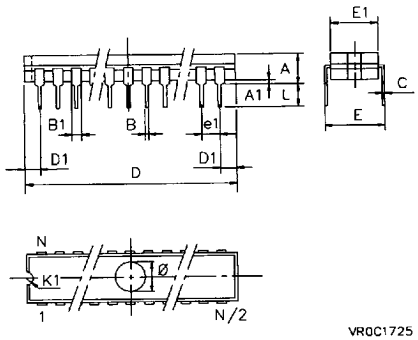
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Res	Resolution			8		Bit
A_{TOT}	Total Accuracy (1) (2)	f_{OSC} > 1.2MHz f_{OSC} > 32kHz			±2 ±4	LSB
t_C (2)	Conversion Time	f_{OSC} = 8MHz		70		µs
V_{AN}	Conversion Range		V_{SS}		V_{DD}	V
ZIR	Zero Input Reading	Conversion result when Vin = V_{SS}	00			Hex
FSR	Full Scale Reading	Conversion result when Vin = V_{DD}			FF	Hex
AD_I	Analog Input Current During Conversion	V_{DD}= 4.5V			1.0	µA
AC_{IN} (3)	Analog Input Capacitance			2	5	pF
ASI	Analog Source Impedance (4)				30	kΩ

Notes:

1. Noise at VDD, VSS <10mV
2. With oscillator frequencies less than 1MHz, the A/D Converter accuracy is decreased.
3. Excluding Pad Capacitance.
4. ASI can be increased as long as the load of the A/D Converter input capacitor is ensured before conversion start.

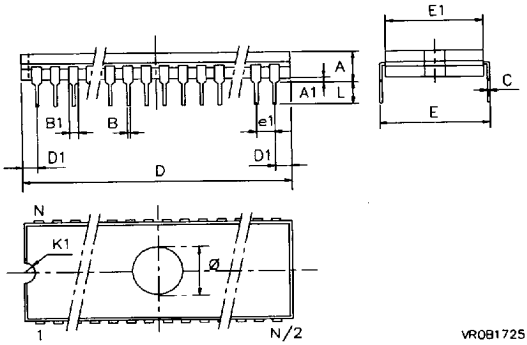
PACKAGE MECHANICAL DATA

Figure 6. 20-Lead Frit Seal Ceramic Dual in Line Package, 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.71			0.225
A1	0.50		1.78	0.020		0.070
B	0.40		0.55	0.016		0.022
B1	1.27		1.52	0.050		0.060
C	0.22		0.31	0.009		0.012
D			26.92			1.059
D1	0.51		1.27	0.020		0.050
E	–	–	–	–	–	–
E1			7.80			0.307
L	3.40			0.134		
e1	2.29		2.79	0.090		0.110
Ø	4.24		4.39	0.167		0.173
	Number of Pins					
N	20					

Figure 7. 28-Lead Frit Seal Ceramic Dual in Line Package, 600-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.71			0.225
A1	0.50		1.78	0.020		0.070
B	0.40		0.55	0.016		0.022
B1	1.17		1.42	.046		.056
C	0.22		0.31	0.009		0.012
D			38.10			1.500
D1	1.52		2.49	.060		.098
E	–	–	–	–	–	–
E1	13.05		13.36	.514		.526
L	3.00			.118		
e1	2.29		2.79	0.090		0.110
Ø	6.86		7.36	.270		.290
	Number of Pins					
N	28					

ORDERING INFORMATION

ORDERING INFORMATION TABLE

Sales Types	OTP/EPROM	I/O	Temperature Range	Package
ST62T60BB6	OTP 4K Bytes	13	-40°C to 85°C	PDIP20
ST62T60BM6				PSO20
ST62T65BB6		21		PDIP28
ST62T65BM6				PSO28
ST62E60BF1	EPROM 4K Bytes	13	0°C to 70°C	CDIP20
ST62E65BF1		21		CDIP28