

SN54LS266, SN74LS266
QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES
WITH OPEN-COLLECTOR OUTPUTS

SDLS151 – DECEMBER 1972 – REVISED MARCH 1988

- Can Be Used as a 4-Bit Digital Comparator
- Input Clamping Diodes Simplify System Design
- Fully Compatible with Most TTL Circuits

FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | H |

H = high level, L = low level

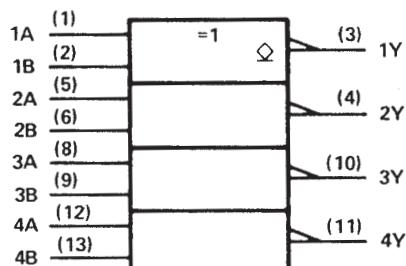
description

The 'LS266 is comprised of four independent 2-input exclusive-NOR gates with open-collector outputs. The open-collector outputs permit tying outputs together for multiple-bit comparisons.

logic symbol (each gate)



logic symbol†



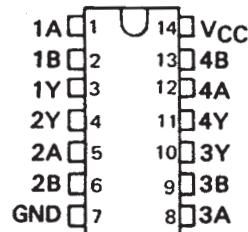
$$\text{positive logic: } Y = \overline{A} \oplus \overline{B} = AB + \overline{AB}$$

† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

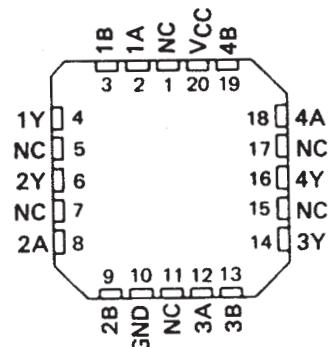
SN54LS266 . . . J OR W PACKAGE
SN74LS266 . . . D OR N PACKAGE

(TOP VIEW)



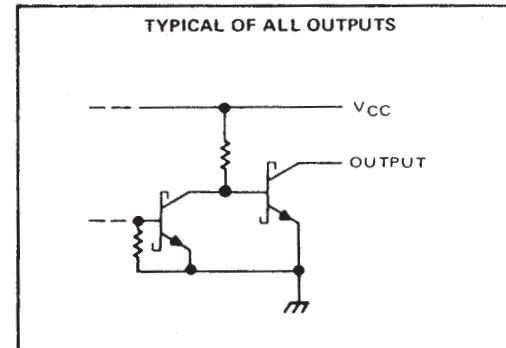
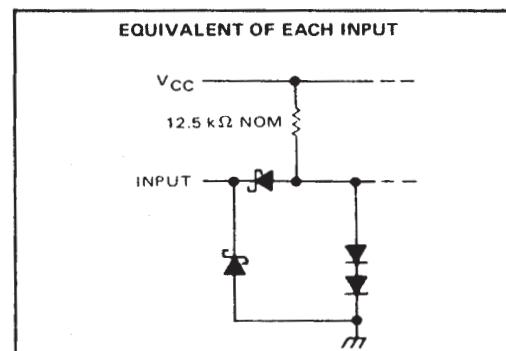
SN54LS266 . . . FK PACKAGE

(TOP VIEW)



NC – No internal connection

schematic of inputs and outputs



SN54LS266, SN74LS266
QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage | 7 V |
| Operating free-air temperature range: SN54LS266 | -55°C to 125°C |
| SN74LS266 | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

| | SN54LS266 | | | SN74LS266 | | | UNIT |
|---------------------------------------|-----------|-----|-----|-----------|-----|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, V_{CC} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output voltage, V_{OH} | | | 5.5 | | | 5.5 | V |
| Low-level output current, I_{OL} | | | 4 | | | 8 | mA |
| Operating free-air temperature, T_A | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS [†] | SN54LS266 | | | SN74LS266 | | | UNIT |
|--|--|-------------------------|------------------|-----|-----------|------------------|-----|------|
| | | MIN | TYP [‡] | MAX | MIN | TYP [‡] | MAX | |
| V_{IH} High-level input voltage | | 2 | | | 2 | | | V |
| V_{IL} Low-level input voltage | | | 0.7 | | | 0.8 | | V |
| V_{IK} Input clamp voltage | $V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$ | | -1.5 | | | -1.5 | | V |
| I_{OH} High-level output current | $V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $V_{OH} = 5.5 \text{ V}$ | | 100 | | | 100 | | μA |
| V_{OL} Low-level output voltage | $V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$ | $I_{OL} = 4 \text{ mA}$ | 0.25 | 0.4 | 0.25 | 0.4 | | V |
| | | $I_{OL} = 8 \text{ mA}$ | | | | 0.35 | 0.5 | |
| I_I Input current at maximum input voltage | $V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$ | | 0.2 | | | 0.2 | | mA |
| I_{IH} High-level input current | $V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$ | | 40 | | | 40 | | μA |
| I_{IL} Low-level input current | $V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$ | | -0.8 | | | -0.8 | | mA |
| I_{CC} Supply current | $V_{CC} = \text{MAX}$, See Note 2 | | 8 | 13 | 8 | 13 | | mA |

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with one input of each gate at 4.5 V, the other inputs grounded, and the outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER [§] | FROM (INPUT) | TEST CONDITIONS | | MIN | TYP | MAX | UNIT | |
|------------------------|-----------------|------------------|--|-----|-----|-----|------|--|
| | | Other input low | Other input high | | | | | |
| t_{PLH} | A or B | Other input low | $C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Note 3 | 18 | 30 | | ns | |
| t_{PHL} | | | | 18 | 30 | | | |
| t_{PLH} | | Other input high | | 18 | 30 | | | |
| t_{PHL} | | | | 18 | 30 | | | |

[§] t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN54LS266J | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54LS266J |
| SN54LS266J.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54LS266J |
| SN74LS266D | Active | Production | SOIC (D) 14 | 50 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS266 |
| SN74LS266D.A | Active | Production | SOIC (D) 14 | 50 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS266 |
| SN74LS266DG4 | Active | Production | SOIC (D) 14 | 50 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS266 |
| SN74LS266N | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS266N |
| SN74LS266N.A | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS266N |
| SNJ54LS266J | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SNJ54LS266J |
| SNJ54LS266J.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SNJ54LS266J |
| SNJ54LS266W | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SNJ54LS266W |
| SNJ54LS266W.A | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SNJ54LS266W |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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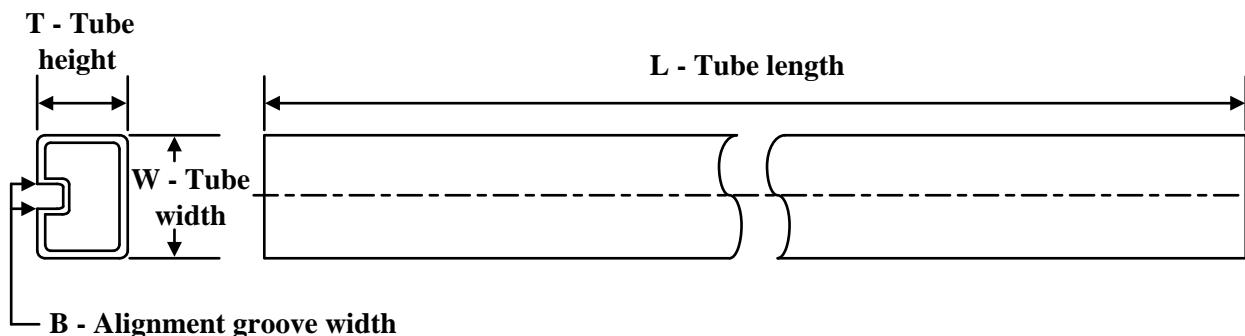
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LS266, SN74LS266 :

- Catalog : [SN74LS266](#)
- Military : [SN54LS266](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE


*All dimensions are nominal

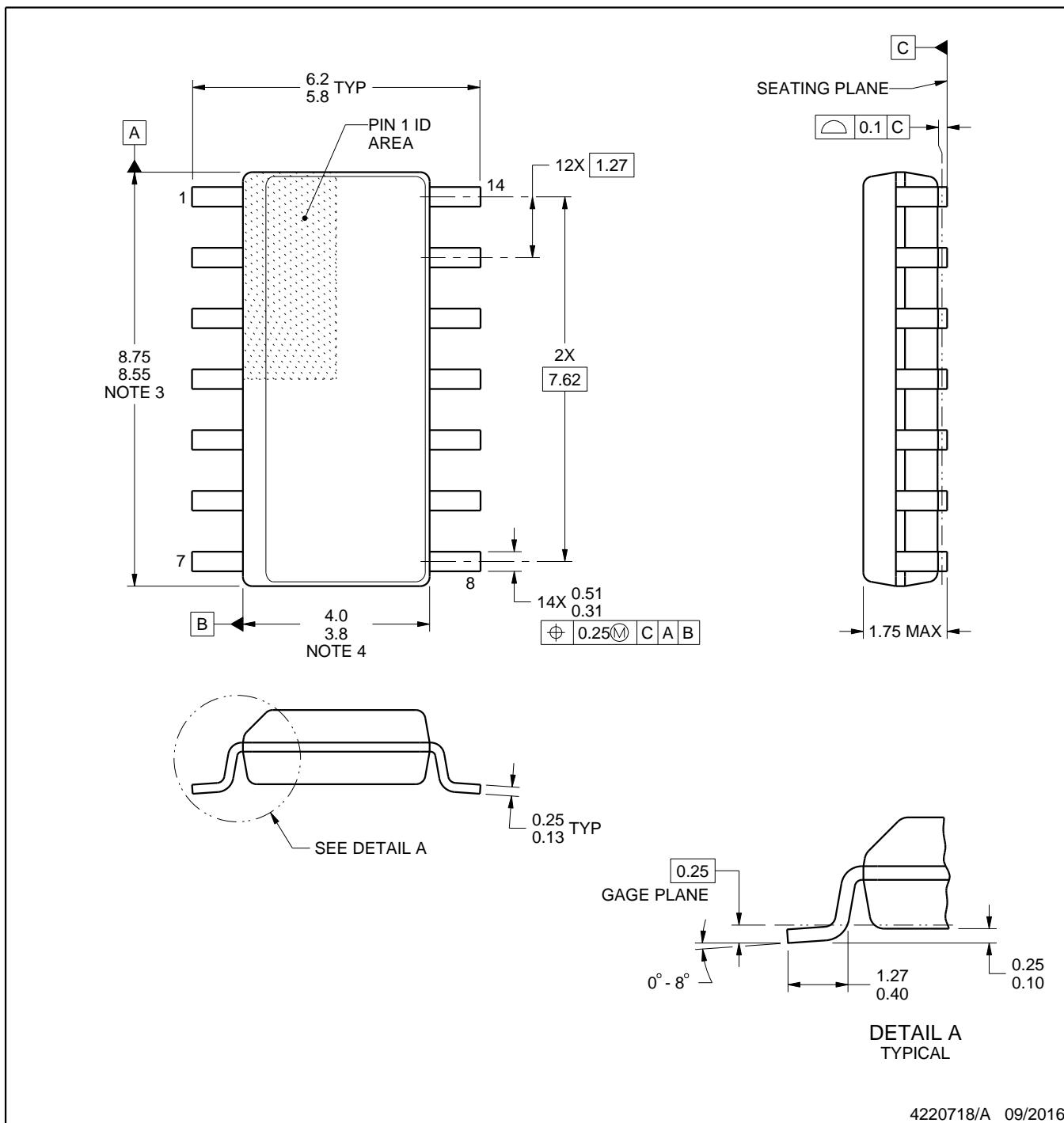
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LS266D | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74LS266D.A | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74LS266DG4 | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74LS266N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS266N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS266N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS266N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54LS266W | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54LS266W.A | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |

PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

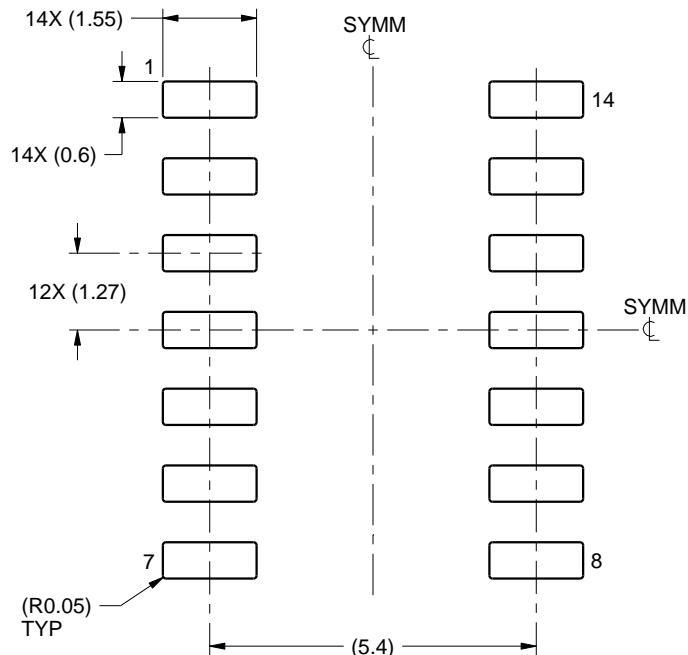
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

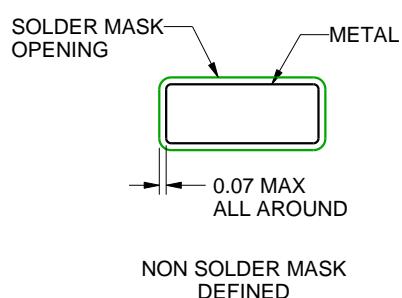
D0014A

SOIC - 1.75 mm max height

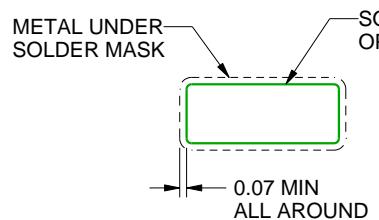
SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

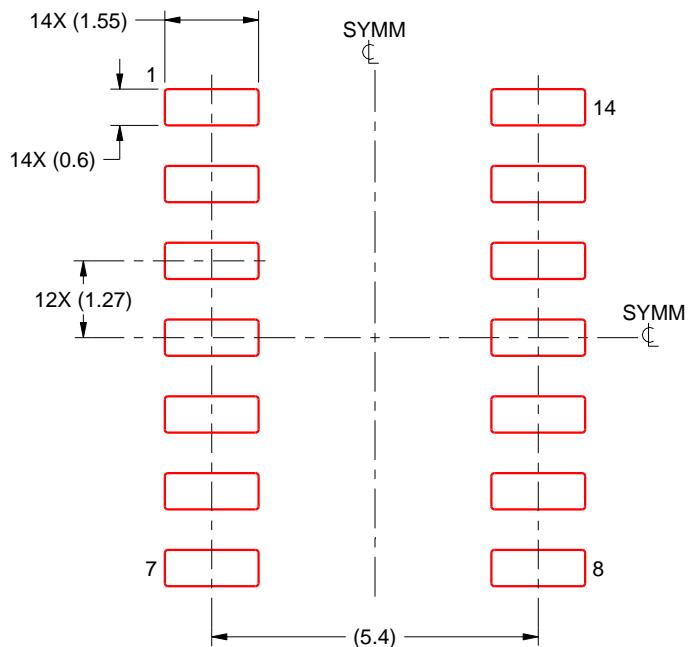
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



**SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X**

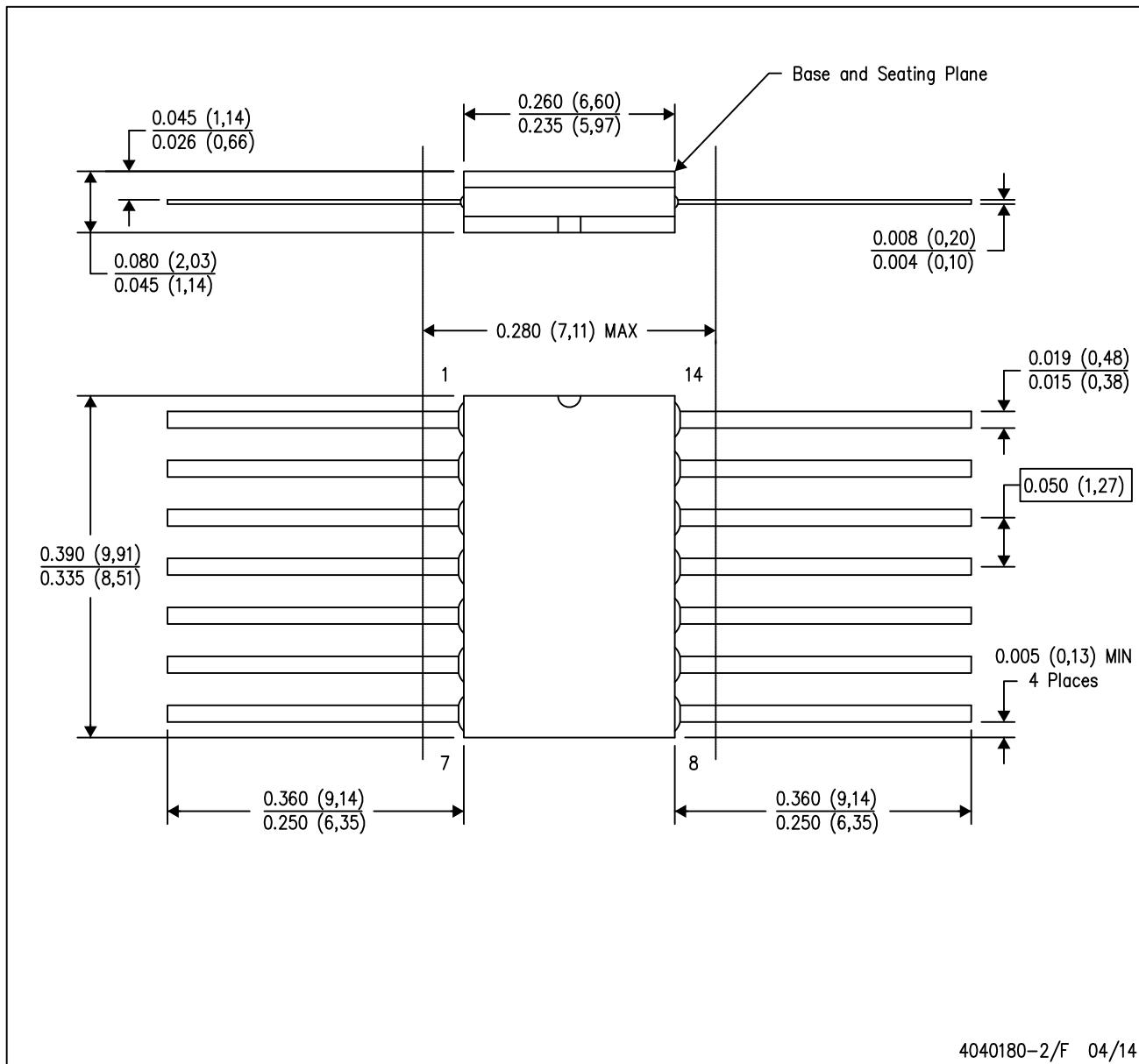
4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/F 04/14

NOTES:

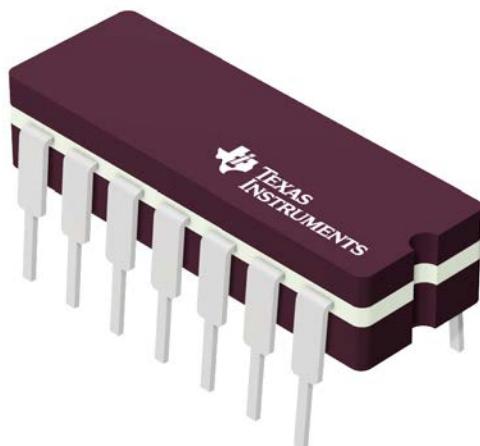
- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within MIL-STD 1835 GDFP1-F14

GENERIC PACKAGE VIEW

J 14

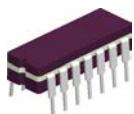
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

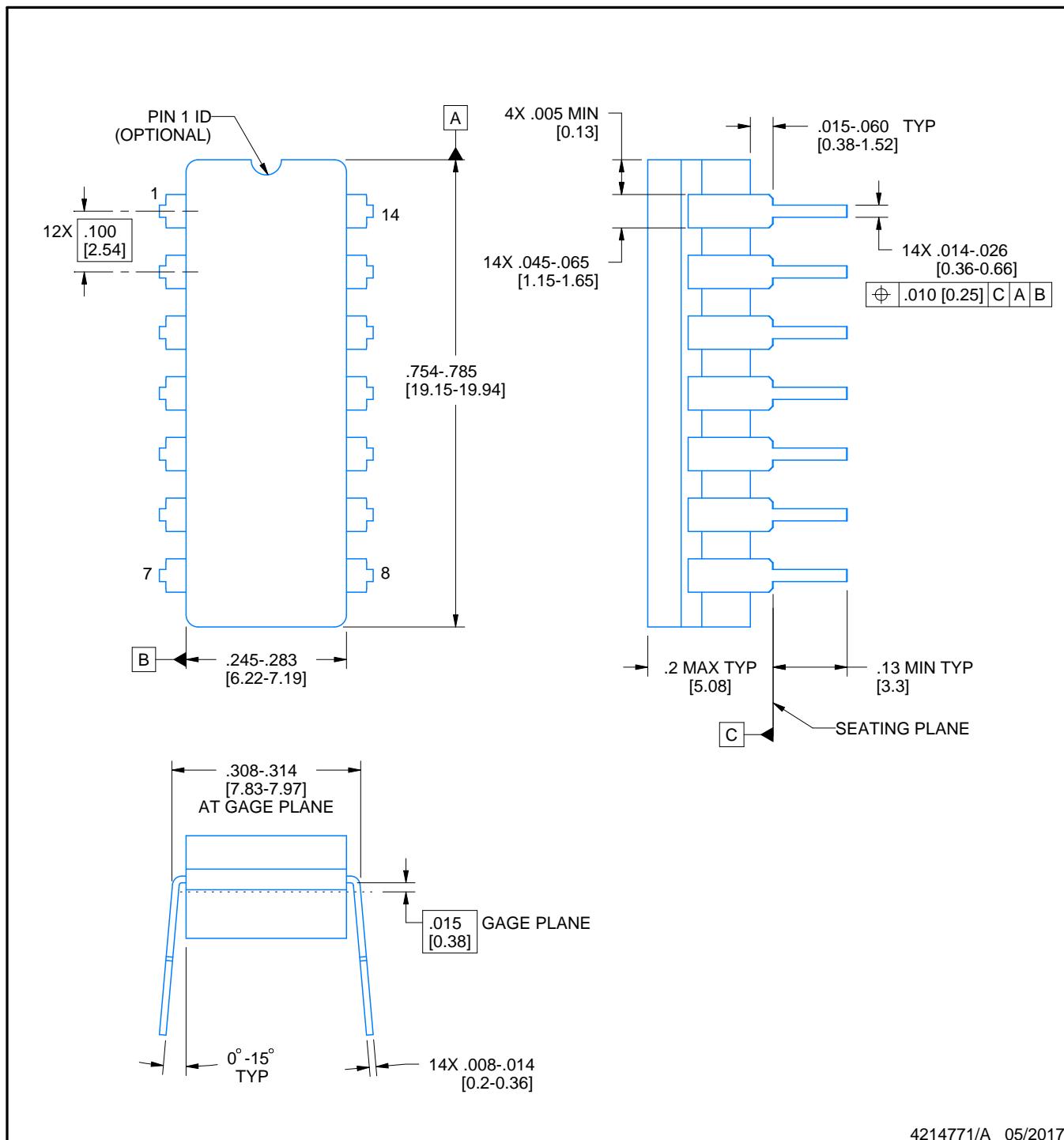


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

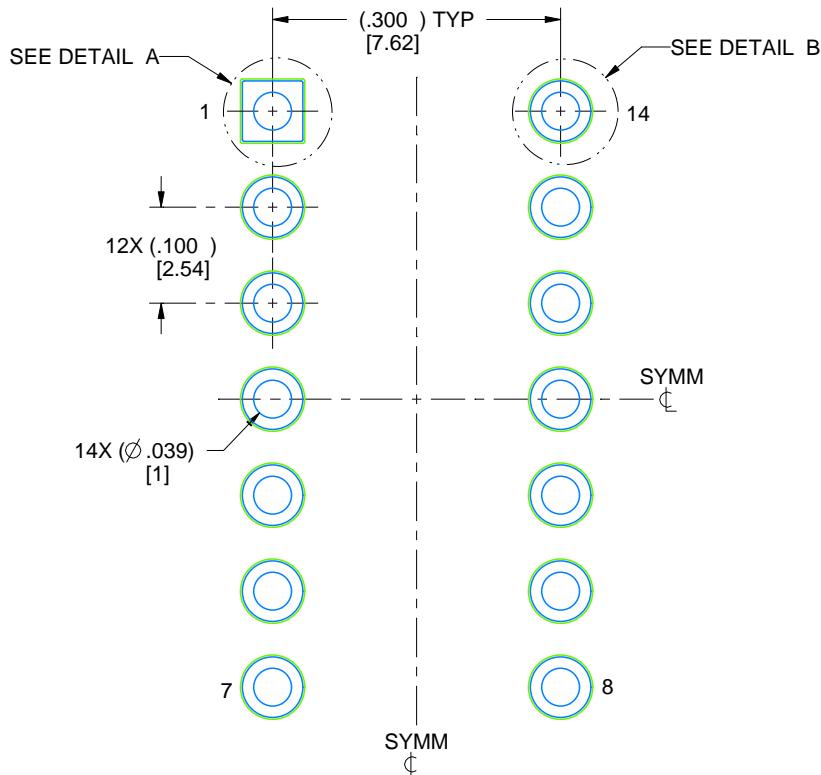
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

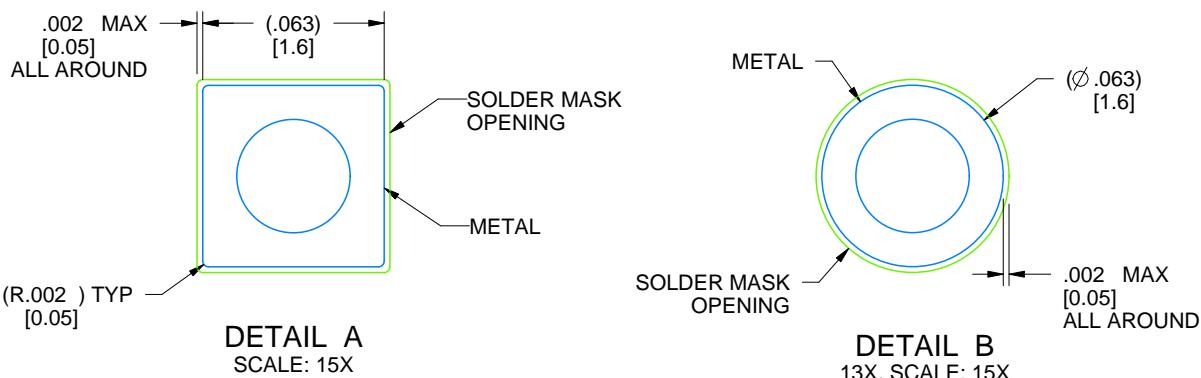
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



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