LED System Driver ICs

ICLS6021J
ICLS6022J
ICLS6022G
ICLS6023J

Off-Line LED Current Mode Controllers
with Integrated 650 V CoolMOS™ & Startup Cell

ICLS6x Series

Data Sheet

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Last Trademarks Update 2011-02-24

Table of Contents

List of Figures

List of Tables

Current Mode Controllers with Integrated 650 V Startup Cell/Depletion CoolMOS™

Product Highlights

- Constant power
- Adjustable blanking window for high-load jumps to increase reliability
- Frequency jittering for low EMI
- Pb-free lead plating, RoHS-compilant

Features

- Frequency jittering for low EMI
- Constant power
- 650 V avalanche-rugged CoolMOS™ with built-in switchable startup cell
- 67 kHz fixed switching frequency
- Auto Restart mode for overtemperature detection
- Auto Restart mode for overvoltage detection
- Auto Restart mode for overload and open loop
- Auto Restart mode for VCC undervoltage
- Floating Load Protection (FLP) mode in the case of open loads
- User-defined soft start
- Minimum number of external components required
- Maximum duty cycle of 75 %
- Overall tolerance of current limiting < ± 5 %
- Internal leading edge blanking
- BiCMOS technology provides a wide VCC range

Description

ICLS6x Series controllers employ a fixed-frequency operation mode optimized for offline LED lighting. The integrated constant power function (patented by Infineon Techologies AG) and the frequency jitter enable high performance without investment of too much effort in stabilization of the system and filtering in terms of EMC.

A wide VCC range up to 26 V is provided by use of BiCMOS technology to cover changes in the auxiliary supply voltage if a CV/CC regulation is implemented on the secondary side.

Auto Restart Mode is entered in the case of overtemperature, VCC overvoltage, output open loop or overload and VCC undervoltage. If an open load event occurs, the device enters the so-called Floating Load Protection (FLP) mode to protect the LED against destruction. The dimensions of the transformer and the secondary diode can be reduced owing to the internal precise peak current limitation to yield greater cost efficiency.

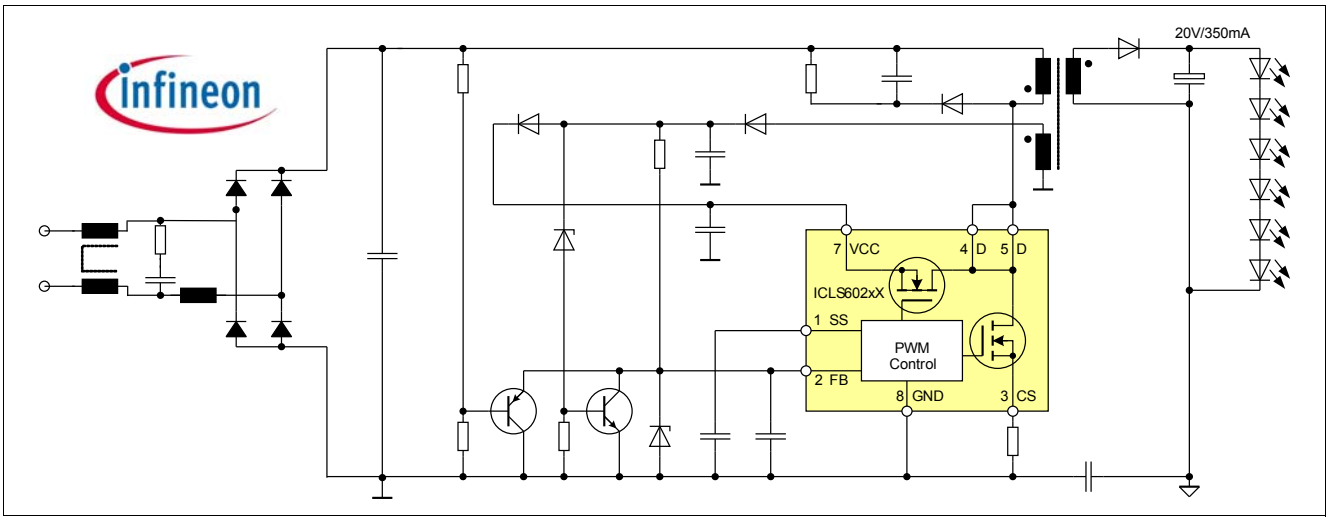


Figure 1 Typical application of ICLS6x Series controllers

Type	Package	Marking	V_{DS}	F_{OSC}	R_{DSon} [1]	230 VAC ± 15 % [2]	110 VAC ± 15 % [2]
ICLS6021J	PG-DIP-8-6	ICLS6021J	650 V	67 kHz	6.45 Ω	12 W	5 W
ICLS6022J	PG-DIP-8-6	ICLS6022J	650 V	67 kHz	4.70 Ω	17 W	9 W
ICLS6022G	PG-DSO-16/12	ICLS6022G	650 V	67 kHz	4.70 Ω	17 W	9 W
ICLS6023J	PG-DIP-8-6	ICLS6023J	650 V	67 kHz	1.70 Ω	26 W	15 W

1) typ. @ T = 25 °C

2) Calculated maximum input power rating at T_a = 80 °C, T_j = 125 °C and without copper area as heat sink

1 Pin Configuration and Functionality

1.1 Pin Configuration for PG-DIP-8-6

Table 1 Pin Configuration for PG-DIP-8-6

Pin	Symbol	Function
1	SoftS	Soft start
2	FB	Feedback
3	CS	Current Sense / 650 V[1)] depletion CoolMOS source™
4	Drain	650 V[1)] depletion CoolMOS source™
5	Drain	650 V[1)] depletion CoolMOS source™
6	n.c.	Not connected
7	VCC	Controller supply voltage
8	GND	Controller ground

1) @ T_j = 110 °C

1.2 PG-DIP-8-6 Package

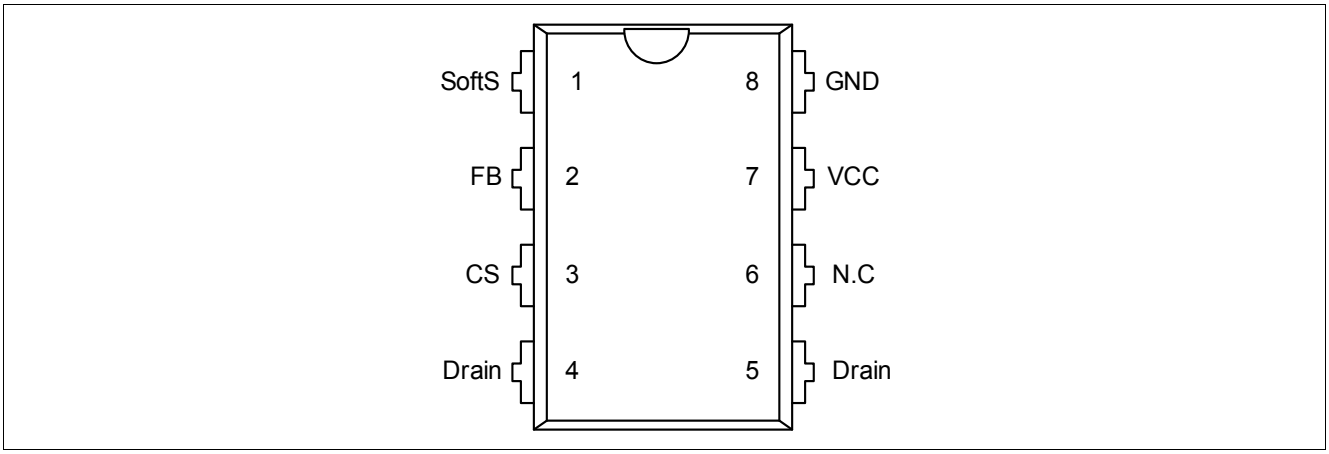


Figure 2 Pin configuration of PG-DIP-8-6 (top view)

1.3 Pin Configuration for PG-DSO-16/12

Table 2 Pin Configuration for PG-DSO-16/12

Pin	Symbol	Function
1	n.c.	Not connected
2	SoftS	Soft start
3	FB	Feedback
4	CS	Current Sense / 650 V[1)] depletion CoolMOS source™
5	Drain	650 V[1)] depletion CoolMOS source™
6	Drain	650 V[1)] depletion CoolMOS source™
7	Drain	650 V[1)] depletion CoolMOS source™
8	Drain	650 V[1)] depletion CoolMOS source™
9	n.c.	Not connected
10	n.c.	Not connected
11	VCC	Controller supply voltage
12	GND	Controller ground

1) @ T_j = 110 °C

1.4 PG-DSO-16/12 Package

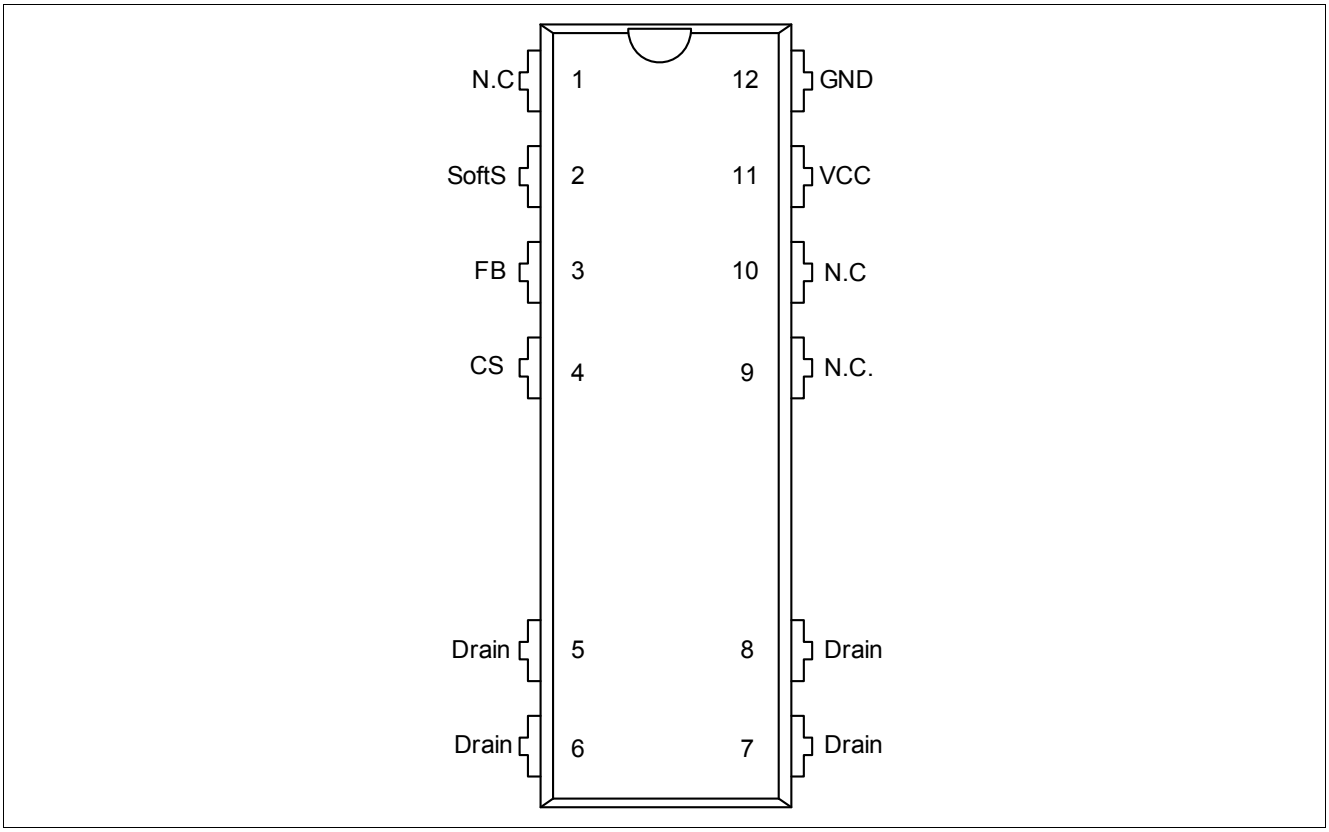


Figure 3 Pin configuration of PG-DSO-16/12 (top view)

1.5 Pin Functionality

SoftS (soft start, auto restart & frequency jittering control)

The SoftS pin combines the soft start function during startup and the error detection function for Auto Restart mode. These functions are implemented and can be adjusted by means of an external capacitor at the SoftS pin connected to ground. This capacitor also provides an adjustable blanking window for high load jumps before the IC enters Auto Restart mode. In addition, this pin is also used to control the period of frequency jittering under normal loads.

FB (feedback)

The information on the regulation is provided by the FB pin to the internal protection unit and to the internal PWM comparator to control the duty cycle. In the event of an open load event, the device enters the Floating Load Protection (FLP) mode.

CS (current sense)

The current sense pin senses the voltage developed on the series resistor inserted into the source of the integrated depletion CoolMOS™. If CS reaches the internal threshold of the current limit comparator, the driver output is immediately switched off. The current information is provided to the PWM comparator to realize the current mode.

Drain (drain of integrated depletion CoolMOS™)

The drain pin provides the connection to the drain of the internal depletion CoolMOS™.

VCC (power supply)

The VCC pin is the positive supply of the IC. The operating range of the supply is between 10.3 V and 26 V.

GND (ground)

The GND pin is the common ground of the controller.

2 Block Diagram

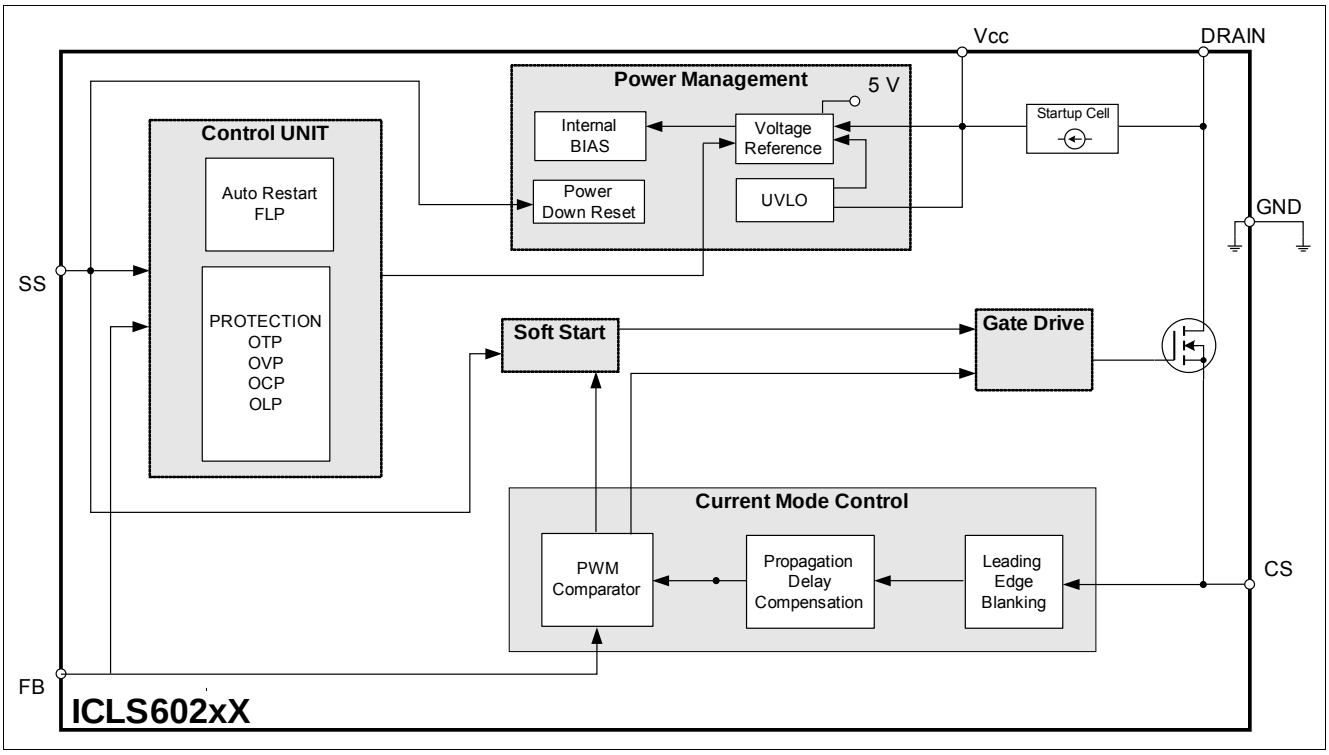


Figure 4 Block diagram of ICLS6x Series controllers

3 Functional Description

All values used in the functional description are typical values. When calculating the worst cases, the minimium/maximum values listed in **Electrical Characteristics** on page **24** have to be considered.

3.1 Introduction

For ICLS6x Series controllers, a high voltage startup cell is integrated into the system IC, which is switched off once the undervoltage lockout-on threshold of 18 V is exceeded. This startup cell is part of the integrated depletion CoolMOS™. The external startup resistor is no longer necessary as the startup cell is connected to the drain, resulting in reduced power losses. This increases the efficiency under light load conditions drastically.

The soft start capacitor is also used for providing an adjustable blanking window for high load jumps. The overload detection function is disabled during this window. With this concept, no further external components are necessary to adjust the blanking window.

An Auto Restart mode is implemented in the IC to reduce the average power conversion in the event of malfunction or unsafe operating conditions in the LED drives. This feature increases the system's robustness and safety, which would otherwise lead to a destruction of the LED drive. Once the malfunction is corrected, normal operation is automatically initiated after the next startup phase.

Together with the soft start capacitor, the feedback can also sense a missing load, which leads to rising output and auxiliary voltages. This triggers the Floating Load Protection (FLP) mode. When feedback falls below 1.35 V, the Soft Start voltage begins to rise up to a threshold of 4 V (depends on the C4 value) and the IC is switched into FLP mode.

The precise internal peak current limitation reduces the costs for the transformer and the secondary diode. The influence of the change in the input voltage on the power limitation can be avoided together with the integrated Propagation Delay Compensation circuit. Consequently, the maximum power is practically independent of the input voltage required for wide range LED drives. There is no need for additional oversizing of the LED drives – e.g., for the transformer or the secondary diode.

3.2 Power Management

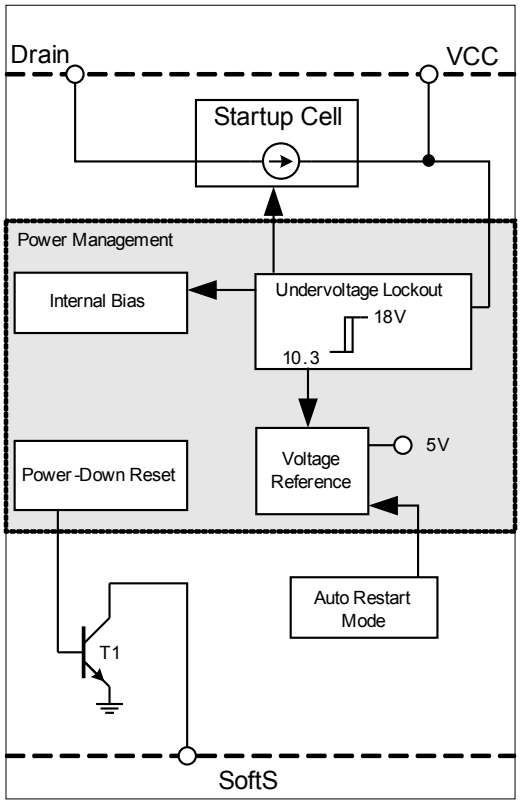


Figure 5 Power management of ICLS6x Series controllers

The undervoltage lockout function monitors the external supply voltage V_{VCC}. When the LED drive is connected to the main line, the internal startup cell is biased and starts to charge the external capacitor C_{VCC}, which is connected to the VCC pin. The VCC charge current that is provided by the startup cell from the drain pin is 1.05 mA. If V_{VCC} exceeds the on-threshold V_{CCon} (= 18 V), the bias circuit is switched on. Then the startup cell is switched off by the undervoltage lockout; therefore no power losses are present due to the connection of the startup cell to the drain voltage. An hysteresis loop is implemented to avoid uncontrolled ringing at switch-on. Switch-off of the controller can only take place after the active mode has been entered and V_{VCC} has fallen below 10.3 V.

The maximum current consumption before the controller is activated is about 300 μA.

If V_{VCC} falls below the off-threshold V_{CCoff} (= 10.3 V), the bias circuit is switched off and a power-down reset causes discharging of the soft-start capacitor C_{SoftS} at pin SoftS via T4 (see **Figure 5**). This ensures in every startup cycle that the voltage ramp at the SoftS pin starts at zero.

The bias circuit is switched off if Auto Restart mode is entered. The current consumption is then reduced to 300 μA.

Once the malfunction condition is resolved, this block will then turn back on. The recovery from Auto Restart mode does not require disconnection of the LED drive from the AC line.

3.3 Startup Phase

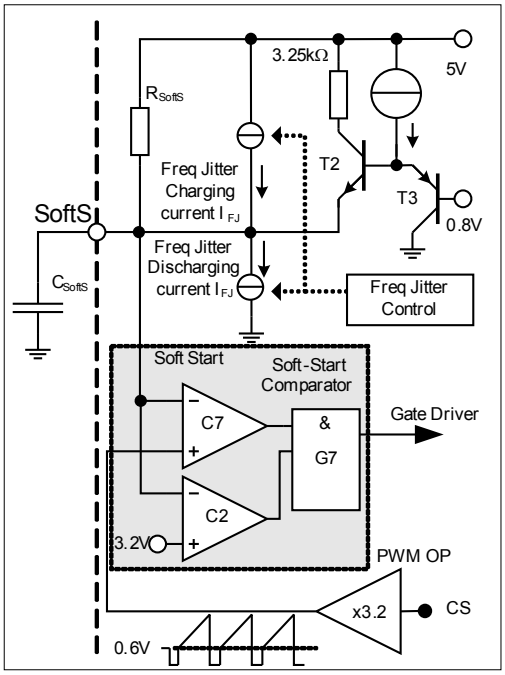


Figure 6 Soft start

At the beginning of the startup phase, the IC provides a soft start period during which it controls the maximum primary current by means of duty cycle limitation. A capacitor C_{Softs} in combination with the internal pull-up resistor R_{SoftS} determines the duty cycle until V_{SoftS} exceeds 3.2 V.

When the soft start begins, C_{SoftS} is immediately charged up to approx. 0.8 V by T2. The soft start phase takes place between 0.8 V and 3.2 V. Above V_{SoftsS} = 3.2 V there is no longer any duty cycle limitation DC_{max} that is controlled by the comparator C7 since the comparator C2 blocks the gate G7 (see **Figure 7**). This maximum charge current in the very first stage when V_{SoftS} is below 0.8 V is limited to 0.9 mA.

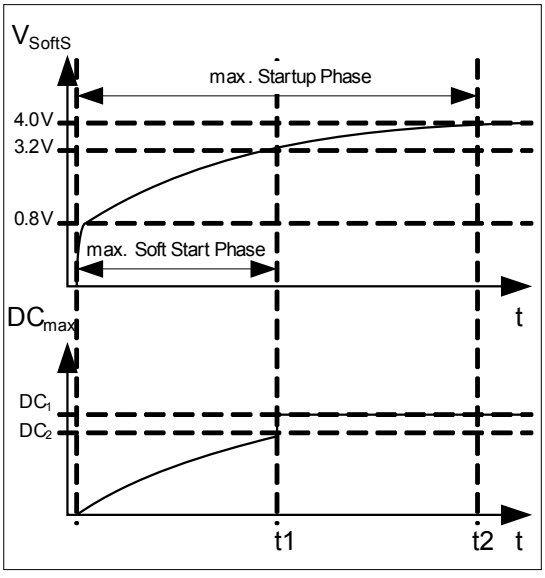


Figure 7 Startup phase

As a consequence of this extra charge stage, there is no delay at the beginning of the startup phase when there is still no switching. Furthermore, soft start is finished at 3.2 V to have maximum power capability even earlier. The duty cycles DC_1 and DC_2 vary according to the mains and the primary inductance of the transformer. The limitation of the primary current by DC_2 is related to V_{SoftS} = 3.2 V. However, DC_1 is related to a maximum primary current, which is limited by the internal current limiting function with CS = 1 V. Therefore the maximum startup phase is divided into a soft start phase until t1 and a phase from t1 to t2 during which maximum power is provided if demanded by the FB signal.

3.4 PWM Section

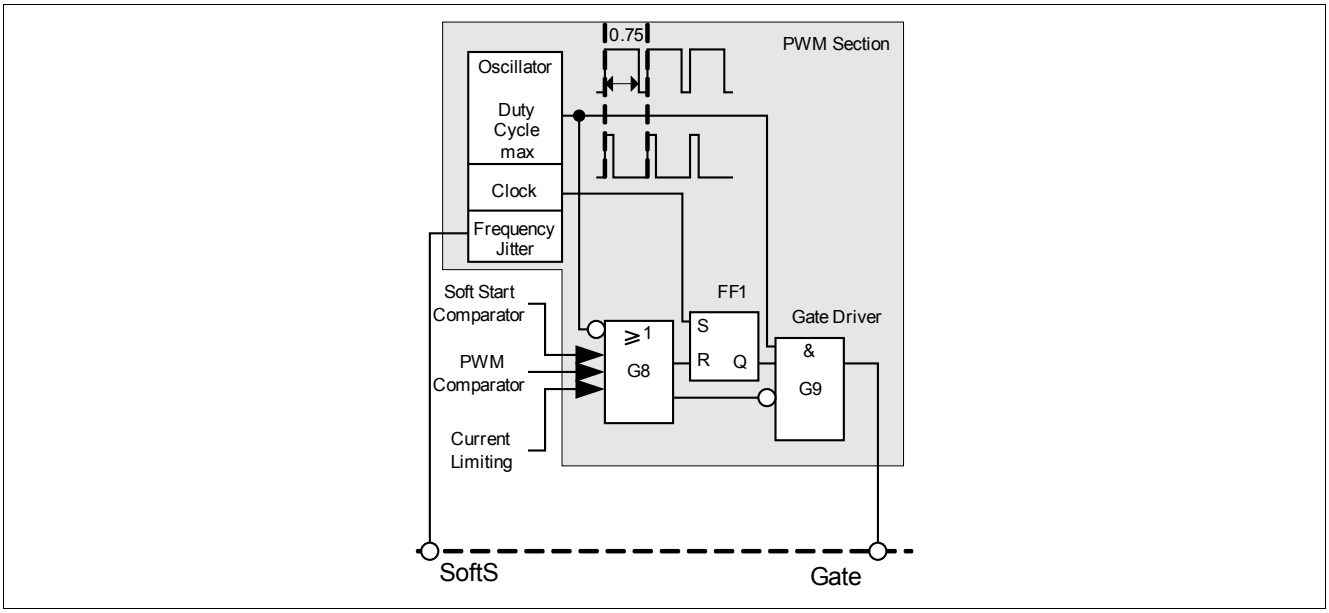


Figure 8 PWM section

3.4.1 Oscillator and Jittering

The oscillator generates a fixed frequency with frequency jittering of ± 4 % from the fixed frequency (i.e., ± 2.7 kHz for 67 kHz) at a jittering period T_{FJ}. The switching frequency is f_{switch} = 67 kHz.

A resistor, a capacitor, a current source and current sink for determining the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed in order to achieve a very accurate switching frequency. The ratio of controlled charge to discharge current is adjusted to reach a maximum duty cycle limitation of D_{max} = 0.75.

Once the soft start period is over and the IC has entered normal mode, the soft start capacitor is charged and discharged through the internal current source I_{FJ} to generate a triangular waveform with a jittering period T_{FJ}, which is externally adjustable by means of the soft start capacitor, C_{SoftS} (see **Figure 6**).

$$T_{FJ} = k_{FJ} * C_{SoftS} \quad (1)$$

where k_{FJ} is a constant = 4 ms/µF.

For example: T_{FJ} = 4 ms if C_{SoftS} = 1µF.

3.4.2 PWM Latch FF1

The oscillator clock output provides a set pulse to the PWM latch when initiating the internal CoolMOS™ conduction. After being set, the PWM latch can be reset by the PWM comparator, the soft start comparator or the current limit comparator. In resetting situations the driver is shut down immediately.

3.4.3 Gate Driver

The gate driver is a fast totem pole gate drive designed to avoid cross conduction currents. It is active low at voltages below the undervoltage lockout threshold V_{VCCoff}.

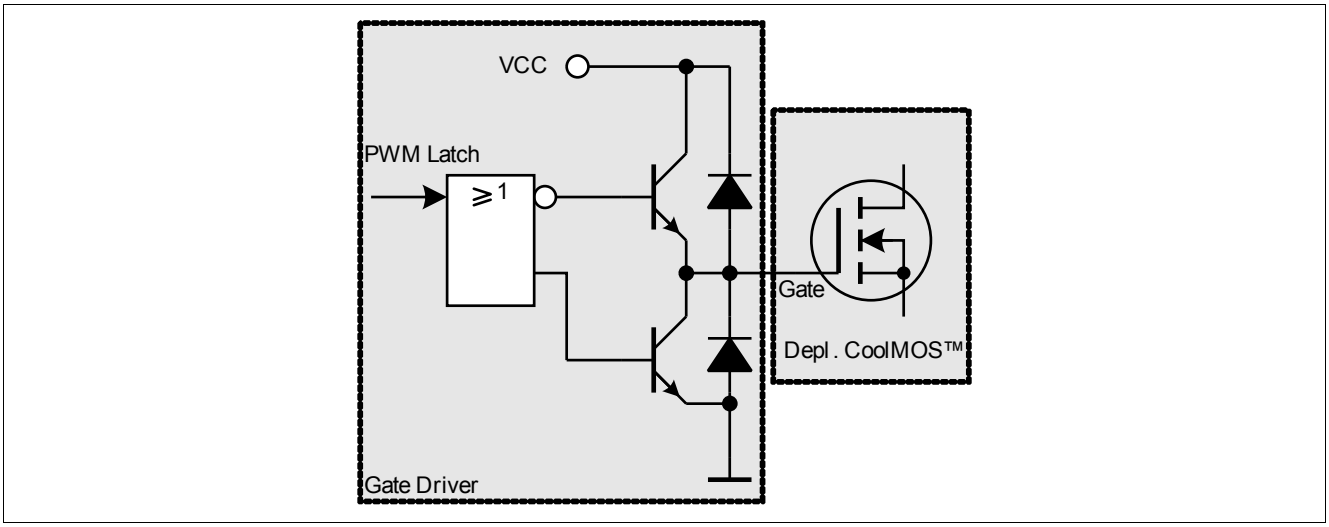


Figure 9 Gate driver

3.5 Current Limiting

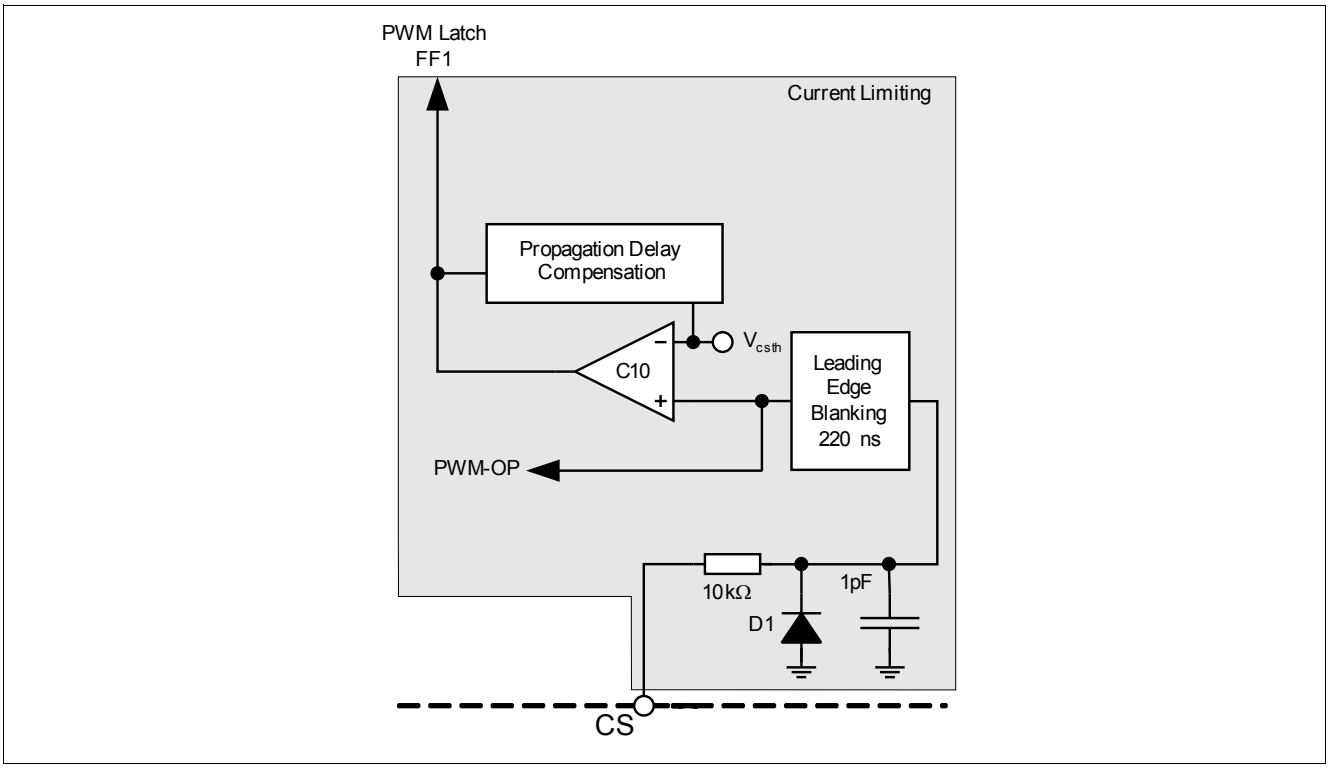


Figure 10 Current limiting

Cycle-by-cycle current limiting realized by the current limit comparator C10 to provide overcurrent detection (see **Figure 10**). The source current of the integrated depletion CoolMOS™ is sensed by means of an external sense resistor R_{Sense}. By means of R_{Sense} the source current is transformed to a sense voltage V_{Sense} which is fed to the CS pin. If V_{Sense} exceeds the internal threshold voltage V_{csth} the comparator C10 immediately turns off the gate drive by resetting the PWM latch FF1. A Propagation Delay Compensation circuit is added to support immediate shutdown without delay of the integrated internal CoolMOS™ in the case of current limiting. The influence of the AC input voltage on the maximum output power can be suppressed as a result.

To prevent the current limiting function from causing distortions by leading edge spikes, a Leading Edge Blanking circuit is integrated into the current sense path for the comparator C10 and the PWM OP.

3.5.1 Leading Edge Blanking

Each time when the integrated internal CoolMOS™ is switched on, a leading edge spike is generated due to the primary-side capacitances and secondary-side rectifier reverse recovery time. This spike can cause the gate drive to switch off unintentionally. To avoid premature termination of the switching pulse, this spike is blanked out with a time constant of t_{LEB} = 220 ns. During this time, the gate drive will not be switched off. This is illustrated in **Figure 11**.

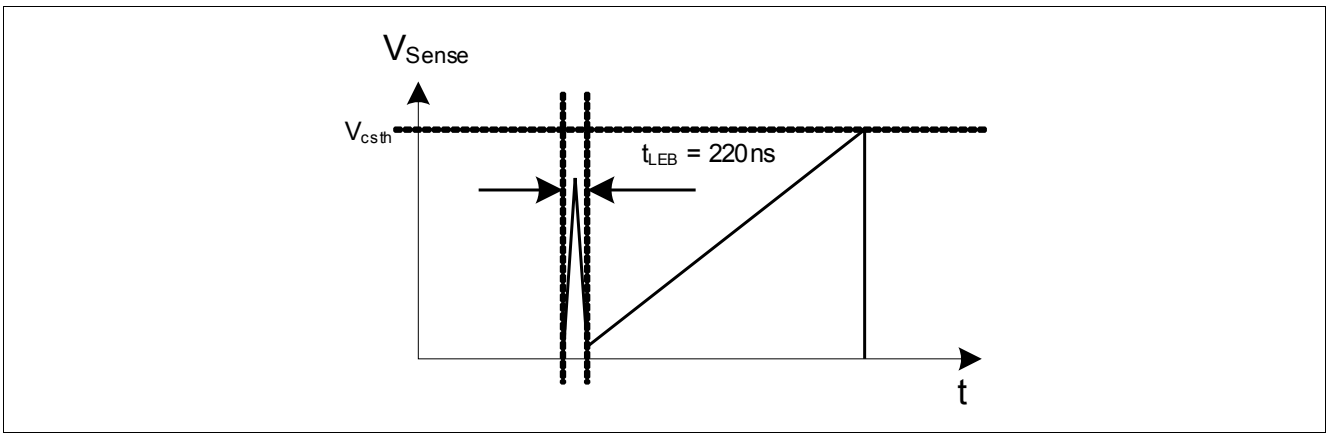


Figure 11 Leading edge blanking

3.5.2 Propagation Delay Compensation

In the case of overcurrent detection, switch-off of the integrated internal CoolMOS™ is delayed due to the propagation delay of the circuit. This delay causes an overshoot of the peak current I_{peak}, which depends on the ratio of dI/dt of the peak current (see **Figure 12**).

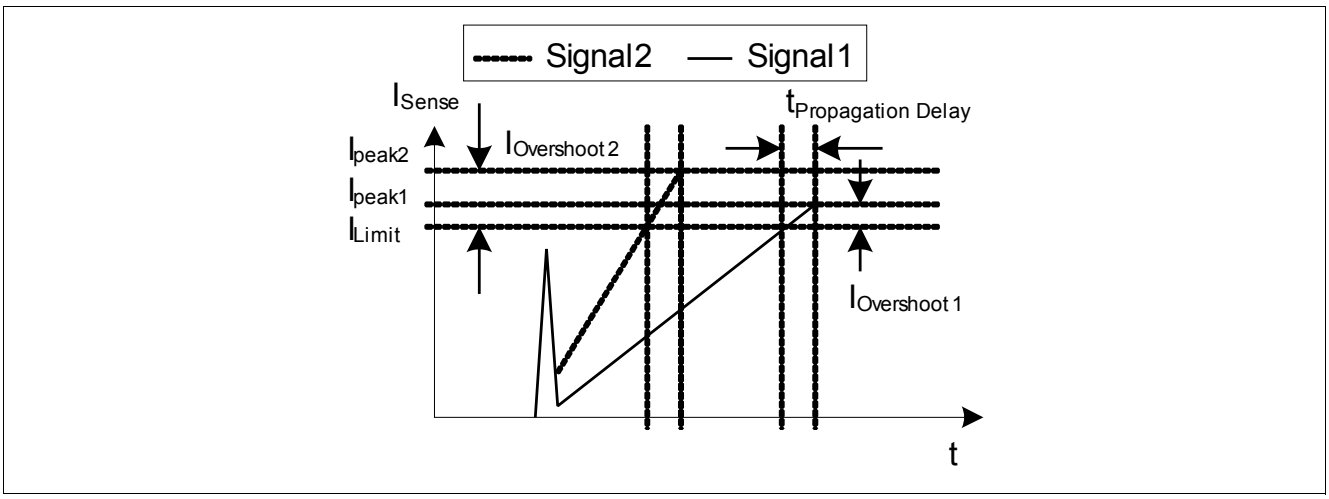


Figure 12 Peak current overshooting

The overshoot of Signal2 is greater than that of Signal1 due to the steeper rising waveform. This change in the slope varies according to the AC input voltage. A Propagation Delay Compensation circuit is integrated to limit the overshoot dependency on dI/dt of the rising primary current. This means that the propagation delay between the time the current sense threshold V_{csth} is exceeded and switch-off of the integrated inernal CoolMOS™ is compensated over temperature within a wide range.

Extremely precise current limiting is now possible.

For example, I_{peak} = 0.5 A with R_{Sense} = 2 Ω. Without propagation delay compensation the current sense threshold is set to a static voltage level V_{csth} = 1 V. A current ramp of dI/dt = 0.4 A/µs (that means, dV_{Sense}/dt = 0.8 V/µs), and a propagation delay time $t_{Propagation\ Delay}$ = 180 ns then leads to an I_{peak} overshoot of 14.4 %. With propagation delay compensation the overshoot is only about 2 % (see **Figure 13**).

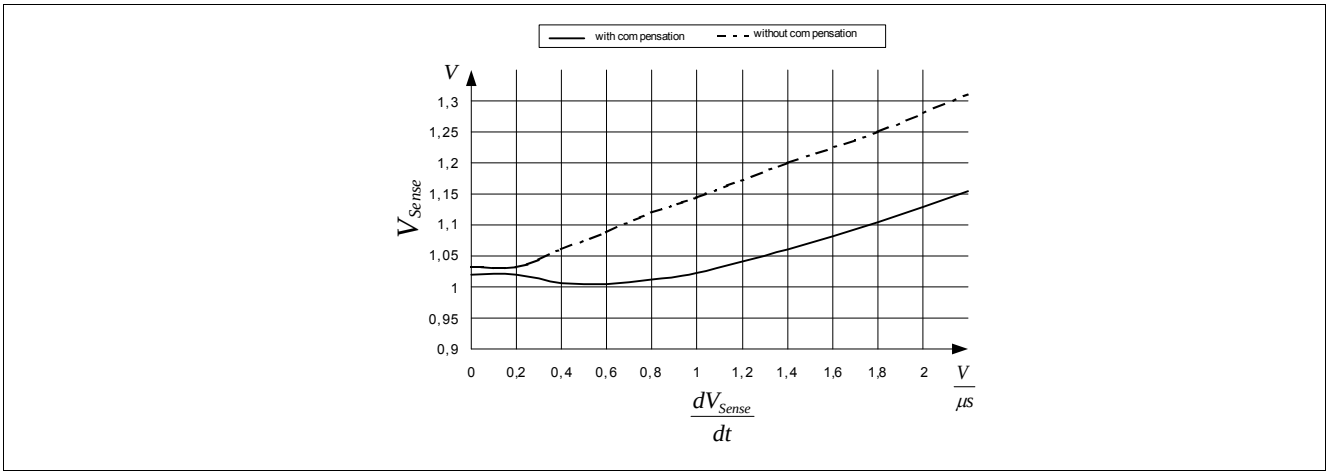


Figure 13 Overcurrent shutdown

Propagation delay compensation is realized by means of a dynamic threshold voltage V_{csth} (see **Figure 14**). If the slope is steeper, driver switch-off takes place earlier to compensate for the delay.

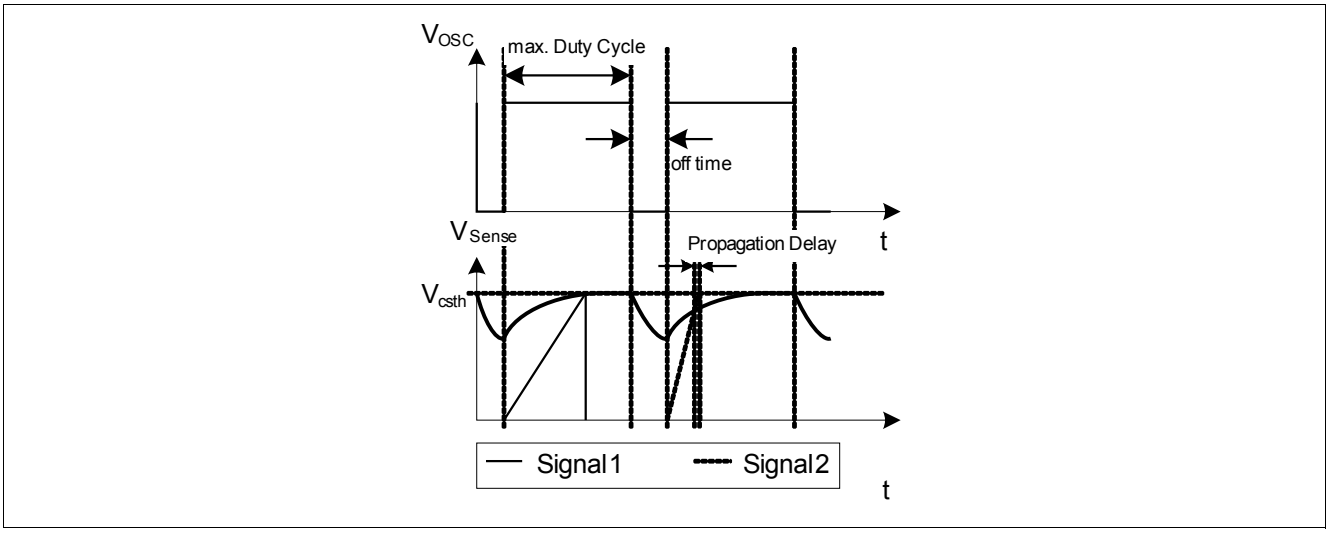


Figure 14 Dynamic voltage threshold V_{csth}

3.6 Control Unit

The Control Unit contains the functions for the Auto Restart and Floating Load Protection (FLP) modes. The Auto Restart mode is combined with an adjustable blanking window, which varies according to the value of the external soft start capacitor. The IC avoids entering into either of these two modes accidentally by means of this adjustable blanking window. The window also provides a certain time during which overload detection is delayed. This delay is useful for applications that normally work with a low current and occasionally require a short duration of high current.

3.6.1 Adjustable Blanking Window

V_{SoftS} swings between 3.2 V and 3.6 V after the LED drive has settled and S2 is on while S3 is off. This behavior is due to the frequency jittering function that makes use of the soft start pin. If overload occurs, V_{FB} exceeds 4.5 V. The Auto Restart mode cannot be entered as the gate G5 is still blocked by the comparator C3. However, after V_{FB} has exceeded 4.5 V, the switch S2 is opened and S3 is closed. The external soft start capacitor can then be further charged by the integrated pull-up resistor R_{SoftS} through the switch S3. The comparator C3 releases the gate G5 once V_{SoftS} has exceeded 4.0 V. This means that Auto Restart mode cannot be entered during the charging time of the external capacitor C_{SoftS}.

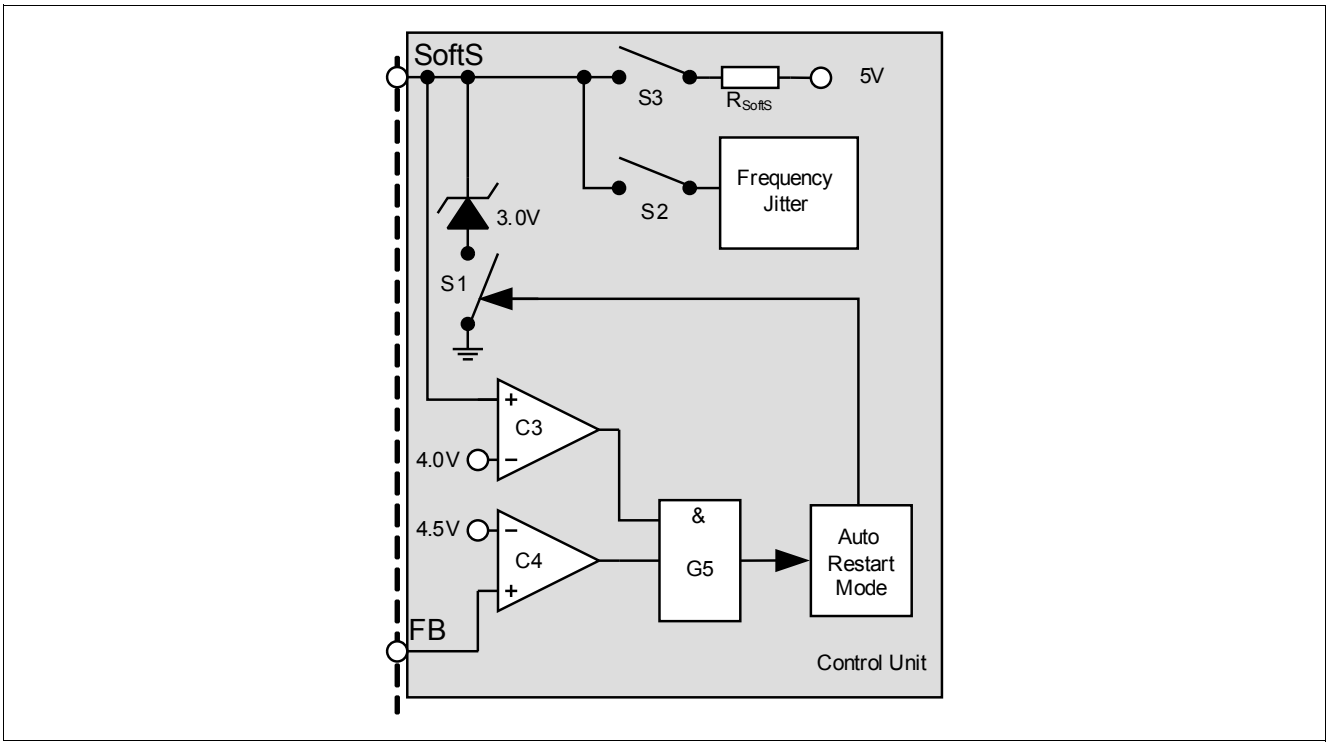


Figure 15 Adjustable blanking window

3.6.2 Protection Modes

The IC provides several protection features to increase the LED drive's robustness and safety. The following table shows the possible system failures and the corresponding protection modes.

Table 3 Protection modes

VCC Overvoltage	Auto Restart mode during startup
Overtemperature	Auto Restart mode during RUN mode
Overload	Auto Restart mode during RUN mode
Open Loop	Auto Restart mode during RUN mode
VCC Undervoltage	Auto Restart mode during RUN mode
Floating Load Protection (FLP)	Floating Load Protection mode

3.6.2.1 Auto Restart Mode during Startup

The VCC voltage is observed by the comparator C13 if 20.5 V is exceeded. The output of C13 is combined with both the output of C3, which checks for V_{SoftS} < 4.0 V, and the output of C4, which checks for V_{FB} > 4.5 V. Therefore, overvoltage detection can only be active during the soft start phase (V_{SoftS} < 4.0 V) and if the FB signal is outside the operating range (> 4.5 V). This means any small voltage overshoots of V_{VCC} occurring during normal operation cannot trigger the Auto Restart mode during startup.

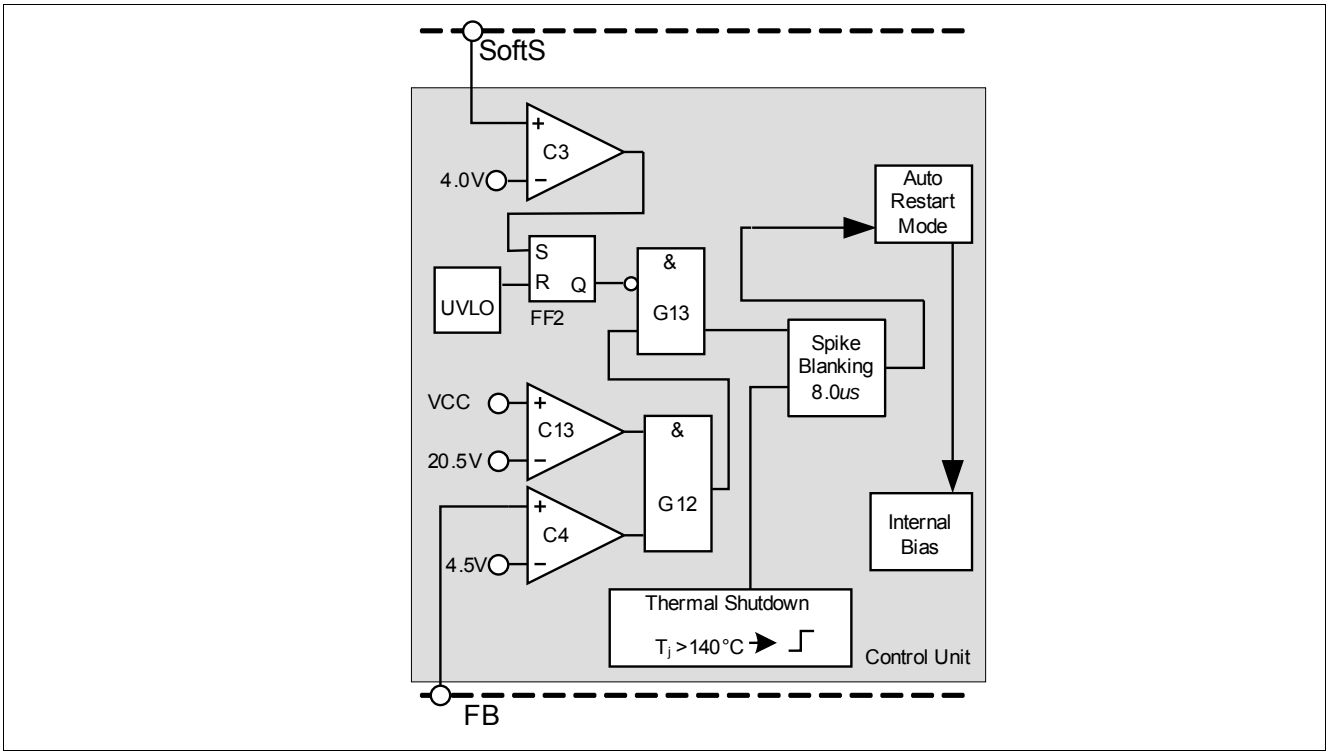


Figure 16 Auto Restart mode during startup

In order to ensure system reliability and prevent any false activation, a blanking time is implemented before the IC can enter Auto Restart mode during startup. The output of the VCC overvoltage detection circuit is fed into a spike blanking with a time constant of 8.0 μs.

The other fault detection function which can result in the Auto Restart mode during startup and has the 8.0 μs blanking time is for overtemperature detection. This block checks for a junction temperature of higher than 140 °C for malfunctioning operation.

Once Auto Restart mode is entered, the internal bias is switched off in order to reduce the current consumption of the IC as much as possible. In this mode, the average current consumption is only 300 μA as the only working blocks are the reference block and the Undervoltage Lockout (UVLO), which controls the startup cell by switching on/off at V_{VCCon}/V_{VCCoff}.

As there is no longer a self supply provided by the auxiliary winding, VCC starts to drop. The UVLO switches on the integrated startup cell when VCC falls below 10.3 V. It continues to charge VCC up to 18 V, at which point it is switched off again and the IC enters the startup phase.

Once all fault conditions have been removed, the IC automatically powers up as usual with a switching cycle at the GATE output after the soft start period has elapsed – hence the name Auto Restart mode.

3.6.2.2 Auto Restart Mode during RUN Mode

In the case of overload or open loop, the FB voltage exceeds 4.5 V, which is observed by C4. At this time, the external soft start capacitor can then be further charged by the integrated pull-up resistor R_{SoftS} via the switch S3 (see **Figure 15**). If V_{SoftS} exceeds 4.0 V, which is observed by C3, Auto Restart mode during RUN mode is activated as both inputs of the gate G5 are high.

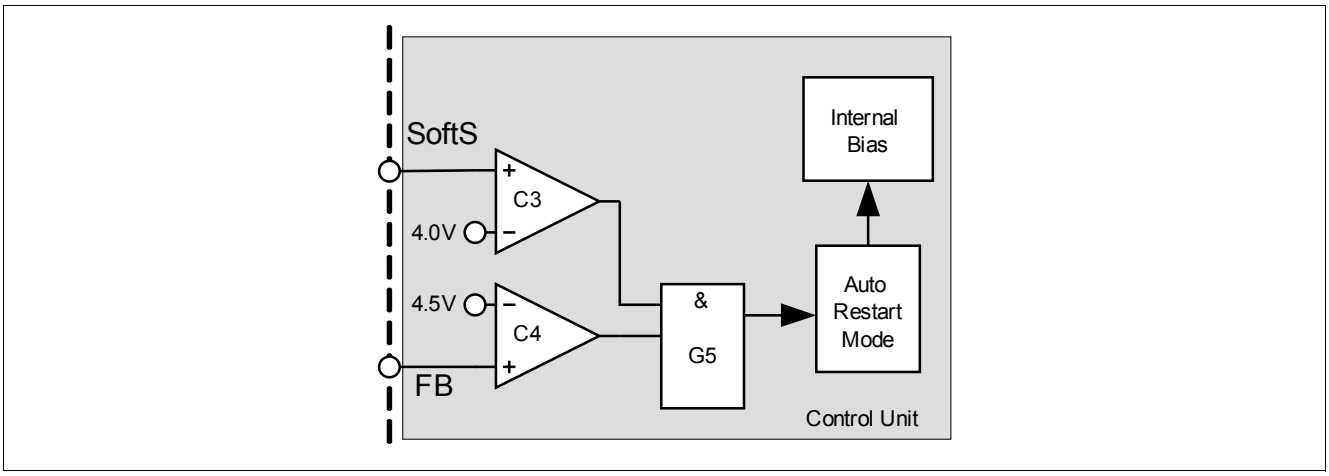


Figure 17 Auto Restart mode during RUN mode

This charging of the soft start capacitor from 3.2 V ~ 3.6 V to 4.0 V defines a blanking window, which prevents the system from entering Auto Restart mode during RUN mode unintentionally during large load jumps. In this event, FB will rise close to 5.0 V for a short duration before the loop regulates FB to less than 4.5 V.

In the case of VCC undervoltage – i.e., VCC falls below 10.3 V, the IC is turned off with the startup cell charging VCC as described earlier in this section. Once VCC is charged to above 18 V, the IC starts a new startup cycle.

This blanking time window for the Floating Load Protection mode can be forced via the external C_{SoftS} capacitor.

3.6.2.3 Floating Load Protection (FLP)

The circuit starts up as usual, but a missing load leads to a rise in the output and auxiliary voltages.

Reaching the VCC threshold of 24.5 V (voltage divider RD2/R4 and Q2) leads to a reduction in the feedback voltage and hence to reduced output current pulses in order to keep the output voltage below the maximum rating of the components. If the feedback level falls below 1.35 V, the Soft Start voltage begins to rise up to a threshold of 4 V (depends on the C4 value) and the IC is switched into the FLP mode.

4 Electrical Characteristics

All voltages are measured in respect to ground (GND, pin 8). The voltage levels are valid if other ratings are not violated.

4.1 Absolute Maximum Ratings

Absolute maximum ratings are defined as ratings, which when exceeded may lead to destruction of the integrated circuit. For the same reason, ensure that any capacitor to be connected to pin 7 (VCC) is discharged before assembling the application circuit.

Parameter	Controller	Symbol	Limit Values		Unit	Remarks
			min.	max.		
Drain/source voltage	ICLS602xX	V_{DS}	–	650	V	T_j = 110°C
Pulse drain current, t_p limited by max. T_j = 150 °C	ICLS6021J	I_{D_Puls1}	–	1.6	A	
	ICLS6022J	I_{D_Puls2}	–	2.3	A	
	ICLS6022G	I_{D_Puls3}	–	2.3	A	
	ICLS6023J	I_{D_Puls4}	–	6.1	A	
Avalanche energy, repetitive t_{AR} limited by max. T_j = 150 °C[1)]	ICLS6021J	E_{AR1}	–	0.005	mJ	
	ICLS6022J	E_{AR2}	–	0.01	mJ	
	ICLS6022G	E_{AR3}	–	0.01	mJ	
	ICLS6023J	E_{AR4}	–	0.15	mJ	
Avalanche current, repetitive t_{AR} limited by max. T_j=150 °C[1)]	ICLS6021J	I_{AR1}	–	0.3	A	
	ICLS6022J	I_{AR2}	–	0.5	A	
	ICLS6022G	I_{AR3}	–	0.5	A	
	ICLS6023J	I_{AR4}	–	1.5	A	
VCC supply voltage	ICLS602xX	V_{VCC}	-0.3	27	V	
FB voltage	ICLS602xX	V_{FB}	-0.3	5.0	V	
SoftS voltage	ICLS602xX	V_{SoftS}	-0.3	5.0	V	
CS voltage	ICLS602xX	V_{CS}	-0.3	5.0	V	
Junction temperature	ICLS602xX	T_j	-40	150	°C	Controllers & CoolMOS™
Storage temperature	ICLS602xX	T_S	-55	150	°C	
Thermal resistance – junction ambient	ICLS602xX	R_{thJA}	–	90	K/W	PG-DIP-8-6
			–	110	K/W	PG-DSO-16/12
ESD capability	ICLS602xX	V_{ESD}	–	2	kV	Human body model[2)]

1) Repetetive avalanche causes additional power losses that can be calculated as $P_{AV} = E_{AR} * f$

2) According to EIA/JESD22-A114-B (discharging a 100 pF capacitor through a 1.5 kΩ series resistor)

4.2 Operating Range

The IC operates as described in the functional description once the values listed here lie within the operating range.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
VCC supply voltage	V_{VCC}	V_{VCCoff}	26	V	
Junction temperature of controller	T_{jCon}	–25	130	°C	Max. value limited due to integrated thermal shutdown
Junction temperature of CoolMOS™	$T_{JCoolMOS}$	–25	150	°C	

4.3 Characteristics

4.3.1 Supply Section

The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and junction temperature range T_J from –25 °C to 130 °C. Typical values represent the median values, which are related to 25 °C. Unless otherwise stated, a supply voltage of VCC = 18 V is assumed.

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Startup current	$I_{VCCstart}$	–	300	450	µA	V_{VCC} = 17 V
VCC charge current	$I_{VCCcharge1}$			5.0	mA	V_{VCC} = 0 V
	$I_{VCCcharge2}$	0.55	1.05	1.60	mA	V_{VCC} = 1 V
	$I_{VCCcharge3}$	–	0.88	–	mA	V_{VCC} = 17 V
Leakage current of the startup cell & CoolMOS™	$I_{StartLeak}$	–	0.2	50	µA	V_{Drain}= 450 V at T_j = 100 °C
Supply current with inactive gate	$I_{VCCsup1}$	–	1.7	2.5	mA	Soft Start pin is open
Supply current with active gate	$I_{VCCsup3}$	–	2.5	3.6	mA	V_{SoftS} = 3.0 V I_{FB} = 0
Supply current in Auto Restart mode with inactive gate	$I_{VCCrestart}$	–	300	–	µA	I_{FB} = 0 I_{SoftS} = 0
Supply current in Floating Load Protection (FLP) mode with inactive gate	$I_{VCCFLP1}$	–	500	950	µA	V_{FB} = 2.5 V I_{SoftS} = 3.0 V
	$I_{VCCFLP2}$	–	500	950	µA	V_{CC} = 11.5 V V_{FB} = 2.5 V I_{SoftS} = 3.0 V
VCC turn-on threshold VCC Turn-off threshold VCC Turn-on/off hysteresis	V_{VCCon} V_{VCCoff} V_{VCChys}	17.0 9.6 –	18.0 10.3 7.7	19.0 11.0 –	V V V	

4.3.2 Internal Voltage Reference

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Trimmed reference voltage	V_{REF}	4.90	5.00	5.10	V	measured at pin FB I_{FB} = 0

4.3.3 PWM Section

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Fixed oscillator frequency	f_{OSC3}	58	67	76	kHz	
	f_{OSC4}	62	67	74.5	kHz	T_j = 25 °C
Frequency jittering range	fdelta	–	±2.7	–	kHz	T_j = 25 °C
Max. duty cycle	D_{max}	0.70	0.75	0.80		
Min. duty cycle	D_{min}	0	–	–		V_{FB} < 0.3 V
PWM OP gain	A_V	3.0	3.2	3.4		
Max. level of voltage ramp	$V_{Max-Ramp}$	–	0.6	–	V	
V_{FB} operating range, min. level	V_{FBmin}	–	0.5	–	V	
V_{FB} operating range, max. level	V_{FBmax}	–	–	4.3	V	CS=1V limited by comparator C4[1)]
Feedback pull-up resistor	R_{FB}	9	14	22	kΩ	
Soft start pull-up resistor	R_{SoftS}	30	45	62	kΩ	

1) This parameter is not subject to production testing and is verified by design/characterization

4.3.4 Control Unit

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Deactivation level for SoftS comparator C7 by C2	$V_{SoftSC2}$	2.98	3.10	3.22	V	V_{FB} = 5 V
Clamped V_{SoftS} voltage during Floating Load Protection (FLP) mode	$V_{SoftSclmp\_FLP}$	2.88	3.0	3.12	V	
Activation limit of comparator C3	$V_{SoftSC3}$	3.85	4.00	4.15	V	V_{FB} = 5 V
SoftS startup current	$I_{SoftSstart}$	–	0.9	–	mA	V_{SoftS} = 0 V
Overload detection limit for comparator C4	V_{FBC4}	4.33	4.50	4.67	V	V_{SoftS} = 4.5 V
Floating Load Protection level for comparator C5	V_{FBC5}	1.23	1.35	1.43	V	V_{SoftS} = 4.5 V
Floating Load Protection level for comparator C6a	V_{FBC6a}	3.48	3.61	3.76	V	After Floating Load Protection mode is entered
Floating Load Protection level for comparator C6b	V_{FBC6b}	2.88	3.0	3.12	V	After Floating Load Protection mode is entered
Overvoltage detection limit	V_{VCCOVP}	19.5	20.5	21.5	V	V_{FB} = 5 V, V_{SoftS} = 3 V
Thermal shutdown[1)]	T_{jSD}	130	140	150	°C	
Spike blanking	t_{Spike}	–	8.0	–	µs	

1) The parameter is not subject to production testing and is verified by design/characterization

Note: The trend of all the voltage levels in the Control Unit is the same regarding the deviation except VVCCOVP.

4.3.5 Current Limiting

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Peak current limitation (incl. propagation delay time) (see **Figure 13**)	V_{csth}	1.01	1.06	1.11	V	dV_{sense} / dt = 0.6 V/µs (PG-DIP-8-6)
		1.02	1.07	1.12	V	dV_{sense} / dt = 0.6 V/µs (PG-DSO-16/12)
Peak current limitation during Floating Load Protection mode	V_{CS2}	0.27	0.32	0.37	V	
Leading edge blanking	t_{LEB}	–	220	–	ns	V_{SoftS} = 3.0 V
CS input bias current	ICSbias	–1.0	–0.2	0	µA	V_{CS} = 0 V

4.3.6 CoolMOS™ Section

Parameter	Controller	Symbol	Limit Values			Unit	Remarks
			min.	typ.	max.		
Drain/source breakdown voltage	ICLS602xX	$V_{(BR)DSS}$	600 650	– –	– –	V V	T_j = 25 °C T_j = 110 °C
Drain/source on resistance	ICLS6021J	R_{DSon1}	– –	6.45 13.70	7.50 17.00	Ω Ω	T_j = 25 °C T_j = 125 °C[1)] at I_D = 0.3 A
	ICLS6022J ICLS6022G	R_{DSon2}	– –	4.70 10.00	5.44 12.50	Ω Ω	T_j = 25 °C T_j = 125 °C[1)] at I_D = 0.5 A
	ICLS6023J	R_{DSon3}	– –	1.70 3.57	1.96 4.12	Ω Ω	T_j = 25 °C T_j = 125 °C[1)] at I_D = 1.5 A
Effective output capacitance, energy-related	ICLS6021J	$C_{o(er)1}$	–	3.65	–	pF	V_{DS} = 0 V to 480 V
	ICLS6022J	$C_{o(er)2}$	–	4.75	–	pF	
	ICLS6022G	$C_{o(er)3}$	–	4.75	–	pF	
	ICLS6023J	$C_{o(er)4}$	–	11.63	–	pF	
Rise time	ICLS602xX	t_{rise}	–	30[2)]	–	ns	
Fall time	ICLS602xX	t_{fall}	–	30[2)]	–	ns	

1) The parameter is not subject to production testing and is verified by design/characterization
2) Measured in a typical flyback converter application

5 Temperature Derating Curves

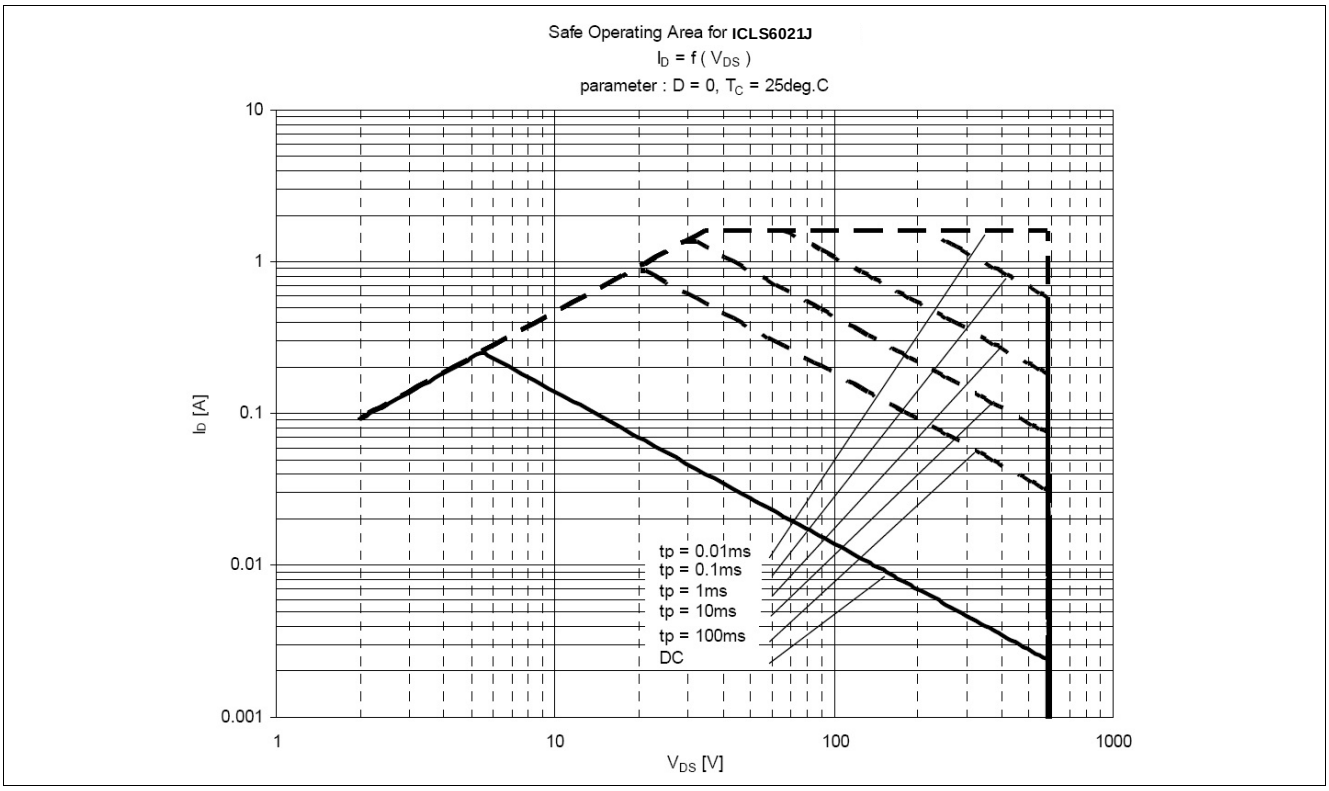


Figure 18 Safe Operating Area (SOA) curve for ICLS6021J

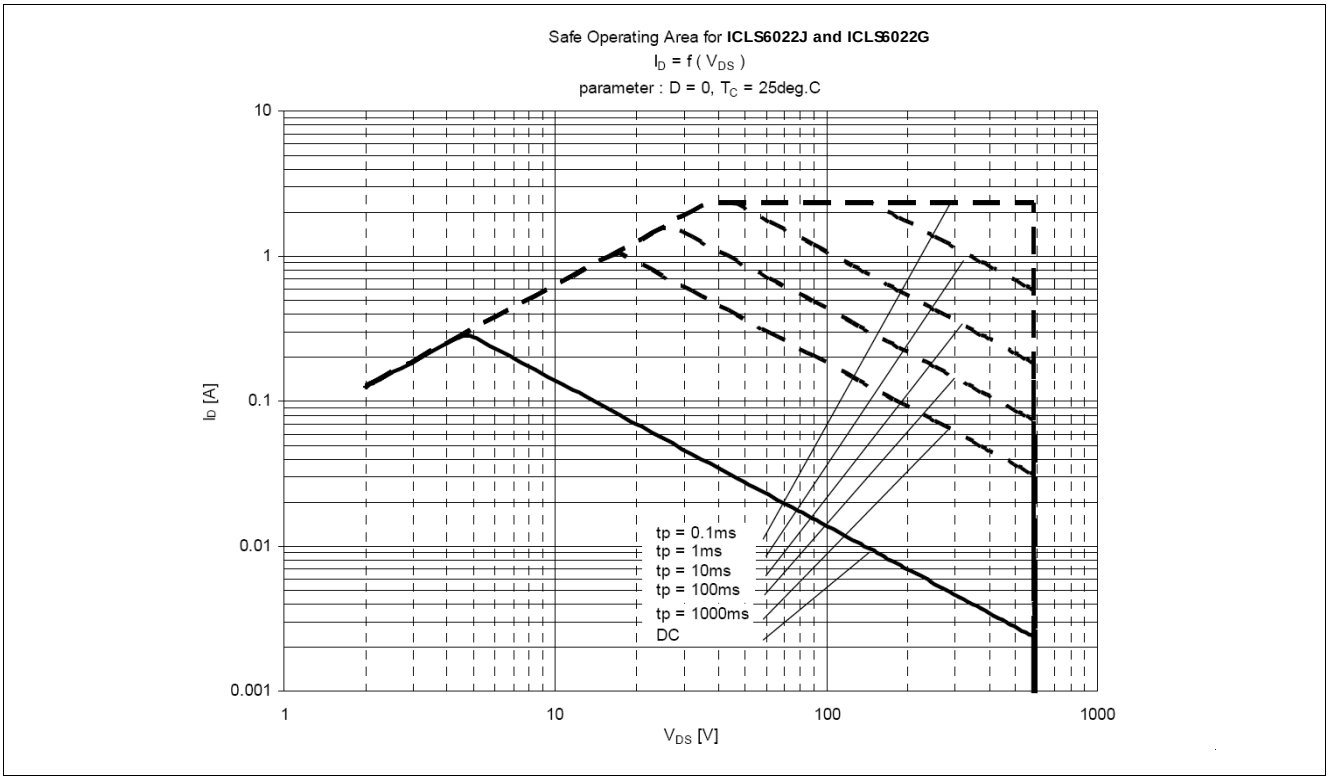


Figure 19 Safe Operating Area (SOA) curve for ICLS6022J and ICLS6022G

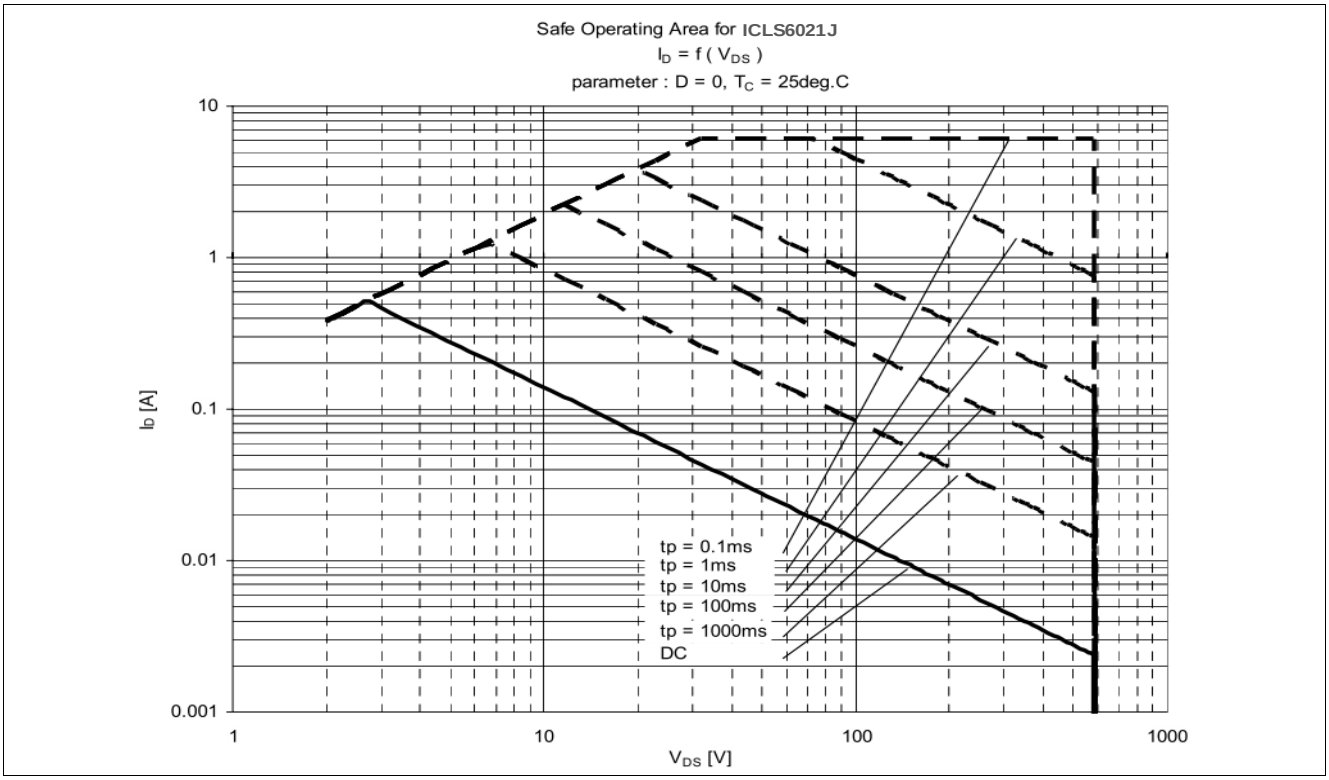


Figure 20 Safe Operating Area (SOA) curve for ICLS6023J

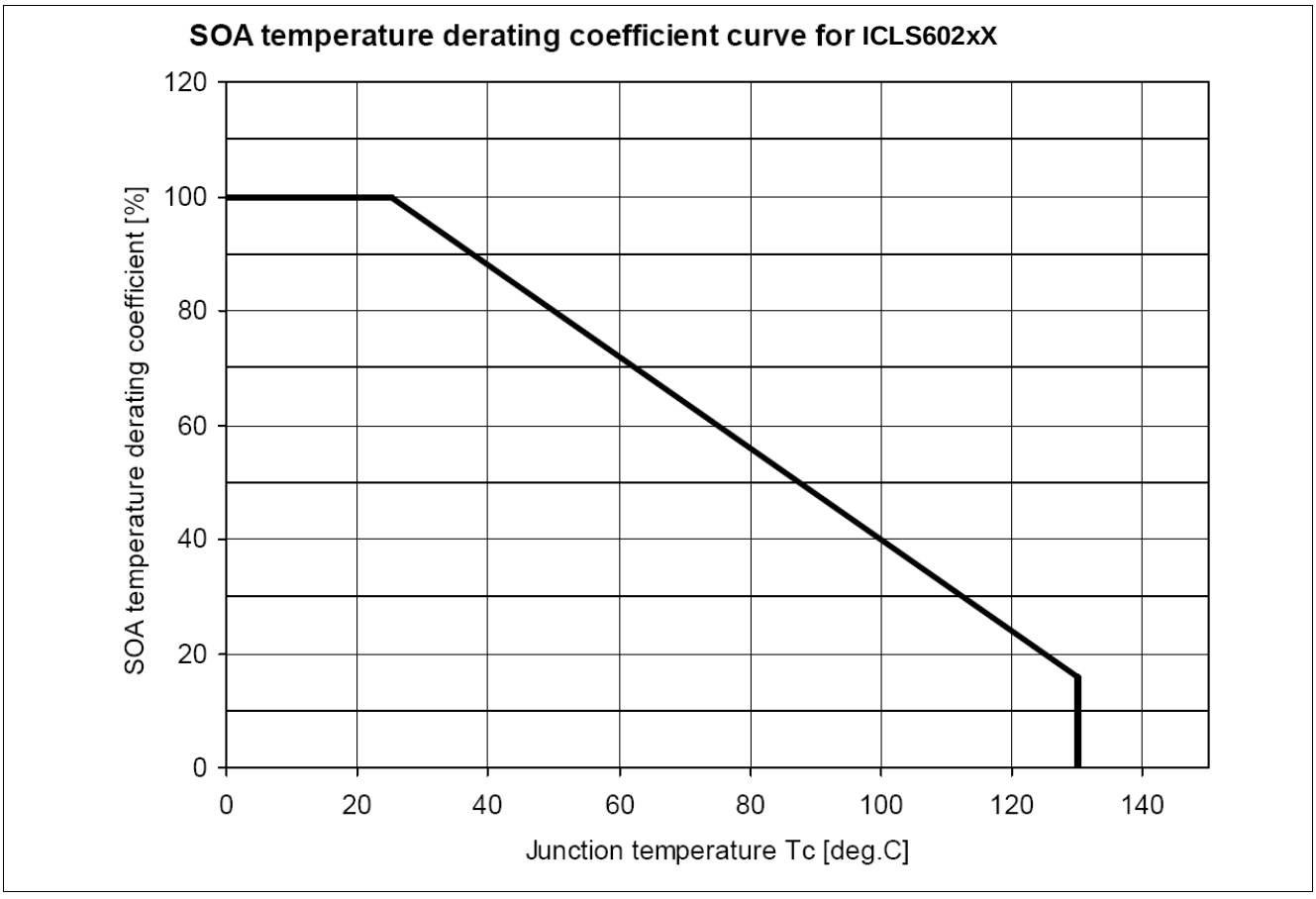
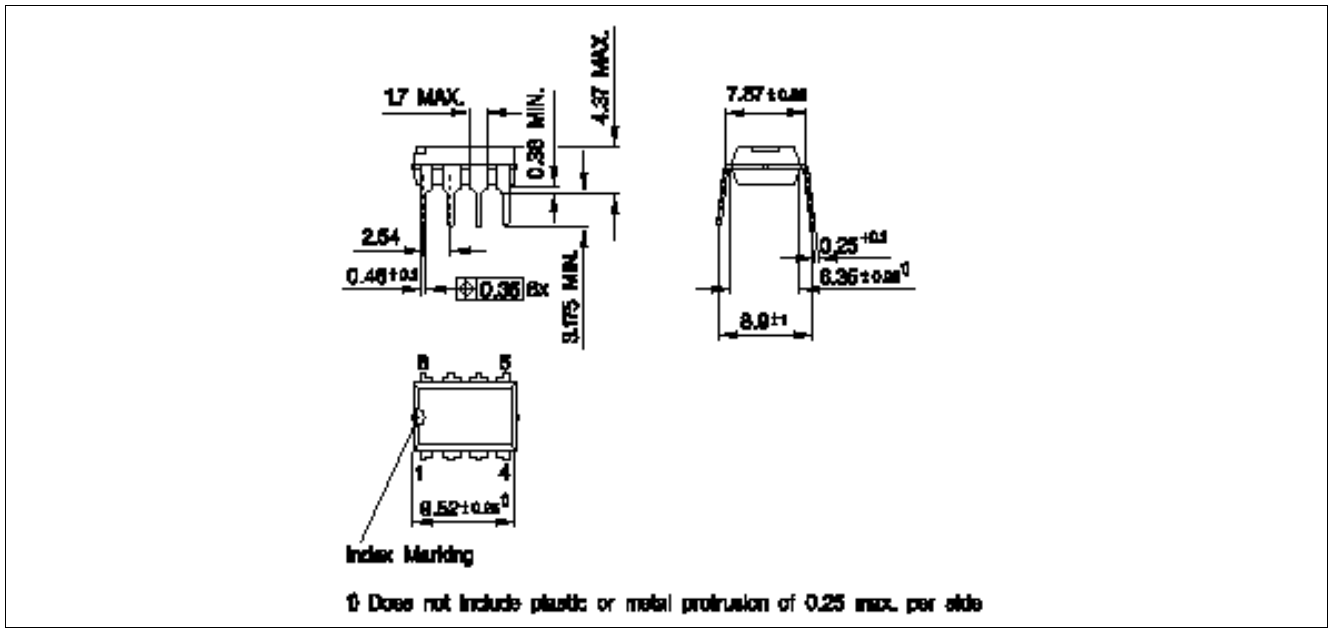


Figure 21 SOA temperature derating coefficient curve

6 Outline Dimensions

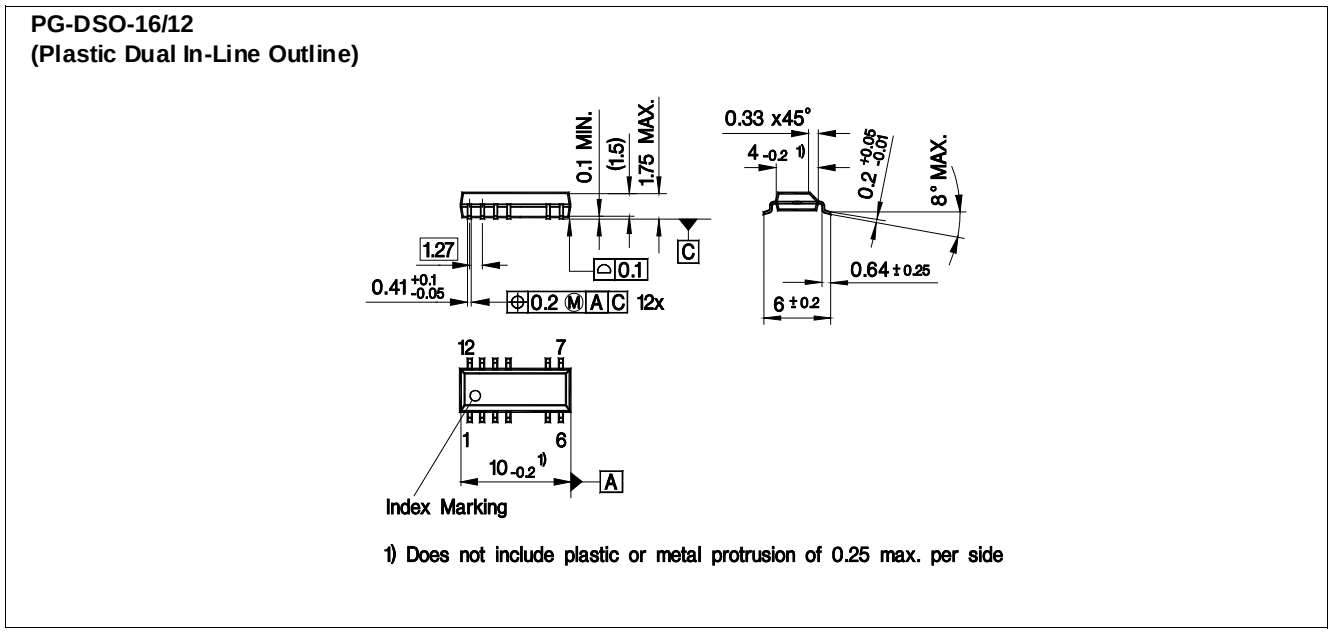
6.1 Outline Dimensions of PG-DIP-8-6



1) Does not include plastic or metal protrusion of 0.25 max. per side

Figure 22 PG-DIP-8-6 (Pb-free lead plating plastic dual inline outline)

6.2 Outline Dimensions of PG-DSO-16/12



1) Does not include plastic or metal protrusion of 0.25 max. per side

Figure 23 PG-DSO-16/12 (plastic dual inline)

7 Marking

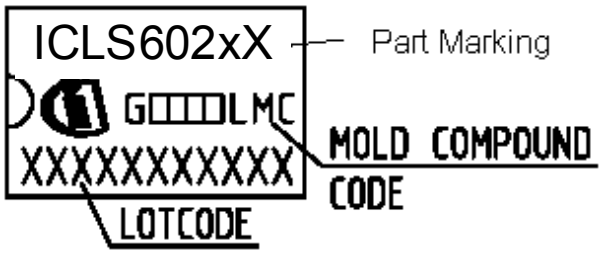


Figure 24 Marking for ICLS6x Series controllers

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