

TC74LVX273F, TC74LVX273FW, TC74LVX273FT

Octal D-Type Flip-Flop with Clear

The TC74LVX273F/ FW/ FT is a high-speed CMOS octal D-flip flop fabricated with silicon gate CMOS technology. Designed for use in 3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

This device is suitable for low-voltage and battery operated systems.

Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse. When the $\overline{\text{CLR}}$ input is held low, the Q outputs are in the low logic level independent of the other inputs.

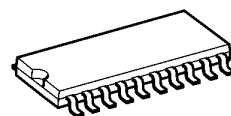
An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

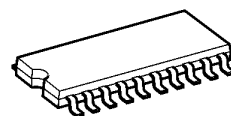
- High-speed: $f_{\text{max}} = 150 \text{ MHz}$ (typ.) ($V_{\text{CC}} = 3 \text{ V}$)
- Low power dissipation: $I_{\text{CC}} = 4 \mu\text{A}$ (max) ($T_a = 25^\circ\text{C}$)
- Input voltage level: $V_{\text{IL}} = 0.8 \text{ V}$ (max) ($V_{\text{CC}} = 3 \text{ V}$)
 $V_{\text{IH}} = 2.0 \text{ V}$ (min) ($V_{\text{CC}} = 3 \text{ V}$)
- Power-down protection provided on all inputs
- Balanced propagation delays: $t_{\text{PLH}} \approx t_{\text{PHL}}$
- Low noise: $V_{\text{OLP}} = 0.8 \text{ V}$ (max)
- Pin and function compatible with 74HC273

Note: xxxFW (JEDEC SOP) is not available in Japan.

TC74LVX273F

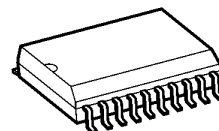


SOP20-P-300-1.27A



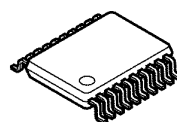
SOP20-P-300-1.27

TC74LVX273FW



SOL20-P-300-1.27

TC74LVX273FT

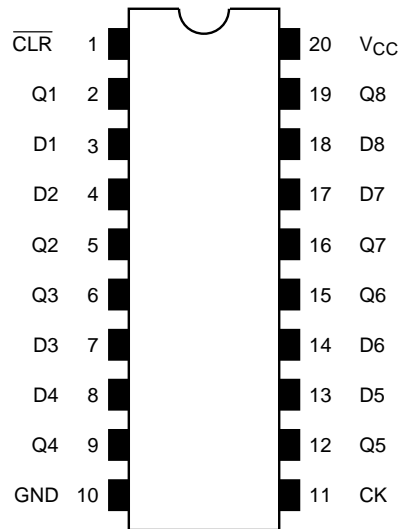


TSSOP20-P-0044-0.65A

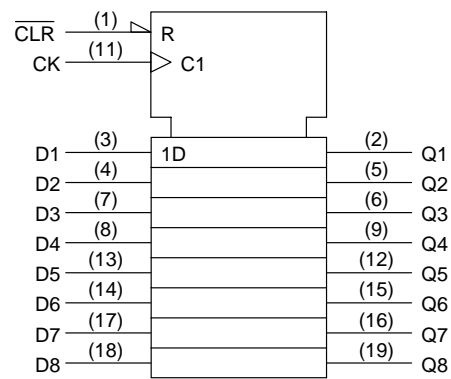
Weight

SOP20-P-300-1.27A	: 0.22 g (typ.)
SOP20-P-300-1.27	: 0.22 g (typ.)
SOL20-P-300-1.27	: 0.46 g (typ.)
TSSOP20-P-0044-0.65A	: 0.08 g (typ.)

Pin Assignment (top view)



IEC Logic Symbol

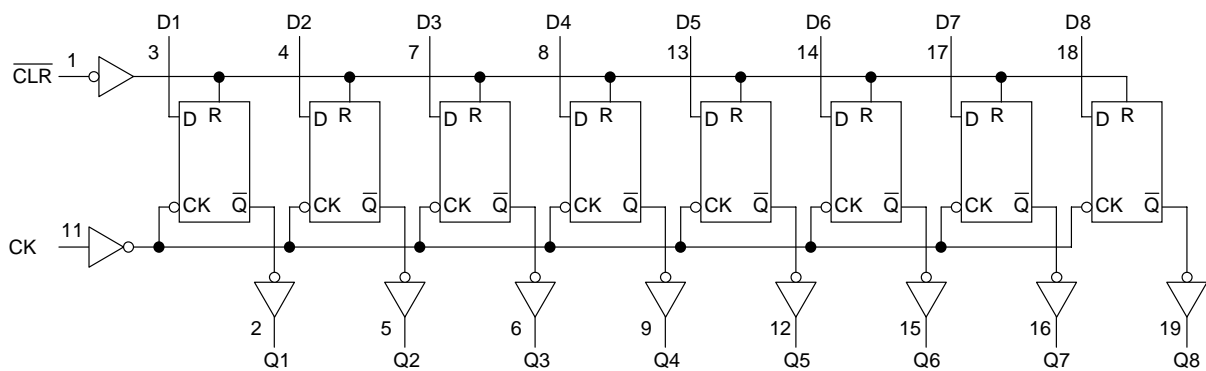


Truth Table

Inputs			Outputs	Function
CLR	D	CK	Q	
L	X	X	L	Clear
H	L		L	—
H	H		H	—
H	X		Qn	No change

X: Don't care

System Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to 7.0	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 75	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Recommended Operating Conditions (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 3.6	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100	ns/V

Note: The recommended operating conditions are required to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics		Sym- bol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit	
					V _{CC} (V)	Min	Typ.	Max	Min		Max
Input voltage	H-level	V _{IH}	—		2.0	1.5	—	—	1.5	—	V
					3.0	2.0	—	—	2.0	—	
					3.6	2.4	—	—	2.4	—	
	L-level	V _{IL}	—		2.0	—	—	0.5	—	0.5	
					3.0	—	—	0.8	—	0.8	
					3.6	—	—	0.8	—	0.8	
Output voltage	H-level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = −50 μA	2.0	1.9	2.0	—	1.9	—	V
				I _{OH} = −50 μA	3.0	2.9	3.0	—	2.9	—	
				I _{OH} = −4 mA	3.0	2.58	—	—	2.48	—	
	L-level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	2.0	—	0	0.1	—	0.1	
				I _{OL} = 50 μA	3.0	—	0	0.1	—	0.1	
				I _{OL} = 4 mA	3.0	—	—	0.36	—	0.44	
Input leakage current		I _{IN}	V _{IN} = 5.5 V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND		3.6	—	—	4.0	—	40.0	μA

Timing Requirements (input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C	Ta = -40 to 85°C	Unit
				V _{CC} (V)	Limit	
Minimum pulse width (CK)	t _W (L)	—		2.7	8.0	ns
	t _W (H)			3.3 ± 0.3	5.5	
Minimum pulse width ($\overline{\text{CLR}}$)	t _W (L)	—		2.7	7.5	ns
				3.3 ± 0.3	5.0	
Minimum set-up time	t _s	—		2.7	8.0	ns
				3.3 ± 0.3	5.5	
Minimum hold time	t _h	—		2.7	1.0	ns
				3.3 ± 0.3	1.0	
Minimum removal time ($\overline{\text{CLR}}$)	t _{rem}	—		2.7	4.0	ns
				3.3 ± 0.3	2.5	

AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit
		VCC (V)	CL (pF)		Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q)	t _{pLH}	—	2.7	15	—	9.0	16.9	1.0	20.5	ns
				50	—	11.5	20.4	1.0	24.0	
	t _{pHL}		3.3 ± 0.3	15	—	7.1	11.0	1.0	13.0	
				50	—	9.6	14.5	1.0	16.5	
Propagation delay time ($\overline{\text{CLR}}$ -Q)	t _{pHL}	—	2.7	15	—	9.3	17.6	1.0	20.5	ns
				50	—	11.8	21.1	1.0	24.0	
			3.3 ± 0.3	15	—	7.3	11.5	1.0	13.5	
				50	—	9.8	15.0	1.0	17.0	
Maximum clock frequency	f _{max}	—	2.7	15	55	110	—	45	—	MHz
				50	45	60	—	40	—	
			3.3 ± 0.3	15	95	150	—	80	—	
				50	60	90	—	50	—	
Output to output skew	t _{osLH}	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
	t _{osHL}		3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input capacitance	C _{IN}	(Note 2)			—	4	10	—	10	pF
Power dissipation capacitance	C _{PD}	(Note 3)			—	31	—	—	—	pF

Note 1: Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

Note 2: Parameter guaranteed by design.

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per F/F)}$$

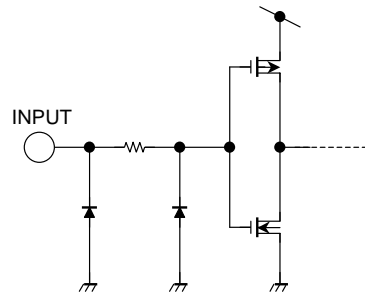
And the total C_{PD} when n pcs. of F/F operate can be gained by the following equation:

$$C_{PD}(\text{total}) = 22 + 9 \cdot n$$

Noise Characteristics (Ta = 25°C, input: $t_r = t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Typ.	Limit	Unit
Quiet output maximum dynamic V _{OL}	V _{OLP}	—	3.3	0.5	0.8	V
Quiet output minimum dynamic V _{OL}	V _{OLV}	—	3.3	−0.5	−0.8	V
Minimum high level dynamic input voltage V _{IH}	V _{IHD}	—	3.3	—	2.0	V
Maximum low level dynamic input voltage V _{IL}	V _{ILD}	—	3.3	—	0.8	V

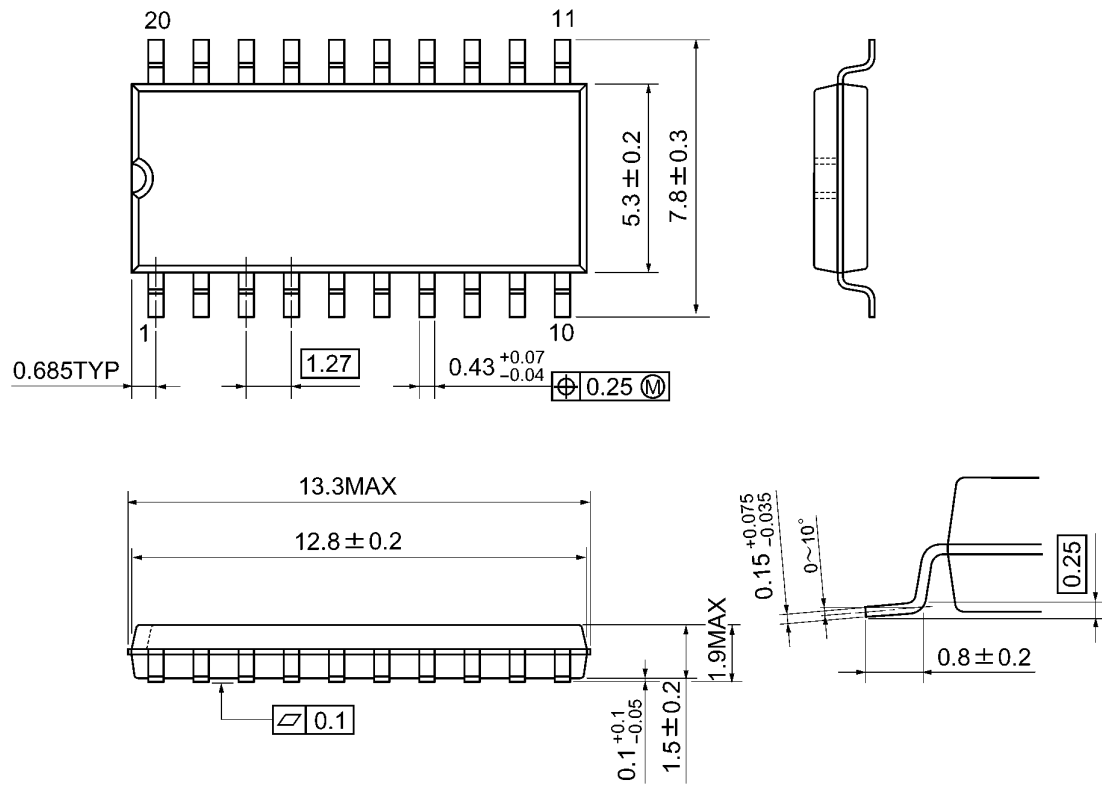
Input Equivalent Circuit



Package Dimensions

SOP20-P-300-1.27A

Unit: mm

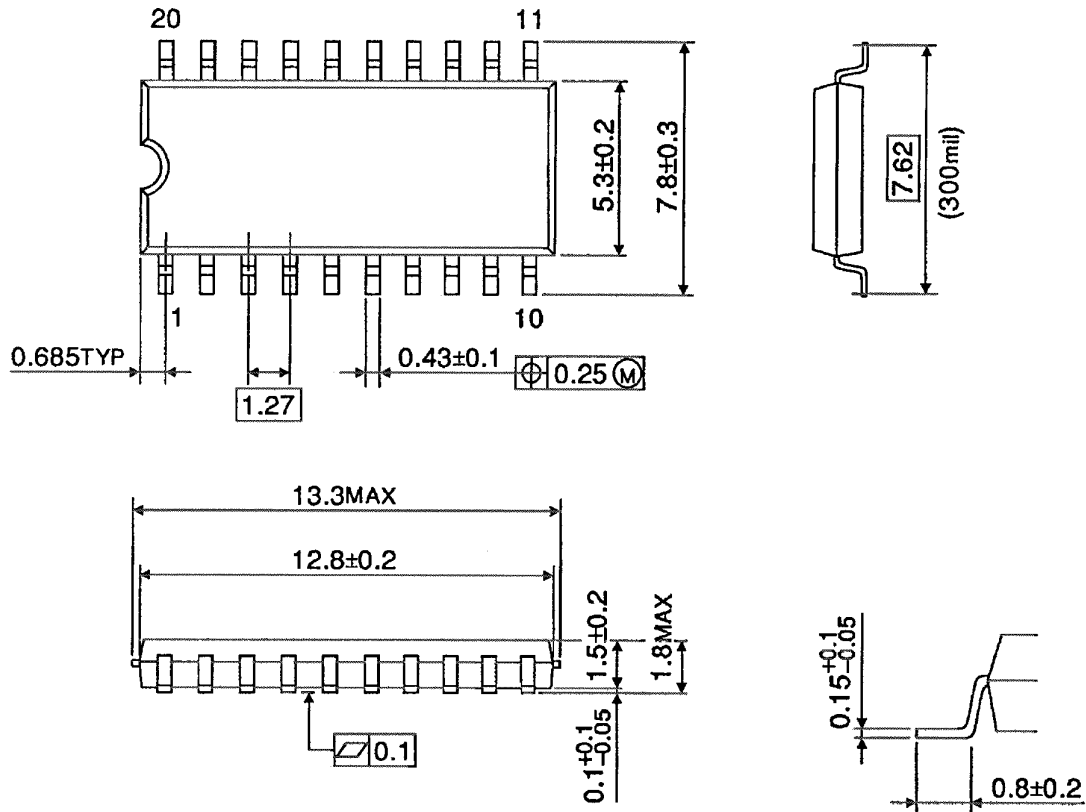


Weight: 0.22 g (typ.)

Package Dimensions

SOP20-P-300-1.27

Unit : mm

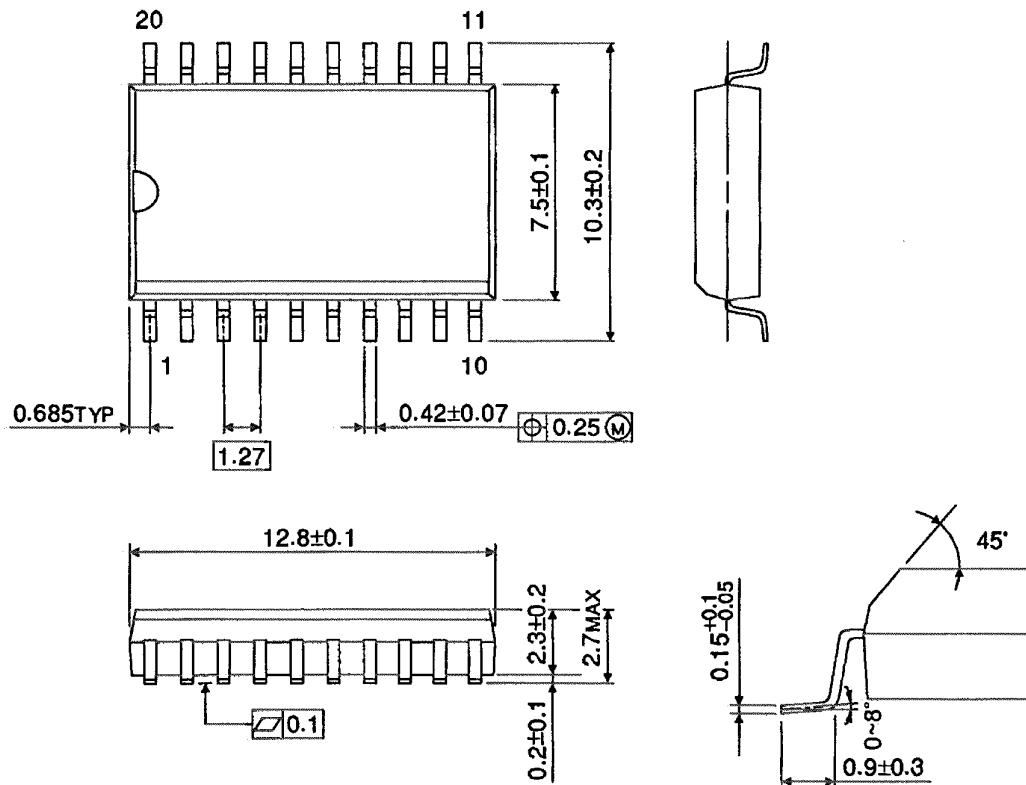


Weight: 0.22 g (typ.)

Package Dimensions (Note)

SOL20-P-300-1.27

Unit : mm



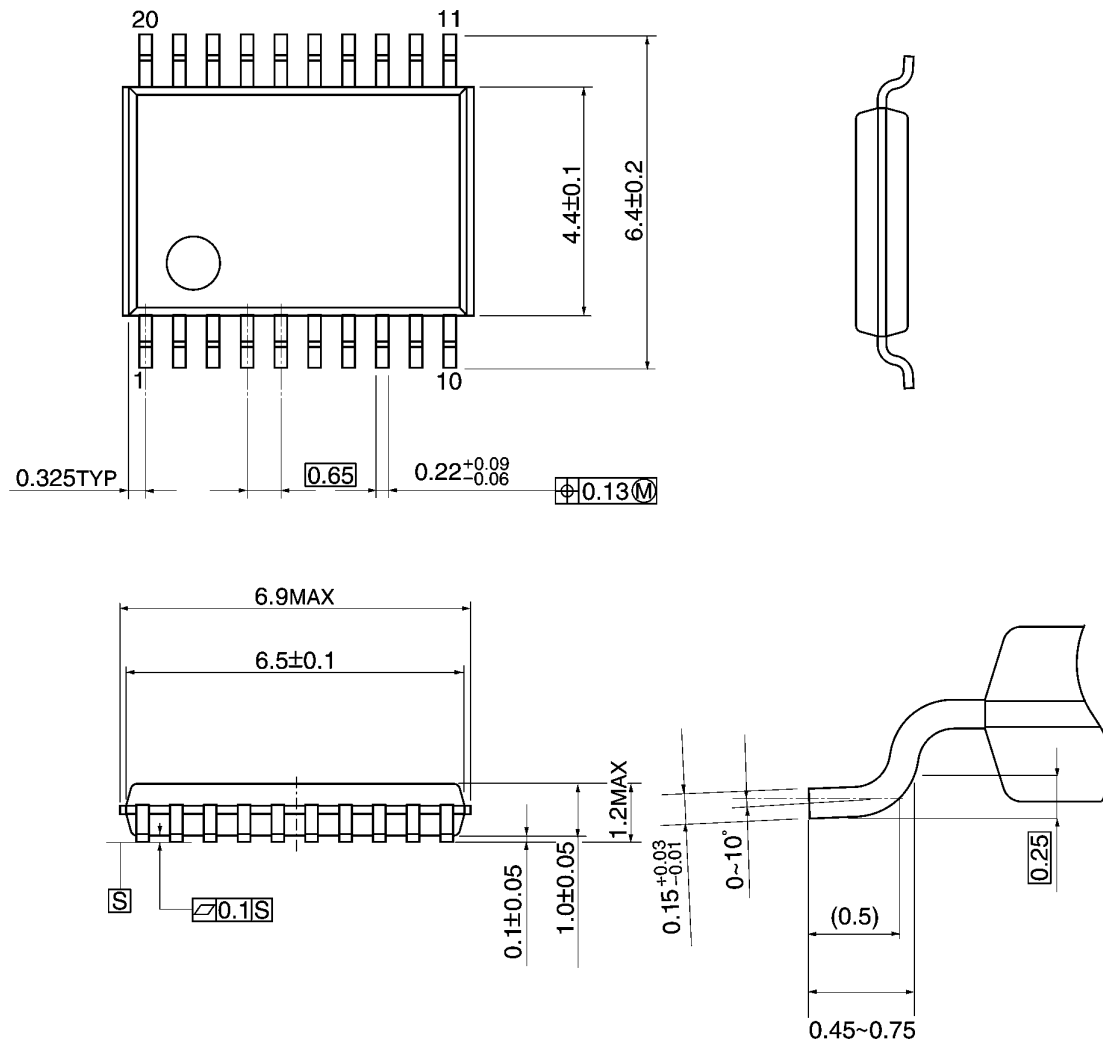
Note: This package is not available in Japan.

Weight: 0.46 g (typ.)

Package Dimensions

TSSOP20-P-0044-0.65A

Unit: mm



Weight: 0.08 g (typ.)

Note: Lead (Pb)-Free Packages

SOP20-P-300-1.27A TSSOP20-P-0044-0.65A

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