

# **PIN Diode Shunt Switch Element**

Rev. V2

#### **Features**

- Supports up to 40 W Power
- Low Insertion Loss:
  0.2 dB to 2.7 GHz
  0.4 dB to 10.0 GHz
- High Isolation:
  30 dB to 10.0 GHz
- RoHS\* Compliant

# **Description**

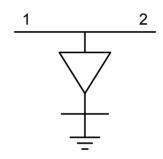
A broadband, high linearity, medium power shunt switch element in a 1.9 x 1.1 mm DFN package.

This device is designed for wireless telecommunications infrastructure and test instrument applications. It is also suited for other applications in  $0.05 \sim 10$  GHz.



2012

#### Pin Out / Schematic



# **Ordering Information**

Part Number	Package
MSWSHB-020-30	3000 piece reel

# Electrical Specifications: T<sub>A</sub> = +25°C

Parameter	Test Conditions	Units	Min.	Тур.	Max.
Breakdown Voltage (V <sub>B</sub> )	Ι <sub>R</sub> = 10 μΑ	V	200	_	_
Insertion Loss (I <sub>L</sub> )	V <sub>R</sub> = 10 V <2.7 GH <10.0 GHz	dB	_	0.08 0.40	0.2 0.5
Isolation (I <sub>SO</sub> )	I <sub>F</sub> = 20 mA <2.7 GH <10.0 GHz	dB	33 28	40 32	_
Input / Output Return Loss	V <sub>R</sub> = 10 V <2.7 GH <10.0 GHz	dB	25 15	28 20	_
Minority Carrier Lifetime (T <sub>L</sub> )	I <sub>F</sub> = 10 mA, I <sub>R</sub> = 6 mA, @ 50%	ns	_	4000	_

<sup>\*</sup> Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.



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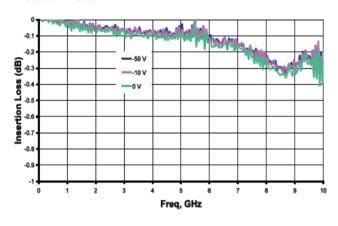
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# **Absolute Maximum Ratings**

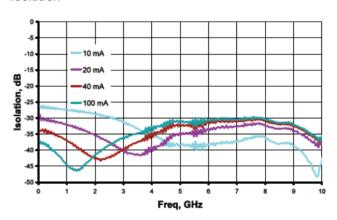
Parameter	Absolute Maximum		
Breakdown Voltage	200 V		
Forward Current	200 mA		
Thermal Resistance	15°C/W		
Junction Temperature	+175°C		
Storage Temperature	-65°C to +150°C		
Assembly Temperature	+260°C Per JEDEC STD-J-20C		

# **Typical Performance Curves**

#### Insertion Loss



#### Isolation



#### Input Return Loss

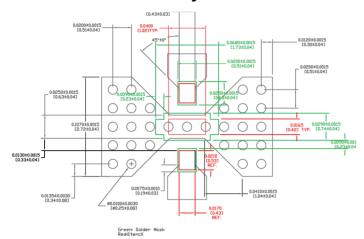




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## **Printed Circuit Board Layout**

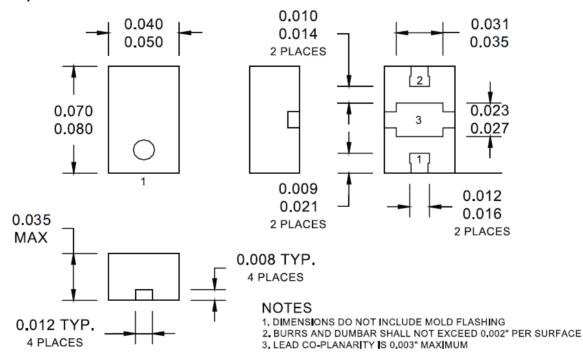


NOTE: If possible, use copper filled vias underneath pin 3 for better thermals; otherwise, use vias that are plated through, filled and plated over.

Solder mask should provide a 60 um clearance between copper pad and soldermask. Rounded pkg pads should have matching rounded solder mask openings.

Use circles or squares for the thermal land stencil such that only get 50% to 80% solder paste coverage.

# **Outline (2012)**



# MSWSHB-020-30



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