DATA SHEET

74LVC377

Octal D-type flip-flop with data enable; positive-edge trigger

Product specification
Supersedes data of 1996 Jun 06
IC24 Data Handbook

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Philips
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74LVC377

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Conforms to JEDEC standard 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74LVC377 is a low-voltage Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC377 has eight edge-triggered , D-type flip-flops with individual D inputs and Q outputs. A common clock (CP) input loads all flip-flops simultaneously when the data enable $\overline{E}$ is LOW. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop. The $\overline{E}$ input must be stable only one set-up time prior to the LOW-to-HIGH transition for predictable operation.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Qn;	C_L = 50pF V_{CC} = 3.3V	6.0	ns
f_{max}	Maximum clock frequency		230	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	V_I = GND to V_{CC}[1]	22	pF

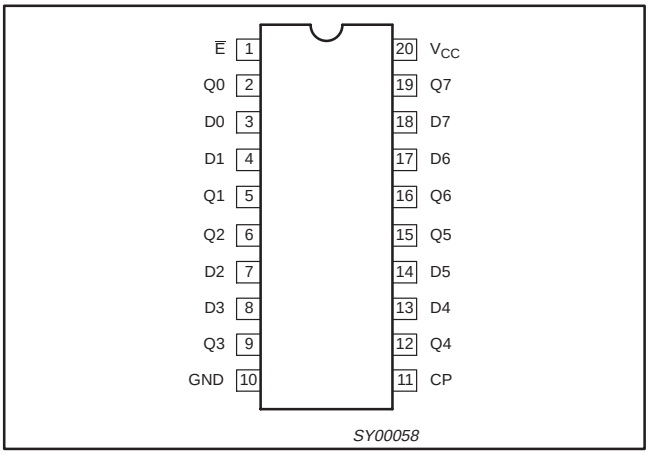
NOTES:

1 C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; C_L = output load capacity in pF;
f_o = output frequency in MHz; V_{CC} = supply voltage in V;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SO	–40°C to +85°C	74LVC377 D	74LVC377 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC377 DB	74LVC377 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC377 PW	74LVC377PW DH	SOT360-1

PIN CONFIGURATION

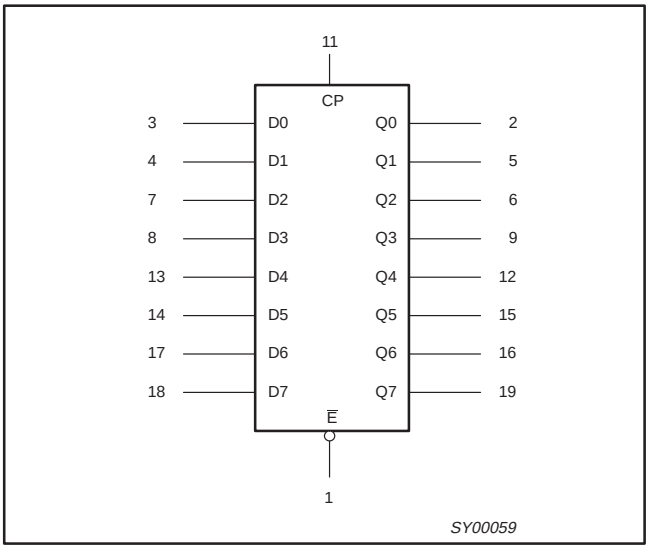


SY00058

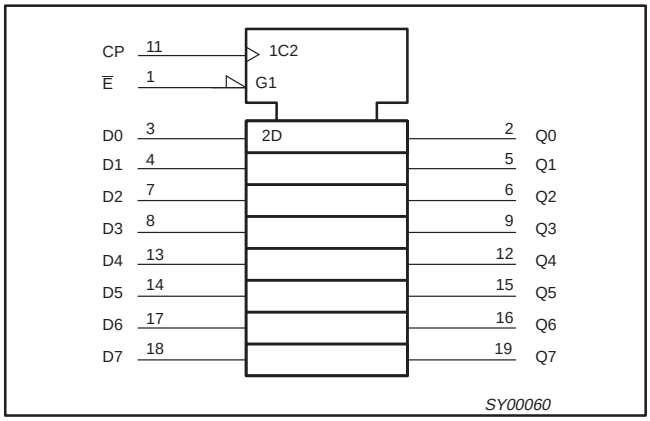
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{E}$	Data enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 – Q7	Flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 – D7	Data inputs
10	GND	Ground (0V)
11	CP	Clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	Positive power supply

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUT
	CP	$\overline{E}$	Dn	Q_n
Load '1'	↑	l	h	H
Load '0'	↑	l	l	L
hold (do nothing)	↑ X	h H	X X	no change no change

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
↑ = LOW-to-HIGH transition
X = Don't care

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC Input voltage range		0	5.5	V
$V_{I/O}$	DC Input voltage range for I/Os		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +5.5	V
$V_{I/O}$	DC input voltage range for I/Os		–0.5 to V_{CC} +0.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_{OUT}	DC output voltage	Note 2	–0.5 to V_{CC} +0.5	V
I_{OUT}	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–60 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V		V_{CC}			V
		V_{CC} = 2.7 to 3.6V		2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V				GND	V
		V_{CC} = 2.7 to 3.6V				0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA		V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA		V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or $V_{IL;}$ I_O = –12mA		V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or $V_{IL;}$ I_O = –24mA		V_{CC} – 1.0			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA				0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA				0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or $V_{IL;}$ I_O = 24mA				0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND	Not for I/O pins		±0.1	±5	µA
I_{IHZ}/I_{ILZ}	Input current for common I/O pins	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND			±0.1	±15	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND			0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0			0.1	10	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0			5	500	µA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

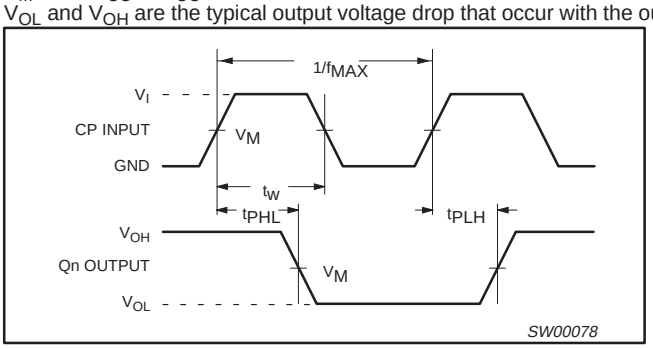
GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			
			MIN	TYP[1]	MAX	MIN	TYP	MAX	
t_{PHL} t_{PLH}	Propagation delay CP to Qn	1		6.0	10.2		6.6	11.2	ns
t_W	Clock pulse width HIGH or LOW	1	4	1.0		5	1.6		ns
t_{su}	Set-up time $\overline{E}$ to CP	2	4	2.3		5	2.9		ns
t_h	Hold time $\overline{E}$ to CP	2	0	–2.2		0	–2.8		ns
t_{su}	Set-up time D_n to CP	3	2	1.3		3	1.8		ns
t_h	Hold time D_n to CP	3	0	–1.2		0	–1.6		ns
f_{max}	Maximum clock pulse frequency	1	125			100			MHz

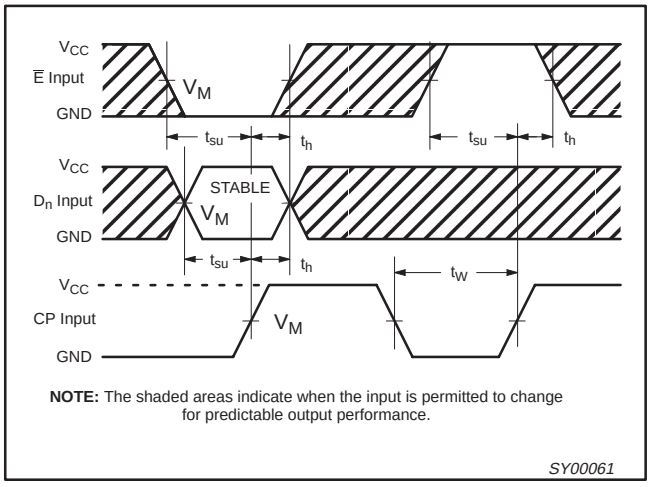
NOTE:
1. Unless otherwise stated, all typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V.
V_M = 0.5 V_{CC} at $V_{CC} <$ 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

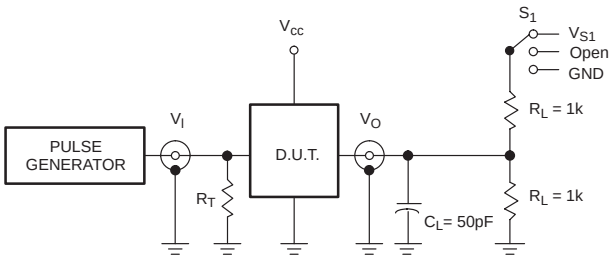


Waveform 1. Clock (CP) to output (Qn) propagation delays the clock pulse width and the maximum clock pulse frequency.

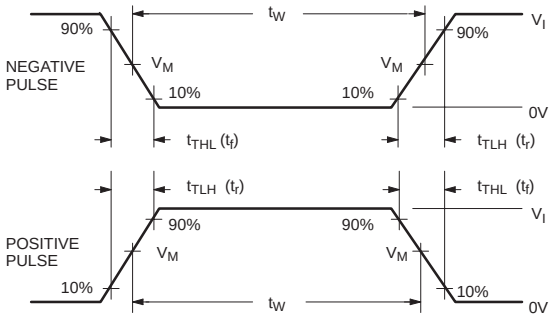


Waveform 2. Data set-up and hold times from the data input (Dn) and from the enable input ($\overline{E}$) to the clock (CP).

TEST CIRCUIT



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{S1}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I	V_{S1}
< 2.7V	V_{CC}	2 * V_{CC}
2.7–3.6V	2.7V	2 * V_{CC}
≥ 4.5 V	V_{CC}	2 * V_{CC}

DEFINITIONS

R_L = Load resistor

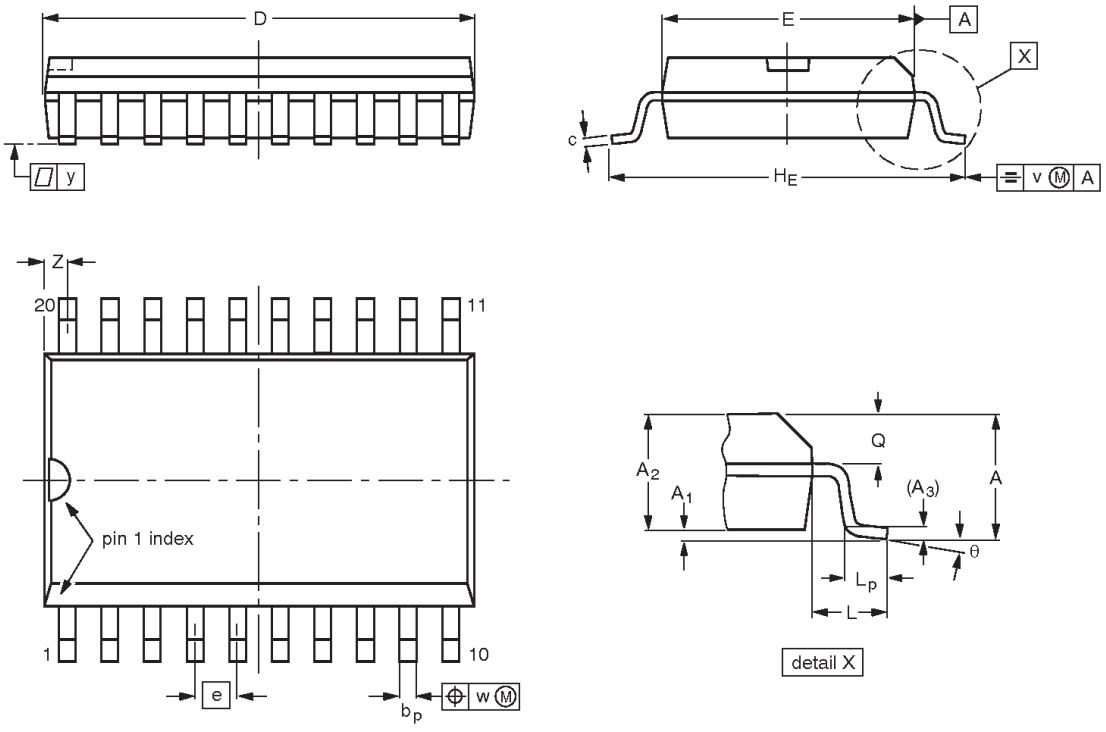
C_L = Load capacitance includes jig and probe capacitance

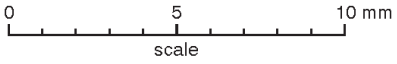
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SY00044

Waveform 3. Load circuitry for switching times.

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

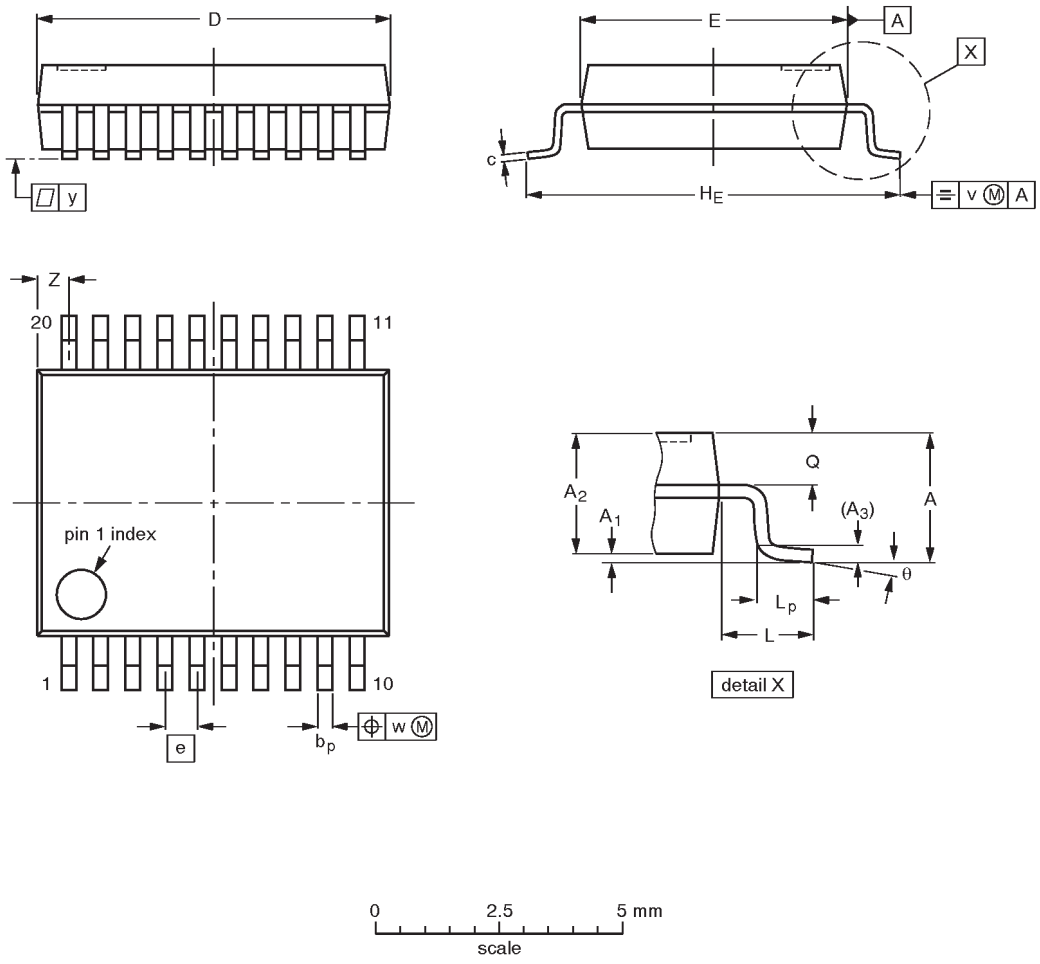
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

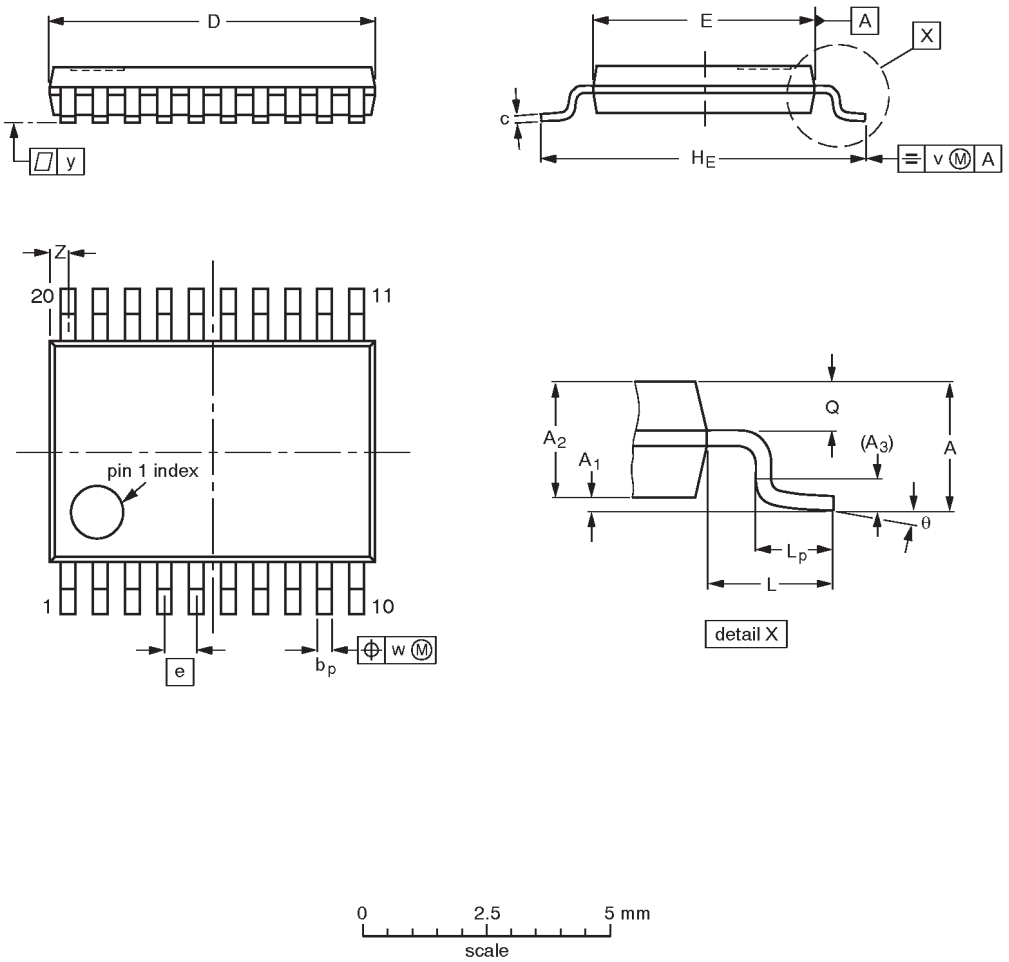
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				~~93-09-08~~ 95-02-04

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				~~93-06-16~~ 95-02-04

Octal D-type flip-flop with data enable; positive-edge trigger

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DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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