

# MC74HC390A

## Dual 4-Stage Binary Ripple Counter with $\div 2$ and $\div 5$ Sections

### High-Performance Silicon-Gate CMOS

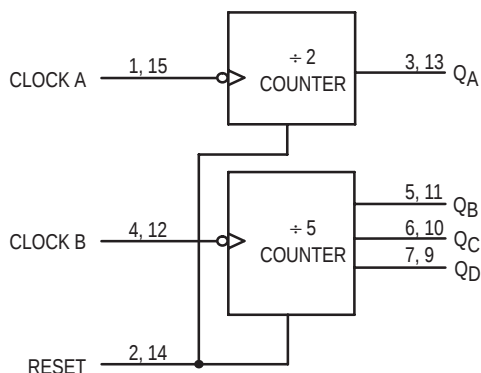
The MC74HC390A is identical in pinout to the LS390. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 4-bit counters, each composed of a divide-by-two and a divide-by-five section. The divide-by-two and divide-by-five counters have separate clock inputs, and can be cascaded to implement various combinations of  $\div 2$  and/or  $\div 5$  up to a  $\div 100$  counter.

Flip-flops internal to the counters are triggered by high-to-low transitions of the clock input. A separate, asynchronous reset is provided for each 4-bit counter. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or strobes except when gated with the Clock of the HC390A.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No 7A
- Chip Complexity: 244 FETs or 61 Equivalent Gates

#### LOGIC DIAGRAM



PIN 16 =  $V_{CC}$   
PIN 8 = GND

#### FUNCTION TABLE

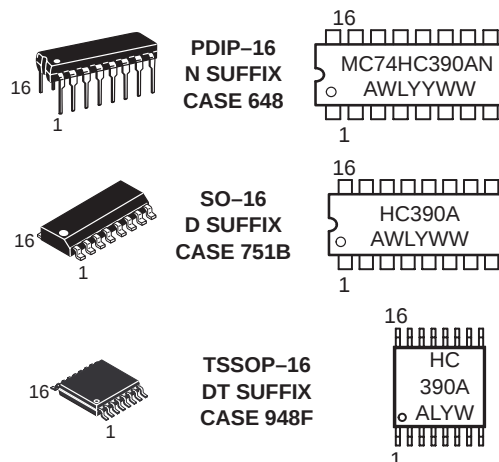
| Clock A | Clock B | Reset | Action                      |
|---------|---------|-------|-----------------------------|
| X       | X       | H     | Reset $\div 2$ and $\div 5$ |
| $\neg$  | X       | L     | Increment $\div 2$          |
| X       | $\neg$  | L     | Increment $\div 5$          |



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#### MARKING DIAGRAMS



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

#### PIN ASSIGNMENT

|                      |   |    |                      |
|----------------------|---|----|----------------------|
| CLOCK A <sub>a</sub> | 1 | 16 | $V_{CC}$             |
| RESET a              | 2 | 15 | CLOCK A <sub>b</sub> |
| Q <sub>Aa</sub>      | 3 | 14 | RESET b              |
| CLOCK B <sub>a</sub> | 4 | 13 | Q <sub>Ab</sub>      |
| Q <sub>Ba</sub>      | 5 | 12 | CLOCK B <sub>b</sub> |
| Q <sub>Ca</sub>      | 6 | 11 | Q <sub>Bb</sub>      |
| Q <sub>Da</sub>      | 7 | 10 | Q <sub>Cb</sub>      |
| GND                  | 8 | 9  | Q <sub>Db</sub>      |

#### ORDERING INFORMATION

| Device         | Package  | Shipping    |
|----------------|----------|-------------|
| MC74HC390AN    | PDIP-16  | 2000 / Box  |
| MC74HC390AD    | SOIC-16  | 48 / Rail   |
| MC74HC390ADR2  | SOIC-16  | 2500 / Reel |
| MC74HC390ADT   | TSSOP-16 | 96 / Rail   |
| MC74HC390ADTR2 | TSSOP-16 | 2500 / Reel |

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## MAXIMUM RATINGS\*

| Symbol    | Parameter                                                                             | Value                   | Unit |
|-----------|---------------------------------------------------------------------------------------|-------------------------|------|
| $V_{CC}$  | DC Supply Voltage (Referenced to GND)                                                 | – 0.5 to + 7.0          | V    |
| $V_{in}$  | DC Input Voltage (Referenced to GND)                                                  | – 0.5 to $V_{CC} + 0.5$ | V    |
| $V_{out}$ | DC Output Voltage (Referenced to GND)                                                 | – 0.5 to $V_{CC} + 0.5$ | V    |
| $I_{in}$  | DC Input Current, per Pin                                                             | ± 20                    | mA   |
| $I_{out}$ | DC Output Current, per Pin                                                            | ± 25                    | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins                                              | ± 50                    | mA   |
| $P_D$     | Power Dissipation in Still Air,<br>Plastic DIP†<br>SOIC Package†<br>TSSOP Package†    | 750<br>500<br>450       | mW   |
| $T_{stg}$ | Storage Temperature                                                                   | – 65 to + 150           | °C   |
| $T_L$     | Lead Temperature, 1 mm from Case for 10 Seconds<br>Plastic DIP, SOIC or TSSOP Package | 260                     | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C

SOIC Package: – 7 mW/°C from 65° to 125°C

TSSOP Package: – 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter                                            | Min                                                                                                                              | Max                       | Unit |
|-------------------|------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------|---------------------------|------|
| $V_{CC}$          | DC Supply Voltage (Referenced to GND)                | 2.0                                                                                                                              | 6.0                       | V    |
| $V_{in}, V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0                                                                                                                                | $V_{CC}$                  | V    |
| $T_A$             | Operating Temperature, All Package Types             | – 55                                                                                                                             | + 125                     | °C   |
| $t_r, t_f$        | Input Rise and Fall Time<br>(Figure 1)               | $V_{CC} = 2.0 \text{ V}$<br>0<br>$V_{CC} = 3.0 \text{ V}$<br>0<br>$V_{CC} = 4.5 \text{ V}$<br>0<br>$V_{CC} = 6.0 \text{ V}$<br>0 | 1000<br>600<br>500<br>400 | ns   |

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol   | Parameter                         | Test Conditions                                                                                                                               | $V_{CC}$<br>V            | Guaranteed Limit          |                           |                           | Unit |
|----------|-----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|---------------------------|---------------------------|---------------------------|------|
|          |                                   |                                                                                                                                               |                          | – 55 to<br>25°C           | ≤ 85°C                    | ≤ 125°C                   |      |
| $V_{IH}$ | Minimum High-Level Input Voltage  | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \leq 20 \mu\text{A}$                                                       | 2.0<br>3.0<br>4.5<br>6.0 | 1.5<br>2.1<br>3.15<br>4.2 | 1.5<br>2.1<br>3.15<br>4.2 | 1.5<br>2.1<br>3.15<br>4.2 | V    |
| $V_{IL}$ | Maximum Low-Level Input Voltage   | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \leq 20 \mu\text{A}$                                                       | 2.0<br>3.0<br>4.5<br>6.0 | 0.5<br>0.9<br>1.35<br>1.8 | 0.5<br>0.9<br>1.35<br>1.8 | 0.5<br>0.9<br>1.35<br>1.8 | V    |
| $V_{OH}$ | Minimum High-Level Output Voltage | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \leq 20 \mu\text{A}$                                                                       | 2.0<br>4.5<br>6.0        | 1.9<br>4.4<br>5.9         | 1.9<br>4.4<br>5.9         | 1.9<br>4.4<br>5.9         | V    |
|          |                                   | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \leq 2.4 \text{ mA}$<br>$ I_{out}  \leq 4.0 \text{ mA}$<br>$ I_{out}  \leq 5.2 \text{ mA}$ | 3.0<br>4.5<br>6.0        | 2.48<br>3.98<br>5.48      | 2.34<br>3.84<br>5.34      | 2.20<br>3.70<br>5.20      | V    |
| $V_{OL}$ | Maximum Low-Level Output Voltage  | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \leq 20 \mu\text{A}$                                                                       | 2.0<br>4.5<br>6.0        | 0.1<br>0.1<br>0.1         | 0.1<br>0.1<br>0.1         | 0.1<br>0.1<br>0.1         | V    |
|          |                                   | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \leq 2.4 \text{ mA}$<br>$ I_{out}  \leq 4.0 \text{ mA}$<br>$ I_{out}  \leq 5.2 \text{ mA}$ | 3.0<br>4.5<br>6.0        | 0.26<br>0.26<br>0.26      | 0.33<br>0.33<br>0.33      | 0.40<br>0.40<br>0.40      | V    |

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## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol          | Parameter                                      | Test Conditions                                                     | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|-----------------|------------------------------------------------|---------------------------------------------------------------------|----------------------|------------------|--------|---------|------|
|                 |                                                |                                                                     |                      | – 55 to 25°C     | ≤ 85°C | ≤ 125°C |      |
| I <sub>in</sub> | Maximum Input Leakage Current                  | V <sub>in</sub> = V <sub>CC</sub> or GND                            | 6.0                  | ± 0.1            | ± 1.0  | ± 1.0   | μA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0 μA | 6.0                  | 4                | 40     | 160     | μA   |

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>f</sub> = t<sub>r</sub> = 6 ns)

| Symbol                                 | Parameter                                                                                  | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|----------------------------------------|--------------------------------------------------------------------------------------------|----------------------|------------------|--------|---------|------|
|                                        |                                                                                            |                      | – 55 to 25°C     | ≤ 85°C | ≤ 125°C |      |
| f <sub>max</sub>                       | Maximum Clock Frequency (50% Duty Cycle)<br>(Figures 1 and 3)                              | 2.0                  | 10               | 9      | 8       | MHz  |
|                                        |                                                                                            | 3.0                  | 15               | 14     | 12      |      |
|                                        |                                                                                            | 4.5                  | 30               | 28     | 25      |      |
|                                        |                                                                                            | 6.0                  | 50               | 45     | 40      |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Clock A to QA<br>(Figures 1 and 3)                              | 2.0                  | 70               | 80     | 90      | ns   |
|                                        |                                                                                            | 3.0                  | 40               | 45     | 50      |      |
|                                        |                                                                                            | 4.5                  | 24               | 30     | 36      |      |
|                                        |                                                                                            | 6.0                  | 20               | 26     | 31      |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Clock A to QC<br>(QA connected to Clock B)<br>(Figures 1 and 3) | 2.0                  | 200              | 250    | 300     | ns   |
|                                        |                                                                                            | 3.0                  | 160              | 185    | 210     |      |
|                                        |                                                                                            | 4.5                  | 58               | 65     | 70      |      |
|                                        |                                                                                            | 6.0                  | 49               | 62     | 68      |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Clock B to QB<br>(Figures 1 and 3)                              | 2.0                  | 70               | 80     | 90      | ns   |
|                                        |                                                                                            | 3.0                  | 40               | 45     | 50      |      |
|                                        |                                                                                            | 4.5                  | 26               | 33     | 39      |      |
|                                        |                                                                                            | 6.0                  | 22               | 28     | 33      |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Clock B to QC<br>(Figures 1 and 3)                              | 2.0                  | 90               | 105    | 180     | ns   |
|                                        |                                                                                            | 3.0                  | 56               | 70     | 100     |      |
|                                        |                                                                                            | 4.5                  | 37               | 46     | 56      |      |
|                                        |                                                                                            | 6.0                  | 31               | 39     | 48      |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Clock B to QD<br>(Figures 1 and 3)                              | 2.0                  | 70               | 80     | 90      | ns   |
|                                        |                                                                                            | 3.0                  | 40               | 45     | 50      |      |
|                                        |                                                                                            | 4.5                  | 26               | 33     | 39      |      |
|                                        |                                                                                            | 6.0                  | 22               | 28     | 33      |      |
| t <sub>PHL</sub>                       | Maximum Propagation Delay, Reset to any Q<br>(Figures 2 and 3)                             | 2.0                  | 80               | 95     | 110     | ns   |
|                                        |                                                                                            | 3.0                  | 48               | 65     | 75      |      |
|                                        |                                                                                            | 4.5                  | 30               | 38     | 44      |      |
|                                        |                                                                                            | 6.0                  | 26               | 33     | 39      |      |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 1 and 3)                            | 2.0                  | 75               | 95     | 110     | ns   |
|                                        |                                                                                            | 3.0                  | 27               | 32     | 36      |      |
|                                        |                                                                                            | 4.5                  | 15               | 19     | 22      |      |
|                                        |                                                                                            | 6.0                  | 13               | 15     | 19      |      |
| C <sub>in</sub>                        | Maximum Input Capacitance                                                                  | —                    | 10               | 10     | 10      | pF   |

- For propagation delays with loads other than 50 pF, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).
- Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

| C <sub>PD</sub> | Power Dissipation Capacitance (Per Counter)* | Typical @ 25°C, V <sub>CC</sub> = 5.0 V | pF |
|-----------------|----------------------------------------------|-----------------------------------------|----|
|                 |                                              | 35                                      |    |

\* Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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## TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

| Symbol     | Parameter                                                                 | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|------------|---------------------------------------------------------------------------|----------------------|------------------|--------|---------|------|
|            |                                                                           |                      | - 55 to<br>25°C  | ≤ 85°C | ≤ 125°C |      |
| $t_{rec}$  | Minimum Recovery Time, Reset Inactive to Clock A or Clock B<br>(Figure 2) | 2.0                  | 25               | 30     | 40      | ns   |
|            |                                                                           | 3.0                  | 15               | 20     | 30      |      |
|            |                                                                           | 4.5                  | 10               | 13     | 15      |      |
|            |                                                                           | 6.0                  | 9                | 11     | 13      |      |
| $t_w$      | Minimum Pulse Width, Clock A, Clock B<br>(Figure 1)                       | 2.0                  | 75               | 95     | 110     | ns   |
|            |                                                                           | 3.0                  | 27               | 32     | 36      |      |
|            |                                                                           | 4.5                  | 15               | 19     | 22      |      |
|            |                                                                           | 6.0                  | 13               | 15     | 19      |      |
| $t_w$      | Minimum Pulse Width, Reset<br>(Figure 2)                                  | 2.0                  | 75               | 95     | 110     | ns   |
|            |                                                                           | 3.0                  | 27               | 32     | 36      |      |
|            |                                                                           | 4.5                  | 20               | 24     | 30      |      |
|            |                                                                           | 6.0                  | 18               | 22     | 28      |      |
| $t_r, t_f$ | Maximum Input Rise and Fall Times<br>(Figure 1)                           | 2.0                  | 1000             | 1000   | 1000    | ns   |
|            |                                                                           | 3.0                  | 800              | 800    | 800     |      |
|            |                                                                           | 4.5                  | 500              | 500    | 500     |      |
|            |                                                                           | 6.0                  | 400              | 400    | 400     |      |

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

## PIN DESCRIPTIONS

### INPUTS

#### Clock A (Pins 1, 15) and Clock B (Pins 4, 15)

Clock A is the clock input to the ÷ 2 counter; Clock B is the clock input to the ÷ 5 counter. The internal flip-flops are toggled by high-to-low transitions of the clock input.

### CONTROL INPUTS

#### Reset (Pins 2, 14)

Asynchronous reset. A high at the Reset input prevents counting, resets the internal flip-flops, and forces  $Q_A$  through  $Q_D$  low.

### OUTPUTS

#### $Q_A$ (Pins 3, 13)

Output of the ÷ 2 counter.

#### $Q_B, Q_C, Q_D$ (Pins 5, 6, 7, 9, 10, 11)

Outputs of the ÷ 5 counter.  $Q_D$  is the most significant bit.  $Q_A$  is the least significant bit when the counter is connected for BCD output as in Figure 4.  $Q_B$  is the least significant bit when the counter is operating in the bi-quinary mode as in Figure 5.

## SWITCHING WAVEFORMS

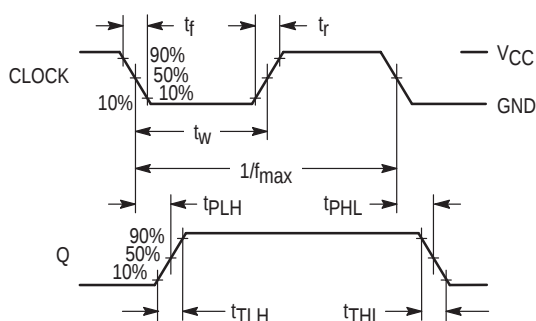


Figure 1.

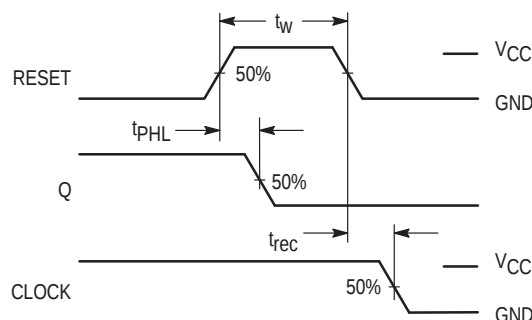
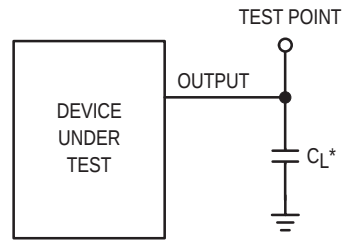


Figure 2.

# MC74HC390A

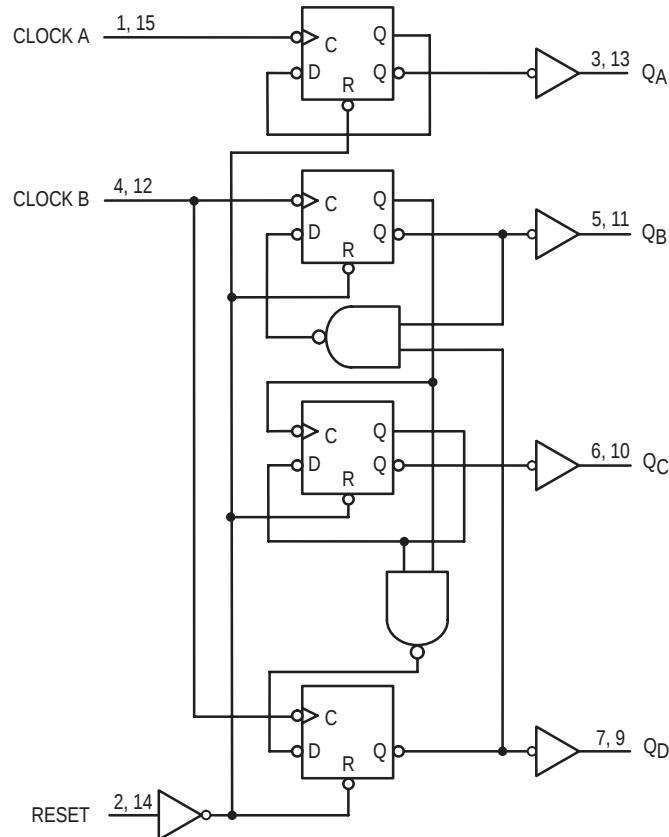
## TEST CIRCUIT



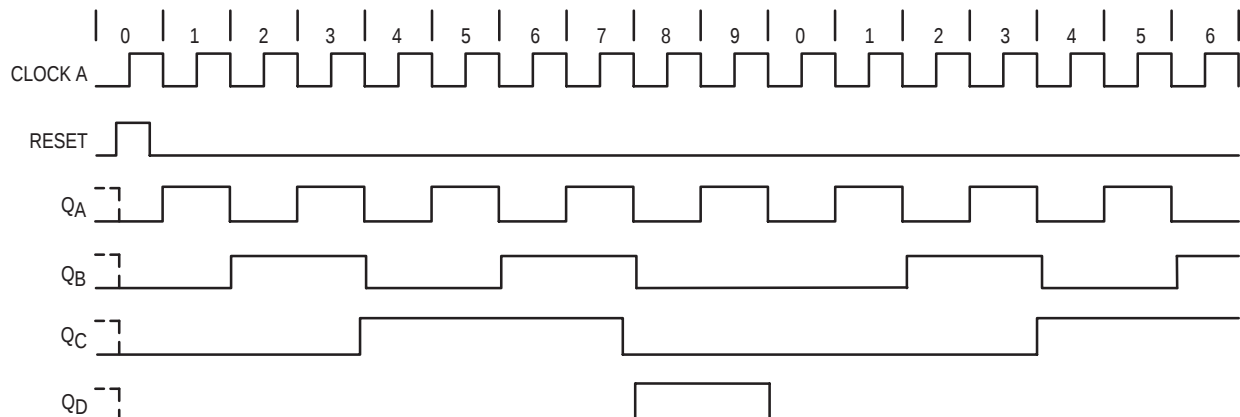
\*Includes all probe and jig capacitance

Figure 3.

## EXPANDED LOGIC DIAGRAM



## TIMING DIAGRAM ( $Q_A$ Connected to Clock B)



# MC74HC390A

## APPLICATIONS INFORMATION

Each half of the MC54/74HC390A has independent  $\div 2$  and  $\div 5$  sections (except for the Reset function). The  $\div 2$  and  $\div 5$  counters can be connected to give BCD or bi-quinary (2–5) count sequences. If Output QA is connected to the Clock B input (Figure 4), a decade divider with BCD output is obtained. The function table for the BCD count sequence is given in Table 1.

To obtain a bi-quinary count sequence, the input signals connected to the Clock B input, and output QD is connected to the Clock A input (Figure 5). The bi-quinary count sequence function table is given in Table 2.

**Table 1. BCD Count Sequence\***

| Count | Output |    |    |    |
|-------|--------|----|----|----|
|       | QD     | QC | QB | QA |
| 0     | L      | L  | L  | L  |
| 1     | L      | L  | L  | H  |
| 2     | L      | L  | H  | L  |
| 3     | L      | L  | H  | H  |
| 4     | L      | H  | L  | L  |
| 5     | L      | H  | L  | H  |
| 6     | L      | H  | H  | L  |
| 7     | L      | H  | H  | H  |
| 8     | H      | L  | L  | L  |
| 9     | H      | L  | L  | H  |

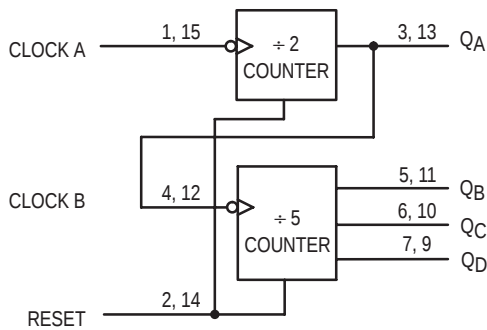
\*QA connected to Clock B input.

**Table 2. Bi-Quinary Count Sequence\*\***

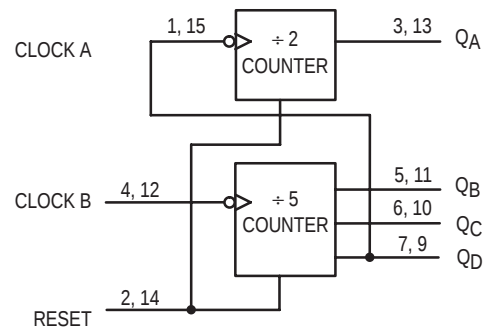
| Count | Output |    |    |    |
|-------|--------|----|----|----|
|       | QA     | QD | QC | QB |
| 0     | L      | L  | L  | L  |
| 1     | L      | L  | L  | H  |
| 2     | L      | L  | H  | L  |
| 3     | L      | L  | H  | H  |
| 4     | L      | H  | L  | L  |
| 8     | H      | L  | L  | L  |
| 9     | H      | L  | L  | H  |
| 10    | H      | L  | H  | L  |
| 11    | H      | L  | H  | H  |
| 12    | H      | H  | L  | L  |

\*\*QD connected to Clock A input.

## CONNECTION DIAGRAMS



**Figure 4. BCD Count**

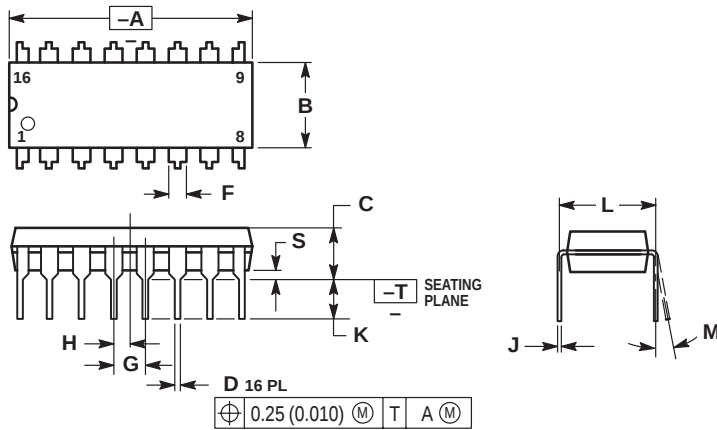


**Figure 5. Bi-Quinary Count**

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## PACKAGE DIMENSIONS

PDIP-16  
N SUFFIX  
CASE 648-08  
ISSUE R

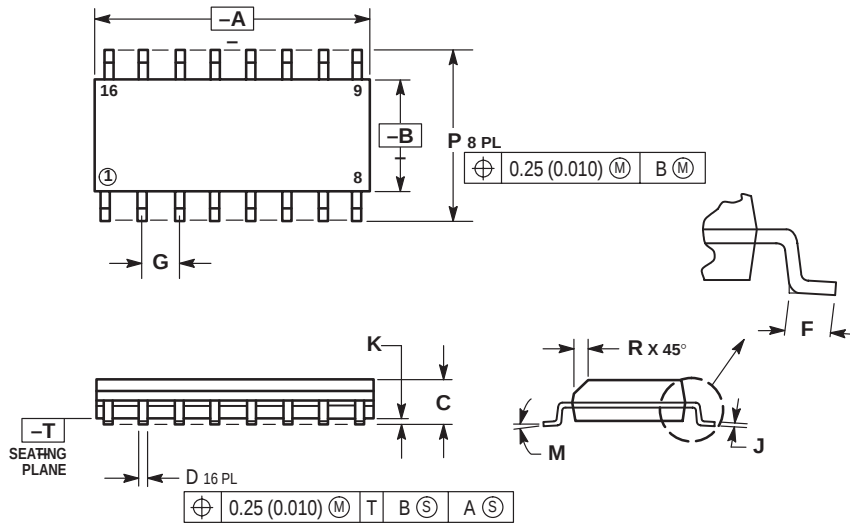


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.740     | 0.770 | 18.80       | 19.55 |
| B   | 0.250     | 0.270 | 6.35        | 6.85  |
| C   | 0.145     | 0.175 | 3.69        | 4.44  |
| D   | 0.015     | 0.021 | 0.39        | 0.53  |
| F   | 0.040     | 0.070 | 1.02        | 1.77  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.050 BSC |       | 1.27 BSC    |       |
| J   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.110     | 0.130 | 2.80        | 3.30  |
| L   | 0.295     | 0.305 | 7.50        | 7.74  |
| M   | 0°        | 10°   | 0°          | 10°   |
| S   | 0.020     | 0.040 | 0.51        | 1.01  |

SOIC-16  
D SUFFIX  
CASE 751B-05  
ISSUE J



### NOTES:

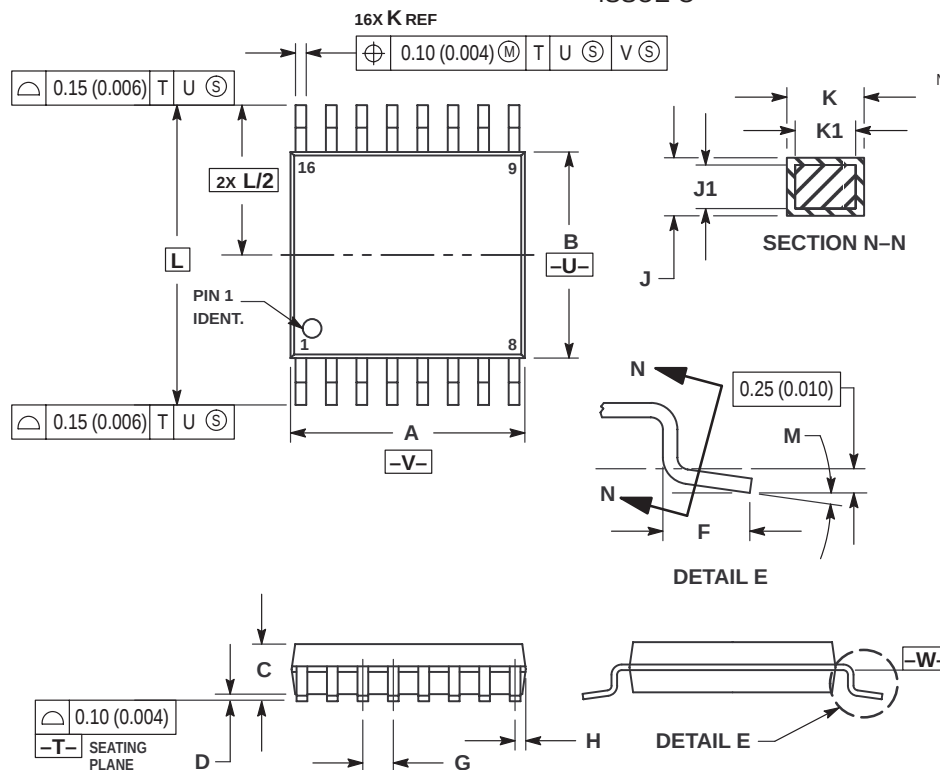
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.40        | 1.25  | 0.016     | 0.049 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.19        | 0.25  | 0.008     | 0.009 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 5.80        | 6.20  | 0.229     | 0.244 |
| R   | 0.25        | 0.50  | 0.010     | 0.019 |

# MC74HC390A

## PACKAGE DIMENSIONS

TSSOP-16  
DT SUFFIX  
CASE 948F-01  
ISSUE O



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |           | INCHES    |       |
|-----|-------------|-----------|-----------|-------|
|     | MIN         | MAX       | MIN       | MAX   |
| A   | 4.90        | 5.10      | 0.193     | 0.200 |
| B   | 4.30        | 4.50      | 0.169     | 0.177 |
| C   | —           | 1.20      | —         | 0.047 |
| D   | 0.05        | 0.15      | 0.002     | 0.006 |
| F   | 0.50        | 0.75      | 0.020     | 0.030 |
| G   | 0.65 BSC    | —         | 0.026 BSC | —     |
| H   | 0.18        | 0.28      | 0.007     | 0.011 |
| J   | 0.09        | 0.20      | 0.004     | 0.008 |
| J1  | 0.09        | 0.16      | 0.004     | 0.006 |
| K   | 0.19        | 0.30      | 0.007     | 0.012 |
| K1  | 0.19        | 0.25      | 0.007     | 0.010 |
| L   | 6.40 BSC    | 0.252 BSC | —         | —     |
| M   | 0°          | 8°        | 0°        | 8°    |

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