Triple 8-bit video digital-to-analog converter

TDA8772; TDA8772A

FEATURES

- 8-bit resolution
- Sampling rate up to
  - 35 MHz for TDA8772H/3, TDA8772AH/3
  - 85 MHz for TDA8772H/8, TDA8772AH/8
- Internal reference voltage regulator
- No deglitching circuit required
- $\overline{SYNC}$, $\overline{BLANK}$ control inputs
- 3 independent clock inputs (one per DAC)
- 1 V output voltage range
- 75 Ω output load
- TDA8772A has $\overline{BLANK}$ control input on the GREEN channel only while TDA8772 has it on the 3 channels
- Single 5 V power supply
- 44-pin QFP package.

APPLICATIONS

- General purpose high-speed digital-to-analog conversion
- Digital TV
- Graphic display
- Desktop video processing.

GENERAL DESCRIPTION

The TDA8772, TDA8772A are triple 8-bit video digital-to-analog converters (DACs). They convert the digital input signals into analog voltage outputs at a maximum conversion rate of 35 MHz (TDA8772H/3, TDA8772AH/3) and 85 MHz (TDA8772H/8, TDA8772AH/8).

The DACs are based on resistor-string architecture with integrated output buffers. The output voltage range is determined by a built-in reference source.

The devices are fabricated in a 5 V CMOS process that ensures high functionality with low power dissipation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	R_L = 75 Ω	–	45	85	mA
I_{DDD}	digital supply current					
	TDA8772H/3, TDA8772AH/3		–	7	16	mA
	TDA8772H/8, TDA8772AH/8		–	16	27	mA
ILE	DC integral linear error	f_{clk} = 35 MHz	–	±0.5	±1	LSB
		f_{clk} = 85 MHz	–	±0.75	tbf	LSB
DLE	DC differential linearity error	f_{clk} = 35 MHz	–	±0.25	±0.5	LSB
		f_{clk} = 85 MHz	-	±0.5	tbf	LSB
$f_{clk(max)}$	maximum clock frequency					
	TDA8772H/3, TDA8772AH/3		35	–	–	MHz
	TDA8772H/8, TDA8772AH/8		85	–	–	MHz
P_{tot}	total power dissipation					
	TDA8772H/3, TDA8772AH/3	R_L = 75 Ω	–	260	530	mW
	TDA8772H/8, TDA8772AH/8	R_L = 75 Ω	–	310	590	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				SAMPLING FREQUENCY
	PINS	PIN POSITION	MATERIAL	CODE	
TDA8772H/3	44	QFP44	plastic	SOT307B	35 MHz
TDA8772AH/3	44	QFP44	plastic	SOT307B	35 MHz
TDA8772H/8	44	QFP44	plastic	SOT307B	85 MHz
TDA8772AH/8	44	QFP44	plastic	SOT307B	85 MHz

BLOCK DIAGRAMS

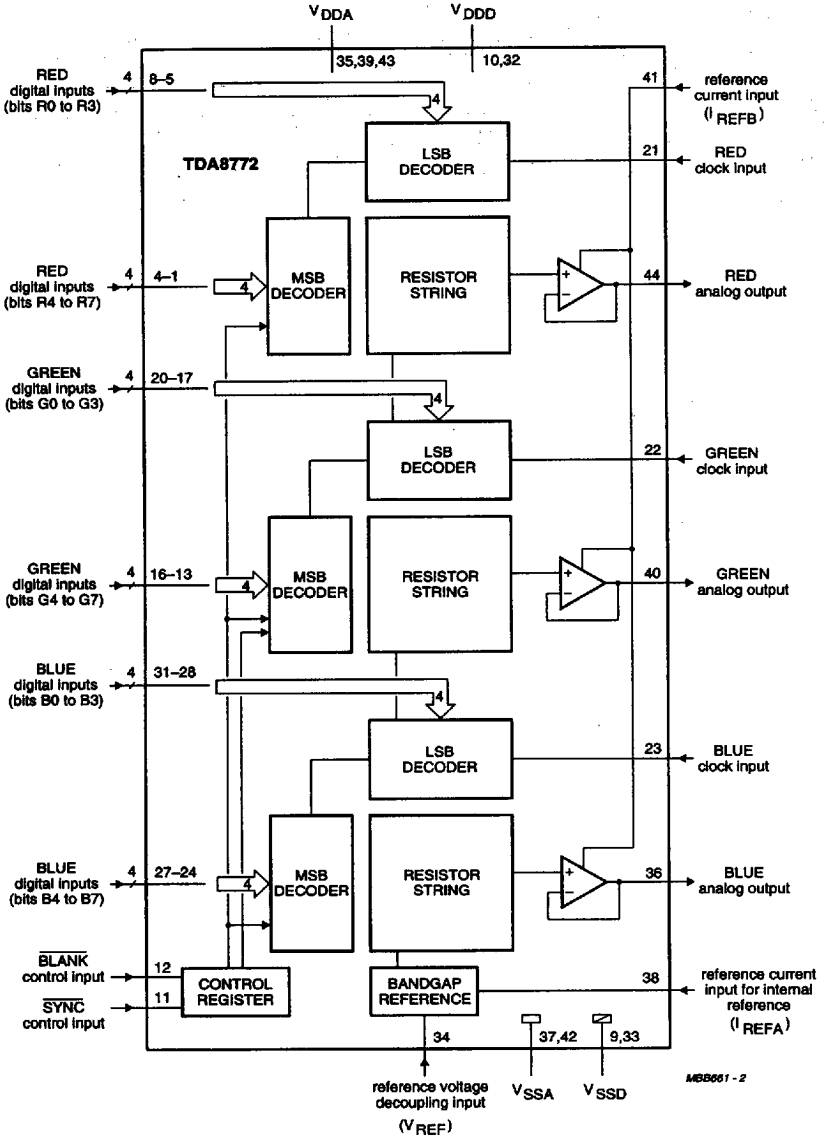


Fig.1 Block diagram for TDA8772.

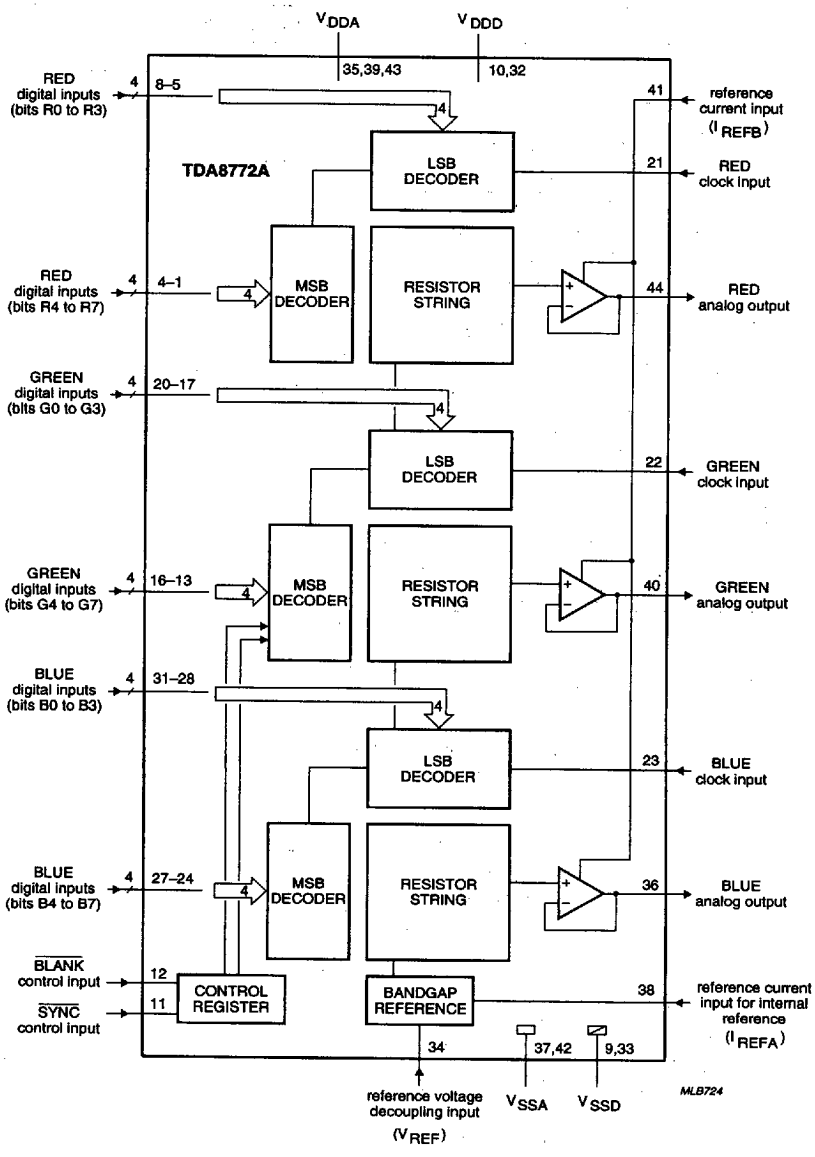


Fig.2 Block diagram for TDA8772A.

PINNING

SYMBOL	PIN	DESCRIPTION
R7	1	RED digital input data; bit 7 (MSB)
R6	2	RED digital input data; bit 6
R5	3	RED digital input data; bit 5
R4	4	RED digital input data; bit 4
R3	5	RED digital input data; bit 3
R2	6	RED digital input data; bit 2
R1	7	RED digital input data; bit 1
R0	8	RED digital input data; bit 0 (LSB)
V_{SSD1}	9	digital supply ground 1
V_{DDD1}	10	digital supply voltage 1
$\overline{SYNC}$	11	composite sync control input; for GREEN channel only (active LOW)
$\overline{BLANK}$	12	composite blank control input (active LOW)
G7	13	GREEN digital input data; bit 7 (MSB)
G6	14	GREEN digital input data; bit 6
G5	15	GREEN digital input data; bit 5
G4	16	GREEN digital input data; bit 4
G3	17	GREEN digital input data; bit 3
G2	18	GREEN digital input data; bit 2
G1	19	GREEN digital input data; bit 1
G0	20	GREEN digital input data; bit 0 (LSB)
CLKR	21	RED clock input
CLKG	22	GREEN clock input
CLKB	23	BLUE clock input
B7	24	BLUE digital input data; bit 7 (MSB)
B6	25	BLUE digital input data; bit 6
B5	26	BLUE digital input data; bit 5
B4	27	BLUE digital input data; bit 4
B3	28	BLUE digital input data; bit 3
B2	29	BLUE digital input data; bit 2
B1	30	BLUE digital input data; bit 1
B0	31	BLUE digital input data; bit 0 (LSB)
V_{DDD2}	32	digital supply voltage 2
V_{SSD2}	33	digital supply ground 2
V_{REF}	34	decoupling input for reference voltage
V_{DDA1}	35	analog supply voltage 1
OUTB	36	BLUE analog output
V_{SSA1}	37	analog supply ground 1
I_{REFA}	38	reference current input for internal reference
V_{DDA2}	39	analog supply voltage 2
OUTG	40	GREEN analog output

SYMBOL	PIN	DESCRIPTION
I_{REFB}	41	reference current input for output buffers
V_{SSA2}	42	analog supply ground 2
V_{DDA3}	43	analog supply voltage 3
OUTR	44	RED analog output

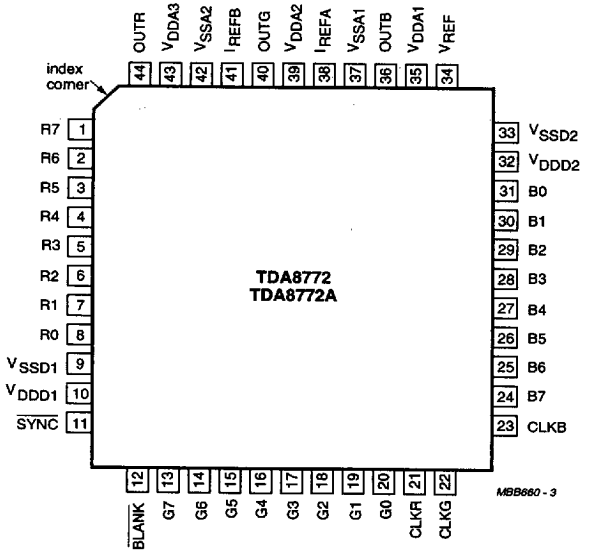


Fig.3 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	−0.5	+6.5	V
V_{DDD}	digital supply voltage	−0.5	+6.5	V
ΔV_{DD}	supply voltage differences between V_{DDA} and V_{DDD}	−1.0	+1.0	V
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	−	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

TDA8772H/3, TDA8772AH/3 operating at 35 MHz and TDA8772H/8, TDA8772AH/8 operating at 85 MHz unless otherwise specified.

$V_{DDA} = V_{DDD} = 4.5$ V to 5.5 V; V_{SSA} and V_{SSD} shorted together; $V_{DDA} - V_{DDD} = -0.5$ V to +0.5 V; $T_{amb} = 0$ to +70 °C; typical values measured at $V_{DDA} = V_{DDD} = 5$ V and $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	$R_L = 75\ \Omega$	–	45	85	mA
I_{DDD}	digital supply current					
	TDA8772H/3, TDA8772AH/3		–	7	16	mA
	TDA8772H/8, TDA8772AH/8		–	16	27	mA
Inputs						
CLOCK INPUTS (PINS 21, 22 AND 23)						
V_{IL}	LOW level input voltage		$V_{SSD} - 0.5$	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	$V_{DDD} + 0.5$	V
$\overline{BLANK}$, $\overline{SYNC}$ INPUTS (PINS 12 AND 11; ACTIVE LOW)						
V_{IL}	LOW level input voltage		$V_{SSD} - 0.5$	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	$V_{DDD} + 0.5$	V
R, G, B DIGITAL INPUTS (PINS 1 TO 8, 13 TO 20 AND 24 TO 31)						
V_{IL}	LOW level input voltage		$V_{SSD} - 0.5$	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	$V_{DDD} + 0.5$	V
I_{REFA} INTERNAL REFERENCE SUPPLY CURRENT (PIN 38)						
I_I	input current		–	0.17	0.25	mA
I_{REFB} OUTPUT BUFFER SUPPLY CURRENT (PIN 41)						
I_I	input current		–	0.5	0.7	mA
Timing (C_L = 25 pF; R_L 75 Ω; see Fig.4)						
$f_{clk(max)}$	maximum clock frequency					
	TDA8772H/3, TDA8772AH/3		35	–	–	MHz
	TDA8772H/8, TDA8772AH/8		85	–	–	MHz
δ_{clk}	clock duty factor		40	–	60	%
t_r	clock rise time					
	TDA8772H/3, TDA8772AH/3		–	–	5	ns
	TDA8772H/8, TDA8772AH/8		–	–	3	ns
t_f	clock fall time					
	TDA8772H/3, TDA8772AH/3		–	–	5	ns
	TDA8772H/8, TDA8772AH/8		–	–	3	ns
$t_{SU;DAT}$	input data set-up time		4	–	–	ns
$t_{HD;DAT}$	input data hold time		2.5	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage reference (pin 34, referenced to V_{SSA})						
V_{REF}	output reference voltage		1.180	1.242	1.305	V
Outputs						
OUTB, OUTR, OUTG ANALOG OUTPUTS (PINS 36, 44 AND 40, REFERENCED TO V_{SSA}) FOR 75 Ω LOAD; SEE TABLES 1 AND 2						
FSR	full-scale output voltage range		0.9	1.0	1.1	V
V_{os}	offset of analog voltage output		0.75	0.83	0.95	V
V_{OUTmax}	maximum output voltage	data inputs = logic 1; note 1	1.65	1.83	2.05	V
V_{OUTmin}	minimum output voltage	data inputs = logic 0; note 1	0.75	0.83	0.95	V
THD	total harmonic distortion	f_i = 4.43 MHz; f_{clk} = 35 MHz	–	–41	–	dB
		f_i = 4.43 MHz; f_{clk} = 85 MHz	–	–40	–	dB
Z_L	output load impedance		60	75	90	Ω
Transfer function (f_{clk} = 85 MHz)						
ILE	DC integral linear error	f_{clk} = 35 MHz	–	±0.5	±1	LSB
		f_{clk} = 85 MHz	–	±0.75	tbf	LSB
DLE	DC differential linearity error	f_{clk} = 35 MHz	–	±0.25	±0.5	LSB
		f_{clk} = 85 MHz	-	±0.5	tbf	LSB
α_{CT}	crosstalk DAC to DAC		–45	–	–	dB
	DAC to DAC matching		–	1.0	2.0	%
Switching characteristics (for 75 Ω output load; see Fig.5)						
t_d	input to 50% output delay time	full-scale change	–	10	–	ns
t_{s1}	settling time	10% to 90% full-scale change	–	6	–	ns
t_{s2}	settling time	to ±1 LSB	–	30	–	ns
Output transients (glitches)						
V_g	area for 1 LSB change		–	1	–	LSB.ns

Note

1. V_{OUT} is directly proportional to V_{REF}.

Table 1 Input coding and DAC output voltages (typical values).

BINARY INPUT DATA (SYNC = BLANK = 0)	CODE	DAC OUTPUT VOLTAGES (V) OUTB, OUTR, OUTG R_L = 75 Ω
0000 0000	0	0.830
0000 0001	1	0.834
....	.	.
1000 0000	128	1.330
....	.	.
1111 1110	254	1.826
1111 1111	255	1.830

Table 2 Input coding and DAC output voltages (typical values).

BINARY INPUT DATA	$\overline{\text{SYNC}}$ (PIN 11)	$\overline{\text{BLANK}}$ (PIN 12)	DAC OUTPUT VOLTAGES (V)		
			OUTG (PIN 40)	OUTR/B (PIN 44, 46) TDA8772	OUTR/B (PIN 44, 46) TDA8772A
....	x	1	see Table 1	see Table 1	see Table 1
....	1	0	0.830	0.830	
....	0	0	0.440		

TIMING

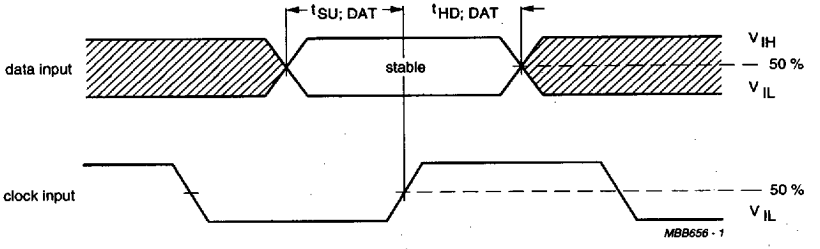


Fig.4 Input timing.

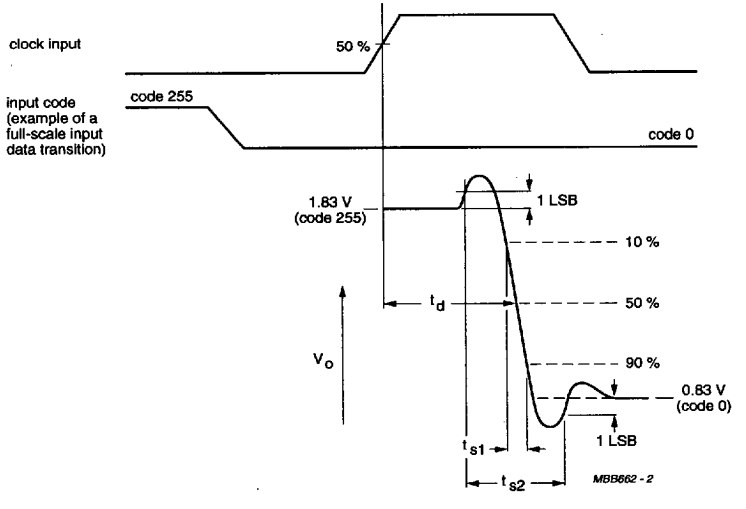
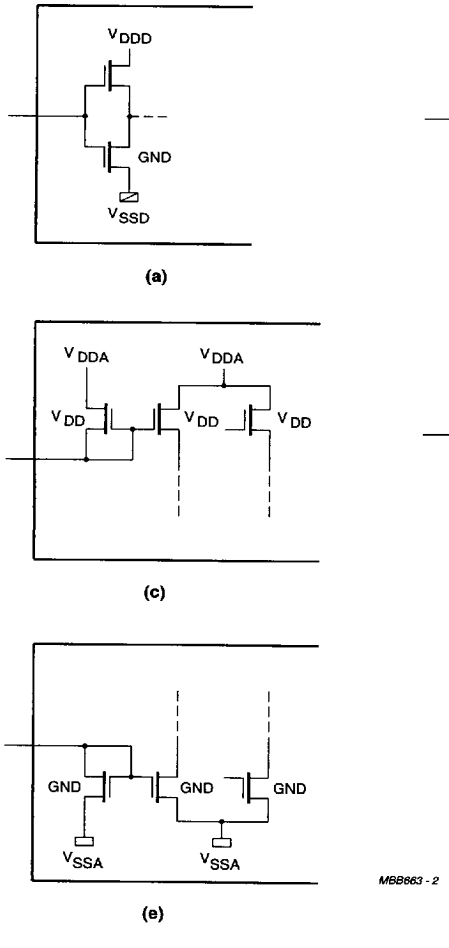


Fig.5 Switching timing.

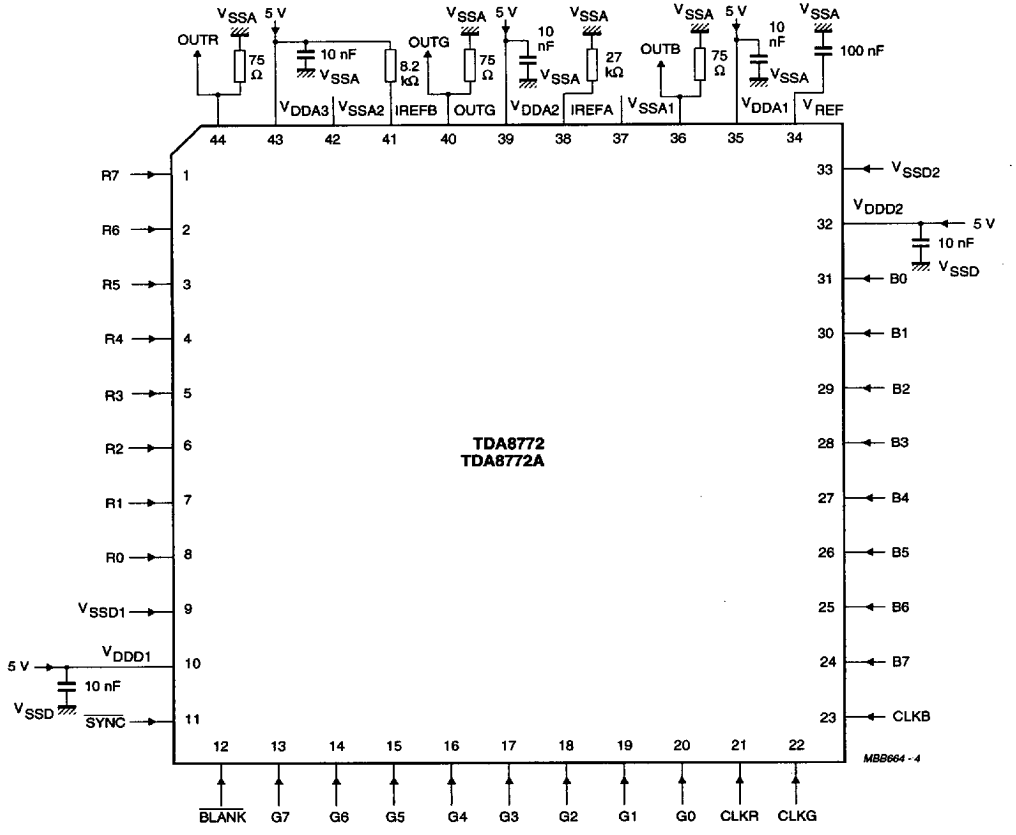
INTERNAL CIRCUITRY



(a) Digital inputs; pins 1 to 8, and 11 to 31.
(b) VREF; pin 34.
(c) IREFA; pin 38.
(d) OUTR, G, B; pins 44, 40 and 36.
(e) IREFB; pin 41.

Fig.6 Internal circuitry.

APPLICATION INFORMATION



Analog and digital supplies should be separated and decoupled.
Supplies are not connected internally.
All ground pins must be connected. One ground plane is preferred although it depends on the application.
See Fig.8 for example of anti-aliasing filter.

Fig.7 Application diagram.

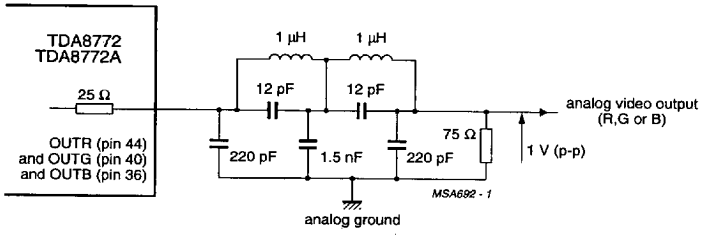


Fig.8 Example of anti-aliasing filter for 1 V output swing.

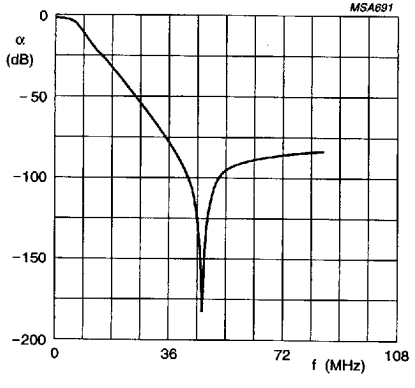


Fig.9 Frequency response for filter shown in Fig. 8.

Characteristics of Fig. 9

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \geq 0.6$ dB
- f at −3 dB = 6.5 MHz
- f_{NOTCH} = 46 MHz.