

## Features

- Very high speed: 45 ns
- Temperature range
  - Industrial: -40 °C to +85 °C
- Wide voltage range: 2.20 V to 3.60 V
- Ultra low standby power
  - Typical standby current: 1 μA
  - Maximum standby current: 7 μA (Industrial)
- Ultra low active power
  - Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  Features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 44-pin thin small outline package (TSOP) II package
- Byte power down feature

## Functional Description

The CY621472E30 is a high performance CMOS static RAM (SRAM) organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device

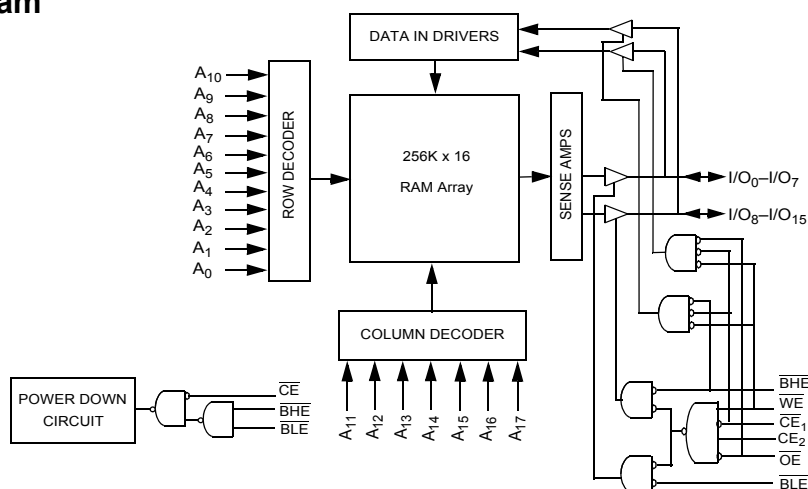
also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW or both  $\overline{BLE}$  and  $\overline{BHE}$  are HIGH). The input and output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high impedance state when:

- Deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW)
- Outputs are disabled ( $\overline{OE}$  HIGH)
- Both Byte High Enable and Byte Low Enable are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH)
- Write operation is active ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH and  $\overline{WE}$  LOW)

To write to the device, take Chip Enable ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from  $I/O$  pins ( $I/O_0$  through  $I/O_7$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{17}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from  $I/O$  pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{17}$ ).

To read from the device, take Chip Enable ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on  $I/O_8$  to  $I/O_{15}$ . See the [Truth Table on page 11](#) for a complete description of read and write modes.

## Logic Block Diagram



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## Product Portfolio

Product	Range	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
						Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
		f = 1 MHz		f = f <sub>max</sub>							
		Min	Typ <sup>[1]</sup>	Max		Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max
CY621472E30LL	Industrial	2.2	3.0	3.6	45	2	2.5	15	20	1	7

## Pin Configuration

Figure 1. 44-pin TSOP II pinout

A <sub>4</sub>	1	44	A <sub>5</sub>
A <sub>3</sub>	2	43	A <sub>6</sub>
A <sub>2</sub>	3	42	A <sub>7</sub>
A <sub>1</sub>	4	41	OE
A <sub>0</sub>	5	40	BHE
CE <sub>1</sub>	6	39	BLE
I/O <sub>0</sub>	7	38	I/O <sub>15</sub>
I/O <sub>1</sub>	8	37	I/O <sub>14</sub>
I/O <sub>2</sub>	9	36	I/O <sub>13</sub>
I/O <sub>3</sub>	10	35	I/O <sub>12</sub>
V <sub>CC</sub>	11	34	V <sub>SS</sub>
V <sub>SS</sub>	12	33	V <sub>CC</sub>
I/O <sub>4</sub>	13	32	I/O <sub>11</sub>
I/O <sub>5</sub>	14	31	I/O <sub>10</sub>
I/O <sub>6</sub>	15	30	I/O <sub>9</sub>
I/O <sub>7</sub>	16	29	I/O <sub>8</sub>
WE	17	28	CE <sub>2</sub>
A <sub>17</sub>	18	27	A <sub>8</sub>
A <sub>16</sub>	19	26	A <sub>9</sub>
A <sub>15</sub>	20	25	A <sub>10</sub>
A <sub>14</sub>	21	24	A <sub>11</sub>
A <sub>13</sub>	22	23	A <sub>12</sub>

### Note

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage to ground potential ..... -0.3 V to +3.9 V ( $V_{CCmax} + 0.3$  V)

DC Voltage Applied to Outputs in High Z State <sup>[2, 3]</sup> ..... -0.3 V to 3.9 V ( $V_{CCmax} + 0.3$  V)

DC input voltage <sup>[2, 3]</sup> ..... -0.3 V to 3.9 V ( $V_{CCmax} + 0.3$  V)

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch up current..... > 200 mA

## Operating Range

Device	Range	Ambient Temperature	$V_{CC}$ <sup>[4]</sup>
CY621472E30LL	Industrial	-40 °C to +85 °C	2.2 V to 3.6 V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns			Unit
			Min	Typ <sup>[5]</sup>	Max	
$V_{OH}$	Output HIGH voltage	$I_{OH} = -0.1$ mA	2.0	—	—	V
		$I_{OH} = -1.0$ mA, $V_{CC} \geq 2.70$ V	2.4	—	—	V
$V_{OL}$	Output LOW voltage	$I_{OL} = 0.1$ mA	—	—	0.4	V
		$I_{OL} = 2.1$ mA, $V_{CC} = 2.70$ V	—	—	0.4	V
$V_{IH}$	Input HIGH voltage	$V_{CC} = 2.2$ V to 2.7 V	1.8	—	$V_{CC} + 0.3$	V
		$V_{CC} = 2.7$ V to 3.6 V	2.2	—	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW voltage	$V_{CC} = 2.2$ V to 2.7 V	-0.3	—	0.6	V
		$V_{CC} = 2.7$ V to 3.6 V	-0.3	—	0.8	V
$I_{IX}$	Input leakage current	$GND \leq V_I \leq V_{CC}$	-1	—	+1	μA
$I_{OZ}$	Output leakage current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-1	—	+1	μA
$I_{CC}$	$V_{CC}$ operating supply current	$f = f_{max} = 1/t_{RC}$	—	15	20	mA
		$f = 1$ MHz	—	2	2.5	
$I_{SB1}$ <sup>[6]</sup>	Automatic CE power-down current – CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2$ V, $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V, $f = f_{max}$ (address and data only),  $f = 0$ ( $\overline{OE}$ , $\overline{BHE}$ , $\overline{BLE}$ and $\overline{WE}$ ), $V_{CC} = 3.60$ V	—	1	7	μA
$I_{SB2}$ <sup>[6]</sup>	Automatic CE Power down current – CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or  $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2$ V,  $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$ , $V_{CC} = 3.60$ V	—	1	7	μA

### Notes

- $V_{IL(min)}$  = -2.0 V for pulse durations less than 20 ns.
- $V_{IH(max)}$  =  $V_{CC} + 0.75$  V for pulse durations less than 20 ns.
- Full device AC operation assumes a minimum of 100 μs ramp time from 0 to  $V_{CC(min)}$  and 200 μs wait time after  $V_{CC}$  stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25$  °C.
- Chip enables ( $\overline{CE}_1$  and  $CE_2$ ) need to be tied to CMOS levels to meet the  $I_{SB1}$  /  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.

## Capacitance

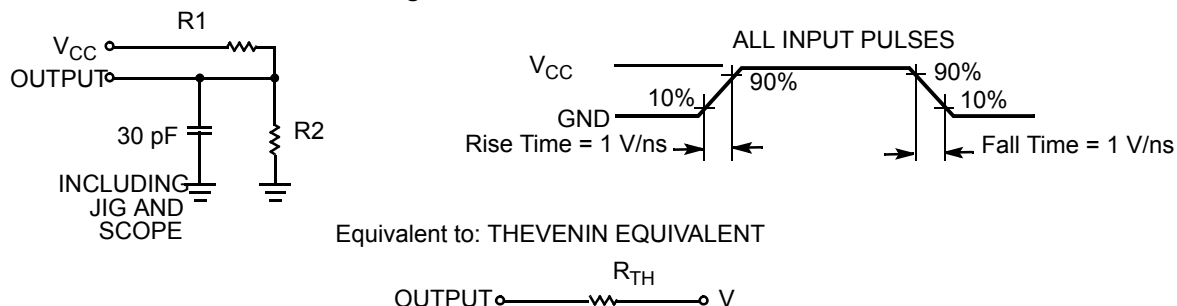
Parameter <sup>[7]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25\text{ }^{\circ}\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = V_{CC(typ)}$	10	pF
$C_{OUT}$	Output capacitance		10	pF

## Thermal Resistance

Parameter <sup>[7]</sup>	Description	Test Conditions	44-pin TSOP II Package	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Still Air, soldered on a $3 \times 4.5$ inch, two-layer printed circuit board	77	$^{\circ}\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		13	$^{\circ}\text{C/W}$

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	2.50 V	3.0 V	Unit
R1	16667	1103	$\Omega$
R2	15385	1554	$\Omega$
$R_{TH}$	8000	645	$\Omega$
$V_{TH}$	1.20	1.75	V

### Note

7. Tested initially and after any design or process changes that may affect these parameters.

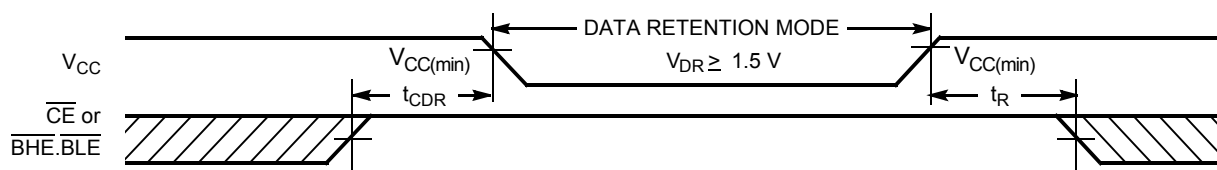
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[8]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1.5	–	–	V
$I_{CCDR}^{[9]}$	Data retention current	$V_{CC} = 1.5\text{ V}$ , $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	0.8	7	$\mu\text{A}$
$t_{CDR}^{[10]}$	Chip deselect to data retention time		0	–	–	ns
$t_R^{[11]}$	Operation recovery time		45	–	–	ns

## Data Retention Waveform

Figure 3. Data Retention Waveform<sup>[12, 13]</sup>



### Notes

8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25^\circ\text{C}$ .
9. Chip enables ( $\overline{CE}_1$  and  $CE_2$ ) need to be tied to CMOS levels to meet the  $I_{SB1}$  /  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.
10. Tested initially and after any design or process changes that may affect these parameters.
11. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ .
12.  $\overline{CE}$  refers to the internal logical combination of  $\overline{CE}_1$  and  $CE_2$  such that when  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW. For all other cases  $\overline{CE}$  is HIGH.
13.  $\overline{BHE.BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Deselect the chip by either disabling the chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

## Switching Characteristics

Over the Operating Range

Parameter <sup>[14]</sup>	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t <sub>RC</sub>	Read cycle time	45	–	ns
t <sub>AA</sub>	Address to data valid	–	45	ns
t <sub>OHA</sub>	Data hold from address change	10	–	ns
t <sub>ACE</sub>	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to data valid	–	45	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to data valid	–	22	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[15]</sup>	5	–	ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[15, 16]</sup>	–	18	ns
t <sub>LZCE</sub>	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to Low Z <sup>[15]</sup>	10	–	ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH/ $CE_2$ LOW to High Z <sup>[15, 16]</sup>	–	18	ns
t <sub>PU</sub>	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to Power-up	0	–	ns
t <sub>PD</sub>	$CE_1$ HIGH/ $CE_2$ LOW to Power-down	–	45	ns
t <sub>DBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to data valid	–	45	ns
t <sub>LZBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Low Z <sup>[15, 17]</sup>	5	–	ns
t <sub>HZBE</sub>	$\overline{BLE}/\overline{BHE}$ HIGH to High Z <sup>[15, 16]</sup>	–	18	ns
Write Cycle <sup>[18, 19]</sup>				
t <sub>WC</sub>	Write cycle time	45	–	ns
t <sub>SCE</sub>	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to Write End	35	–	ns
t <sub>AW</sub>	Address setup to write end	35	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	ns
t <sub>SA</sub>	Address setup to write start	0	–	ns
t <sub>PWE</sub>	$\overline{WE}$ pulse width	35	–	ns
t <sub>BW</sub>	$\overline{BLE}/\overline{BHE}$ LOW to write end	35	–	ns
t <sub>SD</sub>	Data setup to write end	25	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[15, 16]</sup>	–	18	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[15]</sup>	10	–	ns

### Notes

14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the [Figure 2 on page 5](#).

15. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.

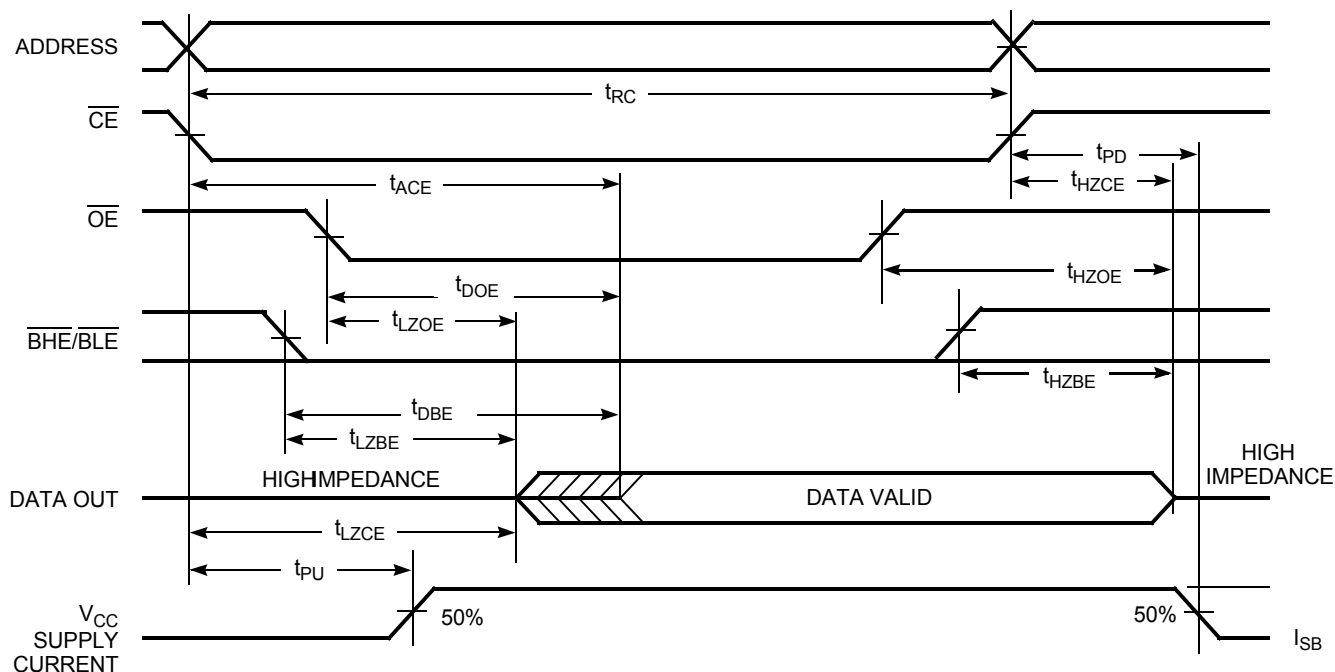
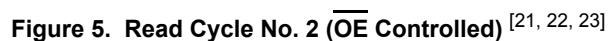
16.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.

17. If both byte enables are together, this value is 10 ns.

18. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$ , or both =  $V_{IL}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

19. The minimum write cycle pulse width for WRITE Cycle 4 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) should be equal to the sum of  $t_{HZWE}$  and  $t_{SD}$ .

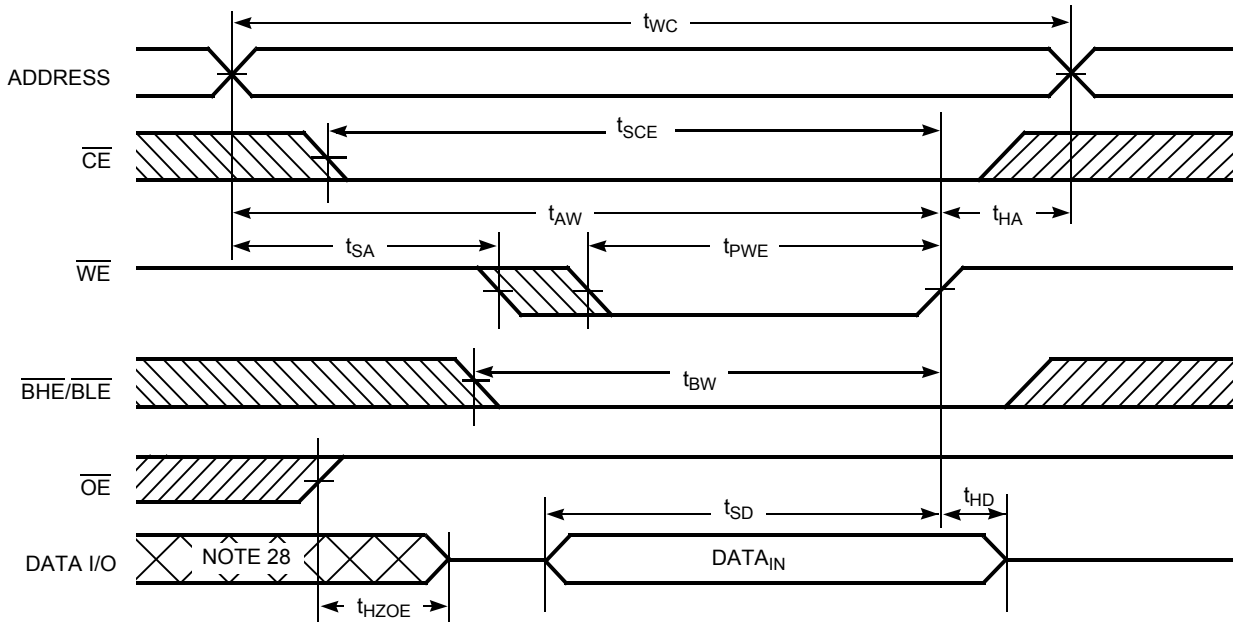
**Figure 4. Read Cycle No. 1 (Address Transition Controlled) [20, 21]**



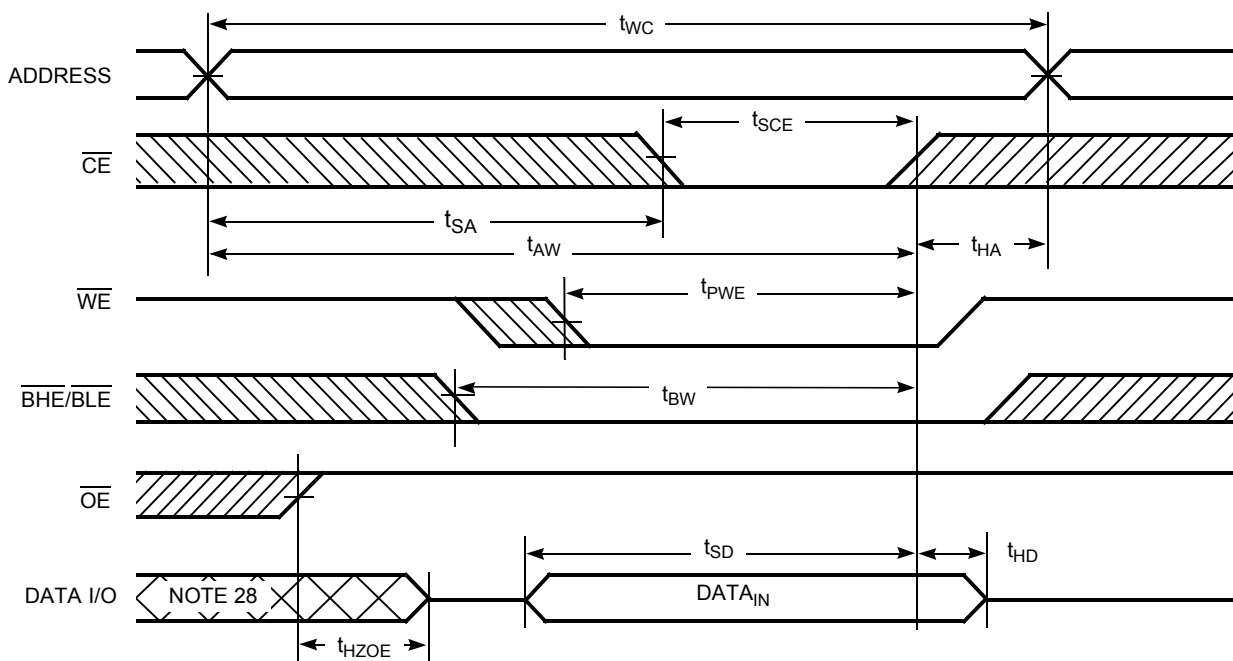
23. Address valid before or similar to  $\overline{CE}$  and  $\overline{BHE}$ .  $\overline{BLE}$  transition LOW.

## Switching Waveforms (continued)

**Figure 6. Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled)** [24, 25, 26, 27]



**Figure 7. Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)** [24, 25, 26, 27]

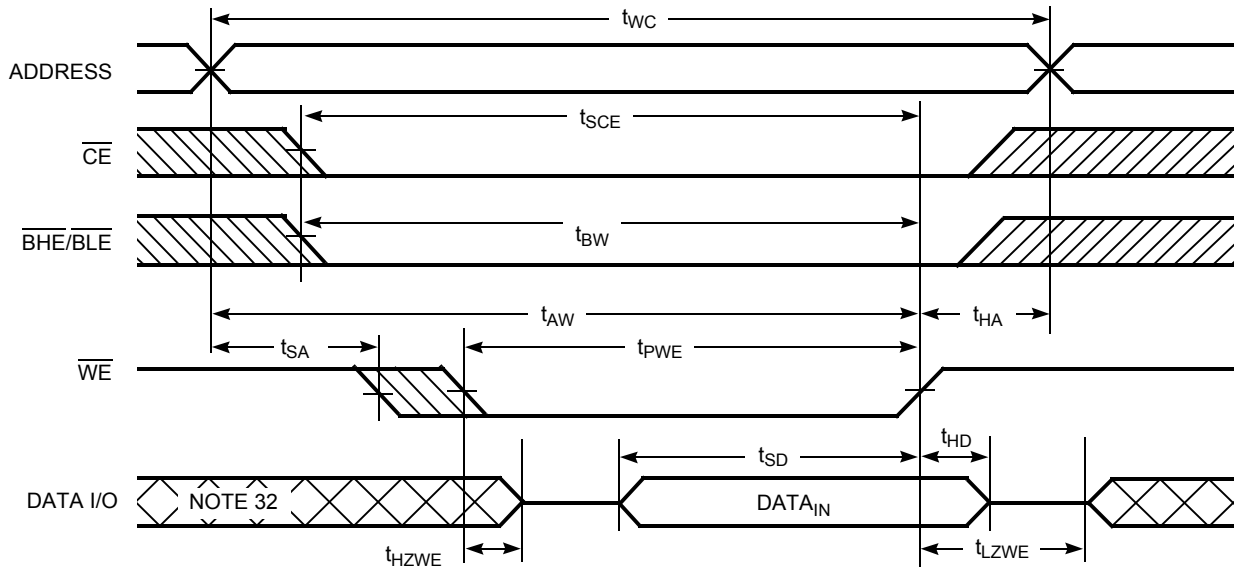


### Notes

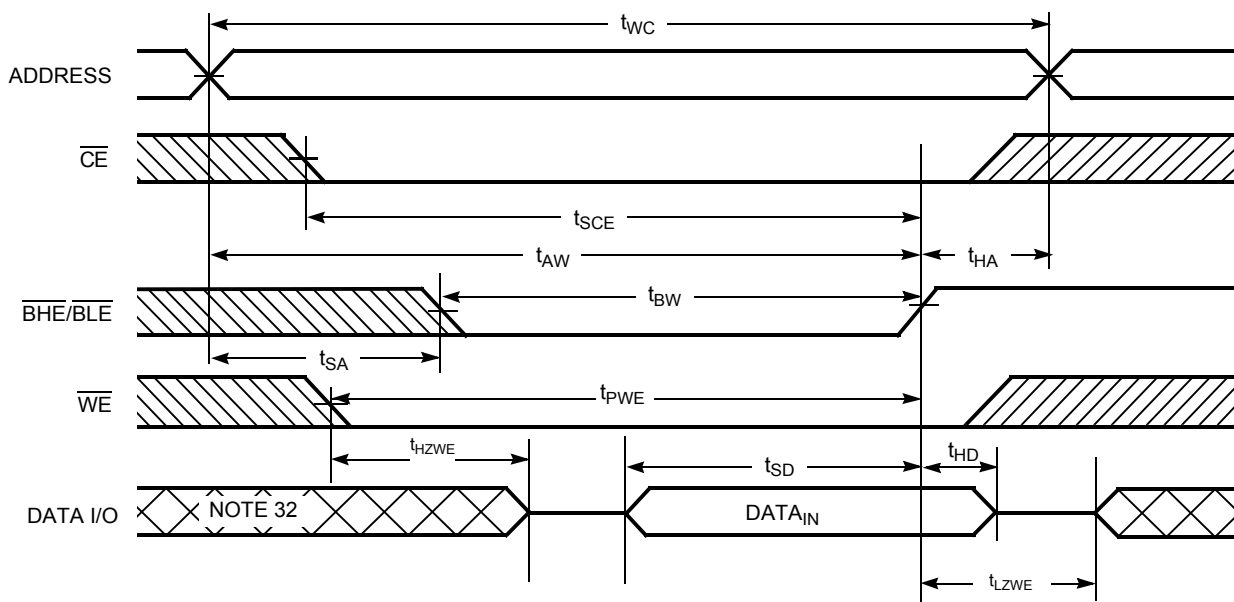
24.  $\overline{\text{CE}}$  refers to the internal logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$  such that when  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW. For all other cases  $\overline{\text{CE}}$  is HIGH.
25. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$ , or both =  $V_{\text{IL}}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
26. Data I/O is high impedance if  $\text{OE} = V_{\text{IH}}$ .
27. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}} = V_{\text{IH}}$ , the output remains in a high impedance state.
28. During this period, the I/Os are in output state. Do not apply input signals.

## Switching Waveforms (continued)

**Figure 8. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)** [29, 30, 31]



**Figure 9. Write Cycle No. 4 ( $\overline{BHE/BLER}$  Controlled,  $\overline{OE}$  LOW)** [29, 30]



### Notes

29.  $\overline{CE}$  refers to the internal logical combination of  $\overline{CE}_1$  and  $CE_2$  such that when  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW. For all other cases  $\overline{CE}$  is HIGH.

30. If  $\overline{CE}$  goes HIGH simultaneously with  $WE = V_{IH}$ , the output remains in a high impedance state.

31. The minimum write cycle pulse width should be equal to the sum of  $t_{HZWE}$  and  $t_{SD}$ .

32. During this period, the I/Os are in output state. Do not apply input signals.

## Truth Table

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	I/Os	Mode	Power
H	X <sup>[33]</sup>	X	X	X	X	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
X <sup>[33]</sup>	L	X	X	X	X	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
X <sup>[33]</sup>	X <sup>[33]</sup>	X	X	H	H	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	H	L	L	L	Data out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	H	L	Data out ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Read	Active ( $I_{CC}$ )
L	H	H	L	L	H	Data out ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Read	Active ( $I_{CC}$ )
L	H	H	H	L	L	High Z	Output disabled	Active ( $I_{CC}$ )
L	H	H	H	H	L	High Z	Output disabled	Active ( $I_{CC}$ )
L	H	H	H	L	H	High Z	Output disabled	Active ( $I_{CC}$ )
L	H	L	X	L	L	Data in ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	H	L	Data in ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Write	Active ( $I_{CC}$ )
L	H	L	X	L	H	Data in ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Write	Active ( $I_{CC}$ )

### Note

33. The 'X' (Don't care) state for the chip enables ( $\overline{CE}_1$  and  $CE_2$ ) in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

## Ordering Information

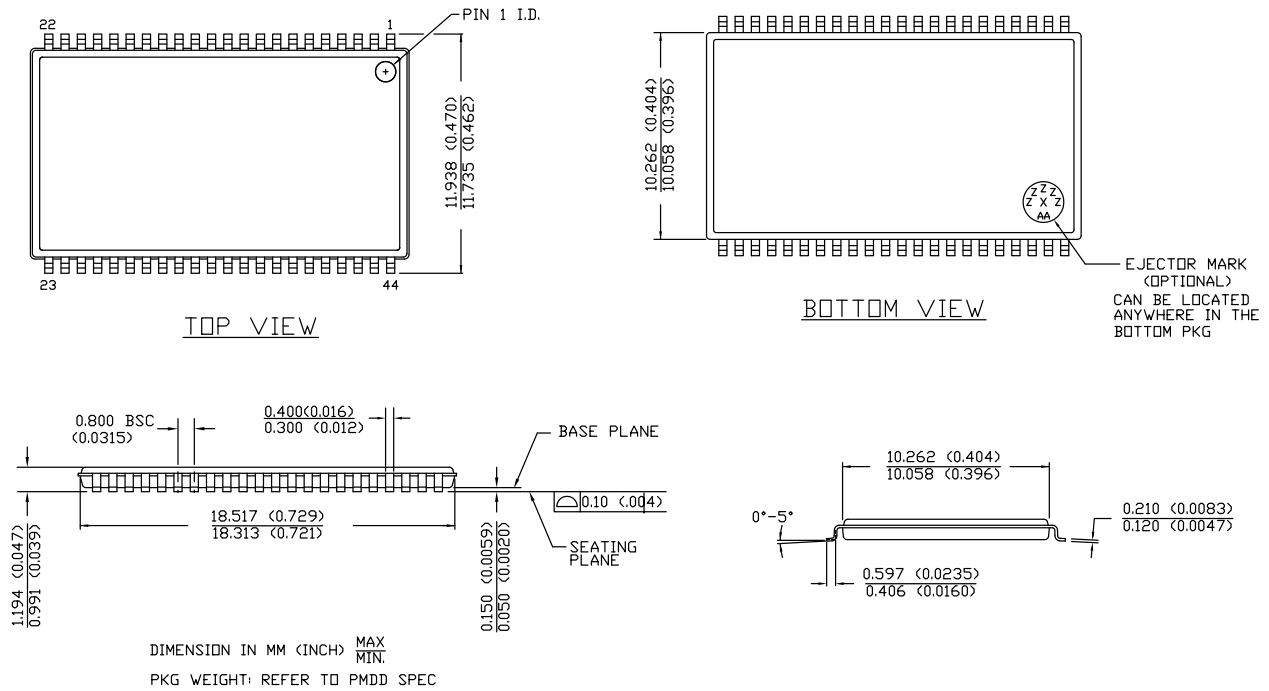
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY621472E30LL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	Industrial

## Ordering Code Definitions

CY	621	4	7	2	E	30	LL	-	45	ZS	X	I	
													Temperature Range: I = Industrial
													Pb-free
													Package Type: ZS = 44-pin TSOP II
													Speed Grade: 45 = 45 ns
													Low Power
													Voltage Range: 30 = 3 V Typical
													Process Technology: E = 90 nm
													Dual Chip Enable
													Bus Width: 7 = × 16
													Density: 4 = 4-Mbit
													Family Code: 621 = MoBL SRAM family
													Company ID: CY = Cypress

## Package Diagram

Figure 10. 44-pin TSOP II Package Outline, 51-85087



51-85087 \*E

## Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
OE	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
WE	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY621472E30 MoBL®, 4-Mbit (256 K × 16) Static RAM Document Number: 001-67798				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	3184883	RAME	03/01/2011	New data sheet.
*A	3223503	RAME	04/15/2011	Overline bar CE <sub>2</sub> removed from the Truth table. Updated all notes as per template.
*B	3261142	RAME	05/19/2011	Updated <a href="#">Switching Characteristics</a> (corrected the Min value of t <sub>LZBE</sub> parameter). Added <a href="#">Ordering Information</a> and <a href="#">Ordering Code Definitions</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> .
*C	3365953	AJU	09/08/2011	Changed datasheet status from Preliminary to Final. Updated 44-pin TSOP II package spec.
*D	3414567	TAVA	10/20/2011	Replaced CY62147EV30 with CY621472E30 through out the data sheet.
*E	4331825	NILE	04/03/2014	Updated <a href="#">Switching Characteristics</a> : Added Note 19 and referred the same note in "Write Cycle".  Updated <a href="#">Switching Waveforms</a> : Added Note 31 and referred the same note in <a href="#">Figure 8</a> .  Updated <a href="#">Package Diagram</a> : spec 51-85087 – Changed revision from *D to *E.  Updated in new template.  Completing Sunset Review.

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