

LM3702/LM3703 Microprocessor Supervisory Circuits with Low Line Output and Manual Reset

Check for Samples: [LM3702](#), [LM3703](#)

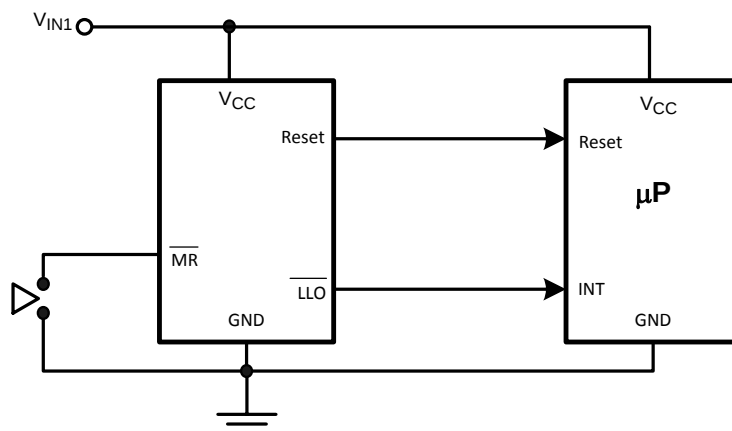
FEATURES

- **Standard Reset Threshold Voltage: 3.08V**
- **Custom Reset Threshold Voltages: For Other Voltages Between 2.2V and 5.0V in 10mV Increments, Contact Texas Instruments.**
- **No External Components Required**
- **Manual-Reset Input**
- **$\overline{\text{RESET}}$ (LM3702) or $\overline{\text{RESET}}$ (LM3703) Outputs**
- **Precision Supply Voltage Monitor**
- **Factory Programmable Reset Timeout Delay**
- **Available in DSBGA Package for Minimum Footprint**
- **$\pm 0.5\%$ Reset Threshold Accuracy at Room Temperature**
- **$\pm 2\%$ Reset Threshold Accuracy Over Temperature Extremes**
- **Reset Assertion Down to 1V V_{CC} ($\overline{\text{RESET}}$ Option Only)**
- **28 μA V_{CC} Supply Current**

APPLICATIONS

- **Embedded Controllers and Processors**
- **Intelligent Instruments**
- **Automotive Systems**
- **Critical μP Power Monitoring**

Typical Application

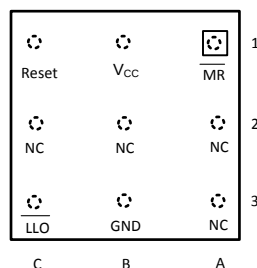


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Connection Diagram

Figure 1.



**Figure 2. Top View
(looking from the coating side)
DSBGA 9 Bump Package**

PIN DESCRIPTIONS

Bump No.	Name	Function
A1	$\overline{\text{MR}}$	Manual-Reset input. When $\overline{\text{MR}}$ is less than V_{MRT} (Manual Reset Threshold) $\overline{\text{RESET}}$ /RESET is engaged.
B1	V_{CC}	Power Supply input.
C1	$\overline{\text{RESET}}$	Reset Logic Output. Pulses low for t_{RP} (Reset Timeout Period) when triggered, and stays low whenever V_{CC} is below the reset threshold or when MR is below V_{MRT} . It remains low for t_{RP} after either V_{CC} rises above the reset threshold, or after MR input rises above V_{MRT} (LM3702 only).
	RESET	Reset Logic Output. RESET is the inverse of $\overline{\text{RESET}}$ (LM3703 only).
C3	$\overline{\text{LLO}}$	Low-Line Logic Output. Early Power-Fail warning output. Low when V_{CC} falls below V_{LLOT} (Low-Line Output Threshold). This output can be used to generate an NMI (Non-Maskable Interrupt) to provide an early warning of imminent power-failure.
B3	GND	Ground reference for all signals.
A2, A3, C2	NC	No Connect.
B2	NC	No Connect. Test input used at factory only. Leave floating.

Block Diagram

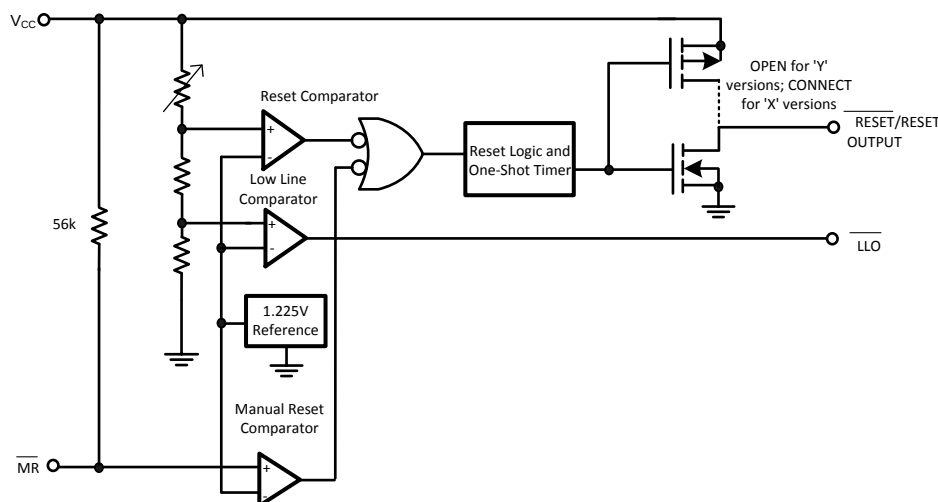


Table 1. Table Of Functions

Part Number	Active Low Reset	Active High Reset	Output (X = totem-pole) (Y = open-drain)	Reset Timeout Period	Manual Reset	Low Line Output
LM3702	x		X, Y ⁽¹⁾	Customized	x	x
LM3703		x	X	Customized	x	x

(1) = available upon request. Contact TI



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

Supply Voltage (V _{CC})		–0.3V to 6.0V
All Other Inputs		–0.3V to V _{CC} + 0.3V
ESD Ratings ⁽³⁾	Human Body Model	1.5kV
	Machine Model	150V
Power Dissipation		See ⁽⁴⁾

(1) **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. **Operating Ratings** indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed conditions.

(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

(3) The Human Body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

(4) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{J-A}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using:

$$P(MAX) = \frac{T_J(MAX) - T_A}{\theta_{J-A}}$$

Where the value of θ_{J-A} for the DSBGA package is 220°C/W.

OPERATING RATINGS⁽¹⁾

Temperature Range	–40°C ≤ T _J ≤ 85°C
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(1) **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. **Operating Ratings** indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed conditions.

LM3702/LM3703 SERIES ELECTRICAL CHARACTERISTICS

Limits in the standard typeface are for T_J = 25°C and limits in **boldface type** apply over full operating range. Unless otherwise specified: V_{CC} = +2.2V to 5.5V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V _{CC}	Operating Voltage Range: V _{CC}	LM3702	1.0		5.5	V
		LM3703	1.2		5.5	
I _{CC}	V _{CC} Supply Current	All inputs = V _{CC} ; all outputs floating		28	50	μA
RESET THRESHOLD						
V _{RST}	Reset Threshold	V _{CC} falling	–0.5 –2	V _{RST}	+0.5 +2	%
		V _{CC} falling: T _A = 0°C to 70°C	–1.5		+1.5	
V _{RSTH}	Reset Threshold Hysteresis			0.0032•V _{RST}		mV
t _{RP}	Reset Timeout Period	Reset Timeout Period = A Reset Timeout Period = B Reset Timeout Period = C Reset Timeout Period = D	1 20 140 1120	1.4 28 200 1600	2 40 280 2240	ms
t _{RD}	V _{CC} to Reset Delay	V _{CC} falling at 1mV/μs		20		μs

LM3702/LM3703 SERIES ELECTRICAL CHARACTERISTICS (continued)

Limits in the standard typeface are for $T_J = 25^\circ\text{C}$ and limits in **boldface type** apply over full operating range. Unless otherwise specified: $V_{CC} = +2.2\text{V}$ to 5.5V .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RESET (LM3703)						
V _{OL}	RESET	V _{CC} > 2.25V, I _{SINK} = 900μA			0.3	V
		V _{CC} > 2.7V, I _{SINK} = 1.2mA			0.3	
		V _{CC} > 4.5V, I _{SINK} = 3.2mA			0.4	
V _{OH}	RESET	V _{CC} > 1.2V, I _{SOURCE} = 50μA	0.8 V _{CC}			V
		V _{CC} > 1.8V, I _{SOURCE} = 150μA	0.8 V _{CC}			
		V _{CC} > 2.25V, I _{SOURCE} = 300μA	0.8 V _{CC}			
		V _{CC} > 2.7V, I _{SOURCE} = 500μA	0.8 V _{CC}			
		V _{CC} > 4.5V, I _{SOURCE} = 800μA	V _{CC} - 1.5V			
I _{LKG}	Output Leakage Current	V _{RESET} = 5.5V			1.0	μA
RESET (LM3702)						
V _{OL}	RESET	V _{CC} > 1.0V, I _{SINK} = 50μA			0.3	V
		V _{CC} > 1.2V, I _{SINK} = 100μA			0.3	
		V _{CC} > 2.25V, I _{SINK} = 900μA			0.3	
		V _{CC} > 2.7V, I _{SINK} = 1.2mA			0.3	
		V _{CC} > 4.5V, I _{SINK} = 3.2mA			0.4	
V _{OH}	RESET	V _{CC} > 2.25V, I _{SOURCE} = 300μA	0.8 V _{CC}			V
		V _{CC} > 2.7V, I _{SOURCE} = 500μA	0.8 V _{CC}			
		V _{CC} > 4.5V, I _{SOURCE} = 800μA	V _{CC} - 1.5V			
MR						
V _{MRT}	MR Input Threshold	MR, Low			0.8	V
		MR, High	2.0			
V _{MRTH}	MR Threshold Hysteresis	MR falling: V _{CC} = V _{RST MAX} to 5.5V		0.0032•V _{RST}		mV
R _{MR}	MR Pull-up Resistance		35	56	75	kΩ
t _{MD}	MR to Reset Delay			12		μS
t _{MR}	MR Pulse Width		25			μS
LLO						
V _{OL}	LLO Output Voltage	V _{CC} > 2.25V, I _{SINK} = 900μA			0.3	V
		V _{CC} > 2.7V, I _{SINK} = 1.2mA			0.3	
		V _{CC} > 4.5V, I _{SINK} = 3.2mA			0.4	
V _{OH}		V _{CC} > 2.25V, I _{SOURCE} = 300μA	0.8 V _{CC}			V
		V _{CC} > 2.7V, I _{SOURCE} = 500μA	0.8 V _{CC}			
		V _{CC} > 4.5V, I _{SOURCE} = 800μA	V _{CC} - 1.5V			
LLO OUTPUT						
V _{LLOT}	LLO Output Threshold (V _{LLO} - V _{RST} , V _{CC} falling)		1.01•V _{RST}	1.02•V _{RST}	1.03•V _{RST}	V
V _{LLOTH}	Low-Line Comparator Hysteresis			0.0032•V _{RST}		mV
t _{CD}	Low-Line Comparator Delay	V _{CC} falling at 1mV/μs		20		μs

TYPICAL PERFORMANCE CHARACTERISTICS

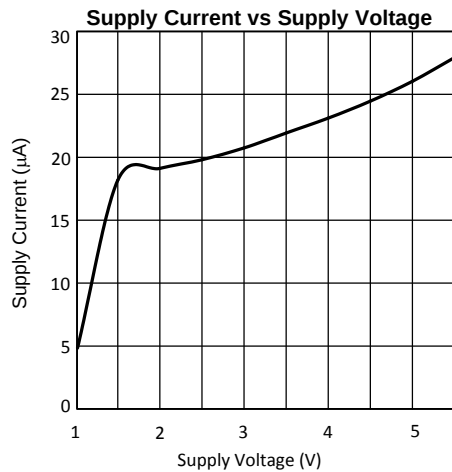


Figure 3.

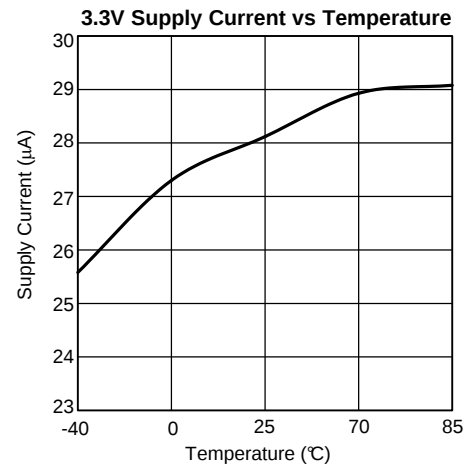


Figure 4.

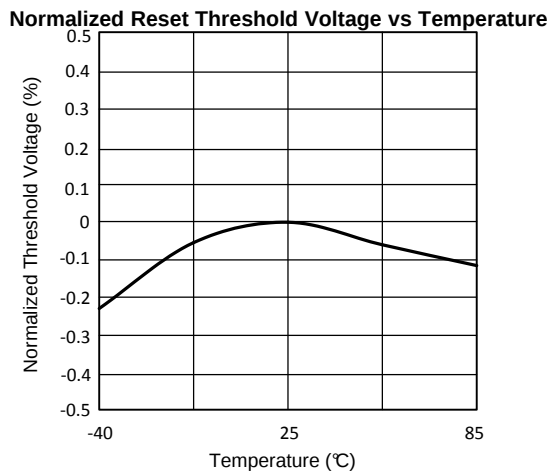


Figure 5.

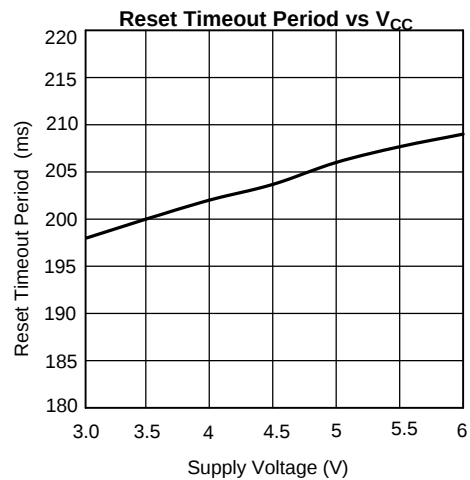


Figure 6.

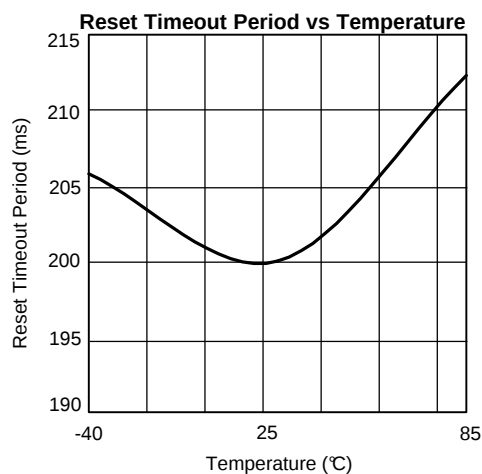


Figure 7.

**Max. Transient Duration vs Reset Comparator Overdrive
($V_{CC} = 3.3V$)**

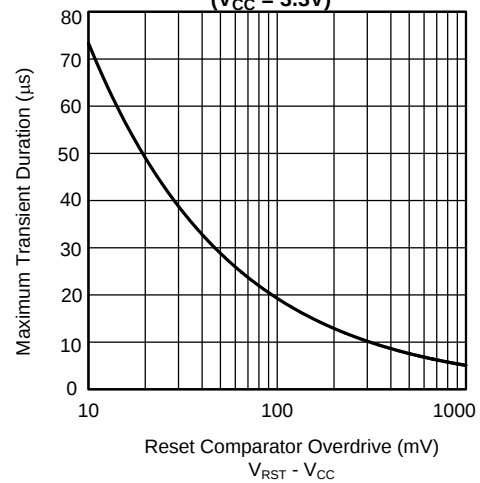
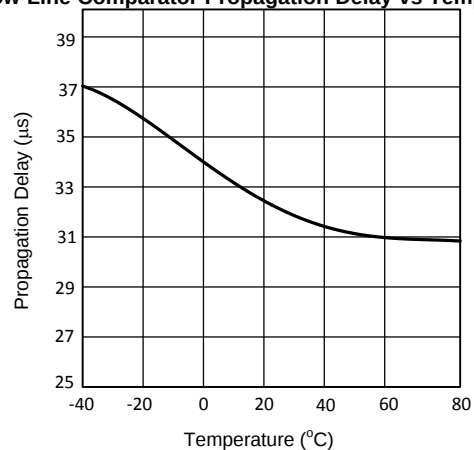


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)**Low-Line Comparator Propagation Delay vs Temperature****Figure 9.**

CIRCUIT INFORMATION

RESET OUTPUT

The Reset input of a μP initializes the device into a known state. The LM3702/LM3703 microprocessor supervisory circuits assert a forced reset output to prevent code execution errors during power-up, power-down, and brownout conditions.

$\overline{\text{RESET}}$ is ensured valid for $V_{\text{CC}} > 1\text{V}$. Once V_{CC} exceeds the reset threshold, an internal timer maintains the output for the reset timeout period. After this interval, reset goes high. The LM3702 offers an active-low $\overline{\text{RESET}}$; The LM3703 offers an active-high RESET.

Any time V_{CC} drops below the reset threshold (such as during a brownout), the reset activates. When V_{CC} again rises above the reset threshold, the internal timer starts. Reset holds until V_{CC} exceeds the reset threshold for longer than the reset timeout period. After this time, reset releases.

The Manual Reset input ($\overline{\text{MR}}$) will initiate a forced reset also. See the [MANUAL RESET INPUT \(\$\overline{\text{MR}}\$ \)](#) section.

RESET THRESHOLD

The LM3702/LM3703 family is available with a reset voltage of 3.08V. Other reset thresholds in the 2.20V to 5.0V range, in steps of 10 mV, are available; contact TI for details.

MANUAL RESET INPUT ($\overline{\text{MR}}$)

Many μP -based products require a manual reset capability, allowing the operator to initiate a reset. The $\overline{\text{MR}}$ input is fully debounced and provides an internal 56 k Ω pull-up. When the $\overline{\text{MR}}$ input is pulled below V_{MRT} (1.225V) for more than 25 μs , reset is asserted after a typical delay of 12 μs . Reset remains active as long as $\overline{\text{MR}}$ is held low, and releases after the reset timeout period expires after $\overline{\text{MR}}$ rises above V_{MRT} . Use $\overline{\text{MR}}$ with digital logic to assert or to daisy chain supervisory circuits. It may be used as another low-line comparator by adding a buffer.

LOW-LINE OUTPUT ($\overline{\text{LLO}}$)

The low-line output comparator is typically used to provide a non-maskable interrupt to a μP when V_{CC} begins falling. $\overline{\text{LLO}}$ monitors V_{CC} and goes low when V_{CC} falls below V_{LLOT} (typically $1.02 \cdot V_{\text{RST}}$) with hysteresis of $0.0032 \cdot V_{\text{RST}}$.

SPECIAL PRECAUTIONS FOR THE DSBGA PACKAGE

As with most integrated circuits, the LM3702 and LM3703 are sensitive to exposure from visible and infrared (IR) light radiation. Unlike a plastic encapsulated IC, the DSBGA package has very limited shielding from light, and some sensitivity to light reflected from the surface of the PC board or long wavelength IR entering the die from the side may be experienced. This light could have an unpredictable affect on the electrical performance of the IC. Care should be taken to shield the device from direct exposure to bright visible or IR light during operation.

DSBGA MOUNTING

The DSBGA package requires specific mounting techniques which are detailed in TI Application Note AN-1112 ([SNVA009](#)). Referring to the section **Surface Mount Technology (SMT) Assembly Considerations**, it should be noted that the pad style which must be used with the 9-pin package is the NSMD (non-solder mask defined) type.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

Timing Diagrams

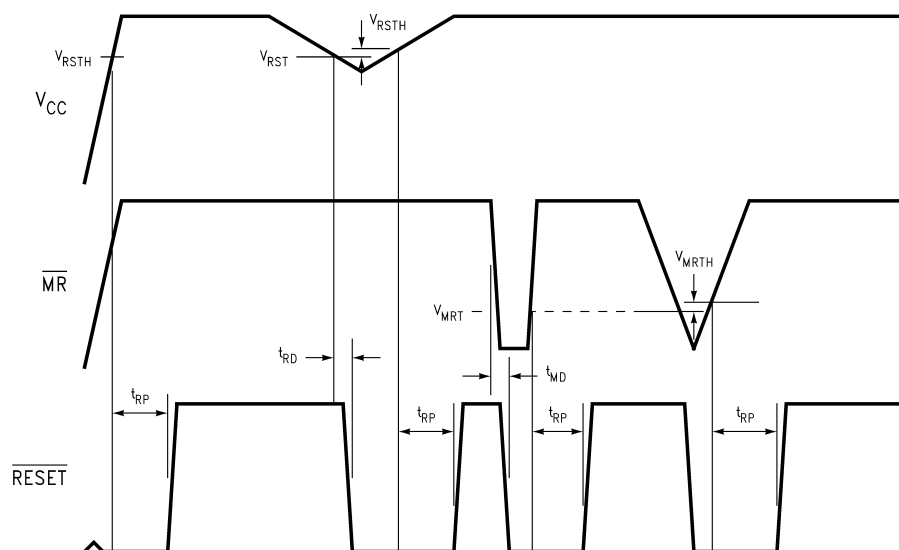


Figure 10. LM3702 Reset Time with $\overline{MR}$

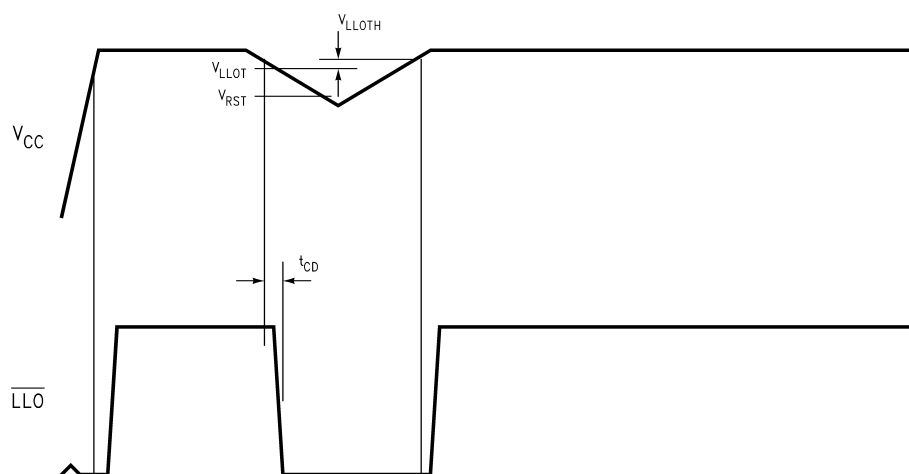


Figure 11. $\overline{LLO}$ Output

Typical Application Circuits

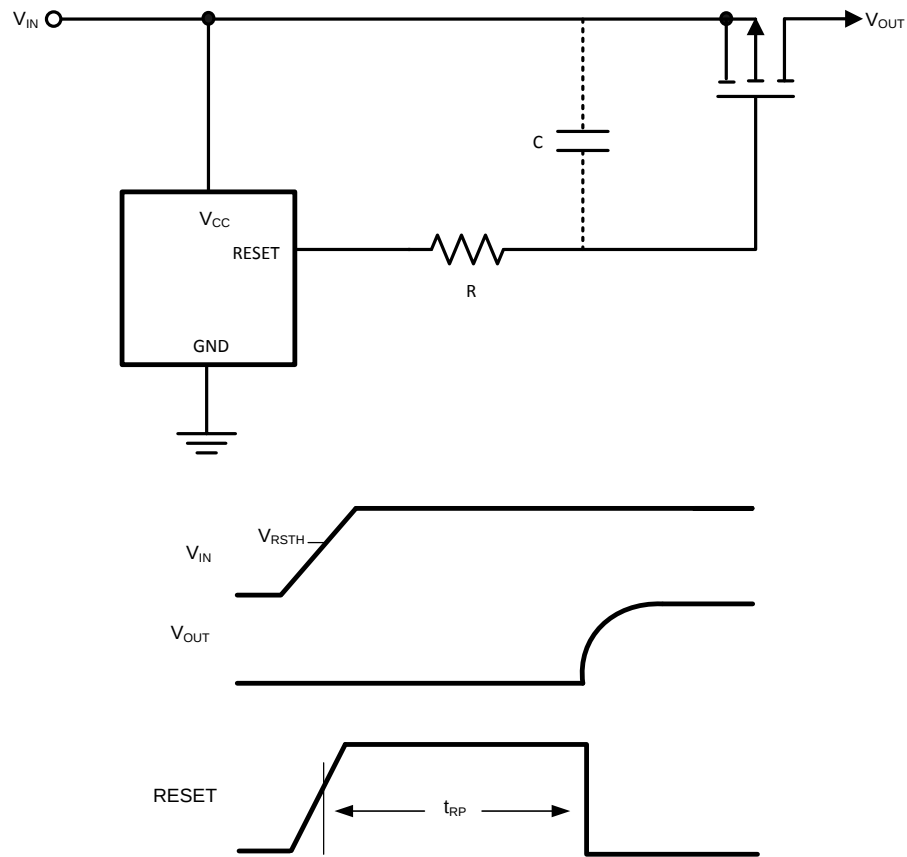


Figure 12. LM3703 Power-On Delay

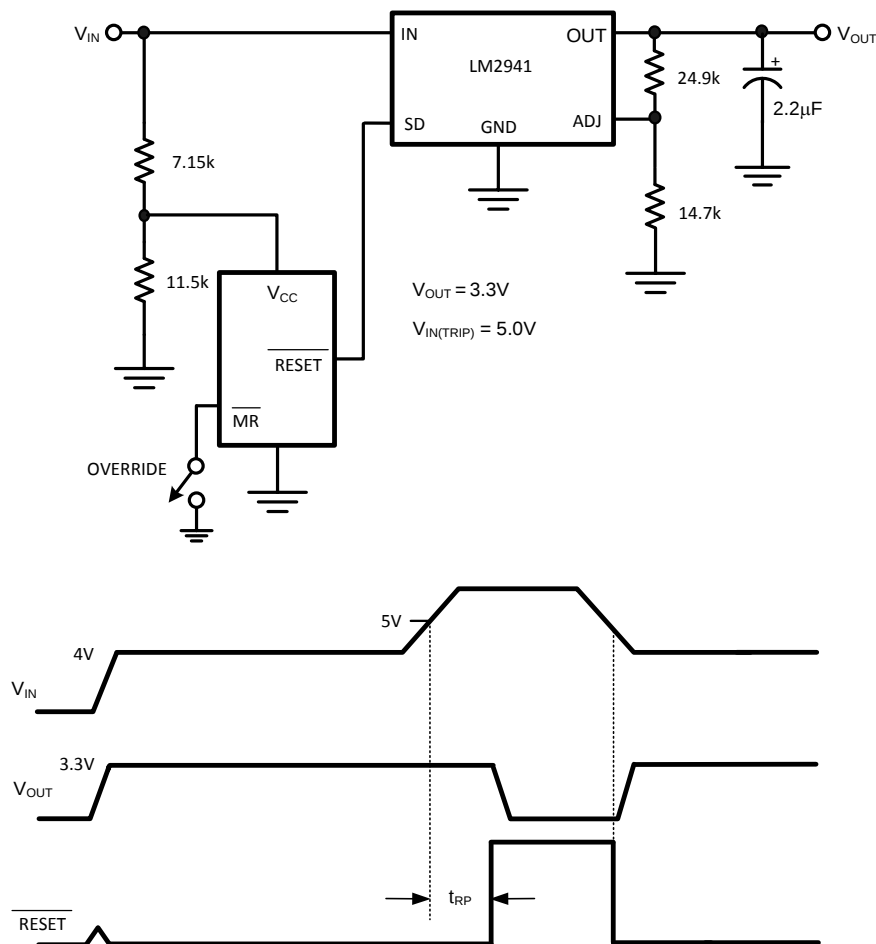


Figure 13. Regulator/Switch with Long-Term Overvoltage Lockout Prevents Overdissipation in Linear Regulator

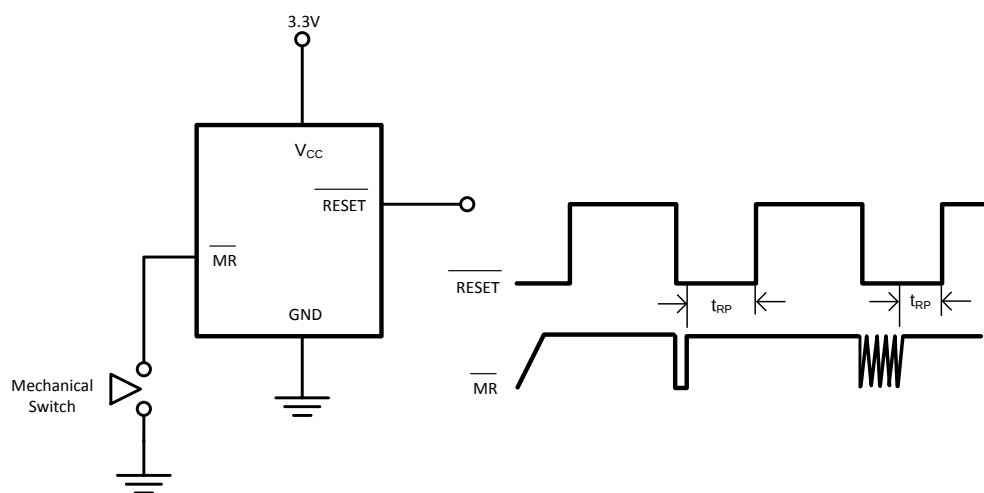


Figure 14. Switch Debouncer

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