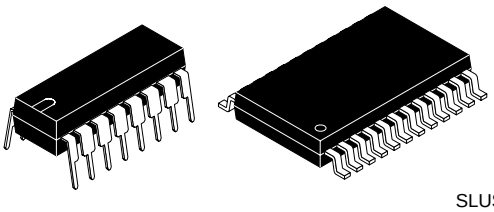


SLUS184A – FEBRUARY 1999 – REVISED OCTOBER 2001

15-V PROGRAMMABLE HOT SWAP POWER MANAGER

FEATURES

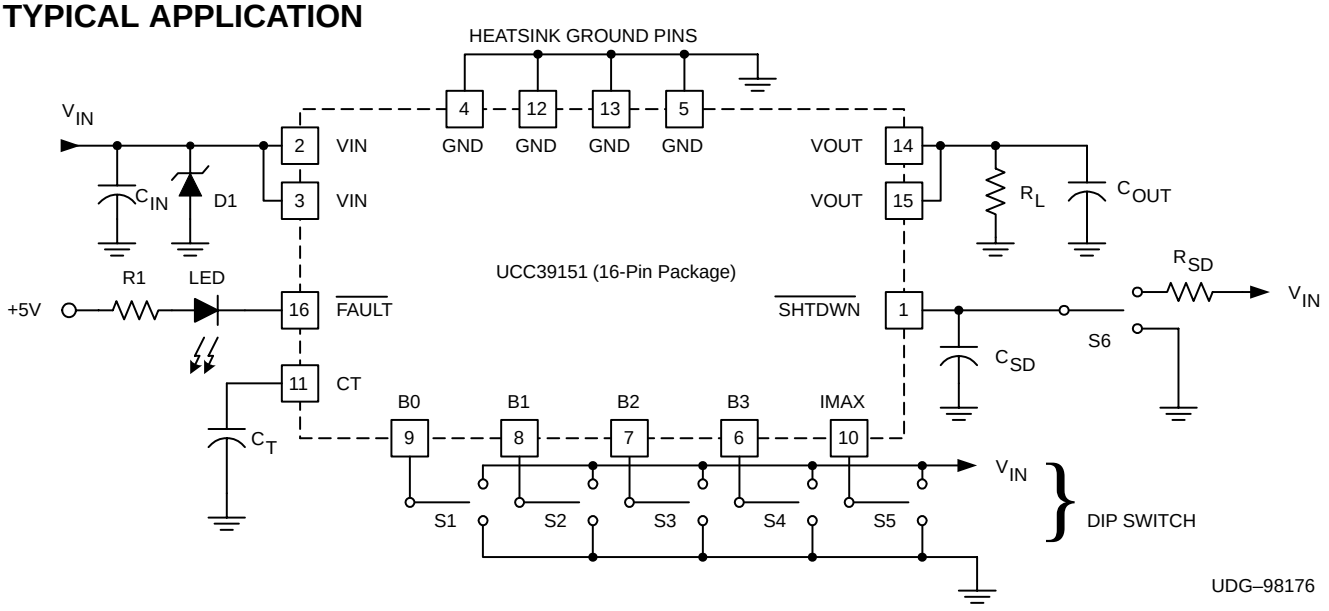
- **Integrated 0.15-Ω Power MOSFET**
- **7-V to 15-V Operation**
- **Digital Programmable Current Limit from 0 A to 3 A**
- **Programmable On-Time**
- **Programmable Start Delay**
- **Fixed 2% Duty Cycle**
- **Thermal Shutdown**
- **Fault Output Indicator**
- **Power SOIC and TSSOP, Low Thermal-Resistance Packaging**

DESCRIPTION

The UCC39151 programmable hot swap power manager provides complete power management, hot swap capability, and circuit breaker functions. The only external component required to operate the device, other than power supply bypassing, is the fault timing capacitor, C_T. All control and housekeeping functions are integrated, and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, and start-up delay. In the event of a constant fault, the internal fixed 2% duty cycle ratio limits average output power.

The internal 4-bit DAC allows programming of the fault level current from 0 A to 3 A with 0.25 A resolution. The IMAX control pin sets the maximum sourcing current to 1 A above the trip level or to a full 4 A of output current for fast output capacitor charging.

TYPICAL APPLICATION



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description (continued)

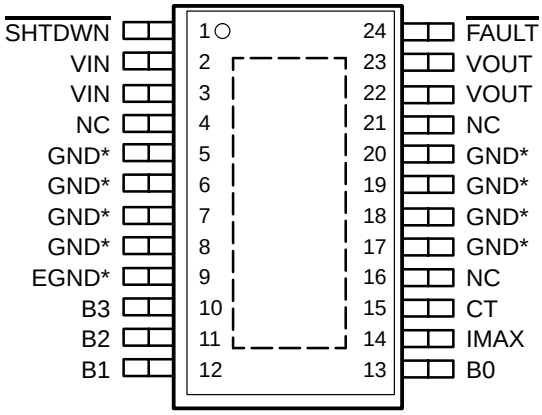
When the output current is below the fault level, the output MOSFET is switched on with a nominal on-resistance of 0.15 Ω. When the output current exceeds the fault level, but is less than the maximum sourcing level, the output remains switched on but the fault timer starts, charging C_T. Once C_T charges to a preset threshold, the switch is turned off, and remains off for 50 times the programmed fault time. When the output current reaches the maximum sourcing level, the MOSFET transitions from a switch to a constant current source.

absolute maximum ratings†

Input voltage, VIN . . . . . 15.5 V
(VOUT – VIN) . . . . . 0.3 V
$\overline{\text{FAULT}}$ sink current . . . . . 50 mA
$\overline{\text{FAULT}}$ voltage . . . . . –0.3 to 8 V
Output current, VOUT . . . . . Self limiting
TTL input voltage . . . . . –0.3 to V_{IN}
Storage temperature . . . . . –65°C to 150°C
Junction temperature . . . . . –55°C to 150°C
Lead temperature (soldering 10 seconds) 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Currents are positive into, negative out of the specified terminal.

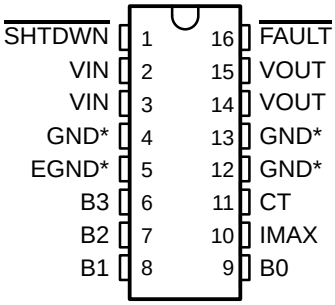
PWP PACKAGE
(TOP VIEW)



NC = no connection

DIL (N) or SOIC (DP) PACKAGE

(TOP VIEW)



* Pin 5 on the N and DP packages (and pin 9 on the PWP package) serves as the lowest impedance to the electrical ground. Pins 4, 12 and 13 on the DP package (and pins 5, 6, 7, 8, 17, 18, 19, and 20 on the PWP package) serve as heatsink/ground. These pins should be connected to large etch areas to help dissipate heat. On the N package, pins 4, 12 and 13 are not connected.

AVAILABLE OPTIONS

T_A	PACKAGES		
	SOIC (DP)†	DIL (N)	TSSOP (PWP)†
0°C to 70°C	UCC39151DP	UCC39151N	UCC39151PWP

† The DP and PWP packages are available taped and reeled. Add TR suffix to device type (e.g. UCC39151DPTR) to order quantities of 2500 (DP) or 2000 (PWP) devices per reel.

electrical characteristics over recommended operating virtual junction temperature range, T_A = 0°C to 70°C, VIN = 12 V, IMAX = 0.4 V, $\overline{SHTDWN}$ = 2.4 V, $T_A = T_J$ (unless otherwise noted)

supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage range		7.0		15.0	V
Supply current			1.0	2.0	mA
Sleep mode current	$\overline{SHTDWN}$ = 0.2 V, No load		100	150	µA
Output leakage	$\overline{SHTDWN}$ = 0.2 V			20	mA

output

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage drop	I_{OUT} = 1 A, 10 V ≤ VIN ≤ 12 V		0.15	0.3	V
	I_{OUT} = 2 A, 10 V ≤ VIN ≤ 12 V		0.3	0.6	
	I_{OUT} = 3 A, 10 V ≤ VIN ≤ 12 V		0.45	0.9	
	I_{OUT} = 1 A, 7 V ≤ VIN ≤ 15 V		0.2	0.4	
	I_{OUT} = 2 A,, 7 V ≤ VIN ≤ 15 V		0.4	0.8	
	I_{OUT} = 3 A, , 7 V ≤ VIN ≤ 12 V(max)		0.6	1.2	
Initial startup time	See Note 1		100		µs
Short circuit response time	See Note 1		100		ns
Thermal shutdown temperature	See Note 1		165		°C
Thermal hysteresis	See Note 1		10		

DAC

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Trip current	Code = 0000 to 0011, (device off)				A
	Code = 0100	0.07	0.25	0.45	
	Code = 0101	0.32	0.50	0.7	
	Code = 0110	0.50	0.75	0.98	
	Code = 0111	0.75	1.00	1.3	
	Code = 1000	1.0	1.25	1.6	
	Code = 1001	1.25	1.50	1.85	
	Code = 1010	1.5	1.75	2.15	
	Code = 1011	1.70	2.00	2.4	
	Code = 1100	1.90	2.25	2.7	
	Code = 1101	2.1	2.50	2.95	
	Code = 1110	2.30	2.75	3.25	
	Code = 1111	2.50	3.0	3.5	
Maximum output current over trip level (current source mode)	Code = 0100 to 1111, IMAX = 0 V	0.35	1.0	1.65	
Maximum output current (current source mode)	Code = 0100 to 1111, IMAX = 2.4 V	3.0	4.0	5.2	

open drain output ($\overline{FAULT}$)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
High-level output current	$\overline{FAULT}$ = 5 V			250	µA
Low-level output voltage	I_{OUT} = 5 mA		0.2	0.8	V

NOTE 1: Ensured by design. Not production tested.

electrical characteristics over recommended operating virtual junction temperature range, T_A = 0°C to 70°C, V_{IN} = 12 V, IMAX = 0.4 V, $\overline{SHTDWN}$ = 2.4 V, $T_A = T_J$ (unless otherwise noted)

fault timer

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CT charge current	V_{CT} = 1.0 V	–83	–62	–47	µA
CT discharge current	V_{CT} = 1.0 V	0.8	1.2	1.8	µA
Output duty cycle	V_{OUT} = 0 V	1.0%	1.9%	3.3%	
CT fault threshold voltage		1.2	1.5	1.7	V
CT reset threshold voltage		0.4	0.5	0.6	V

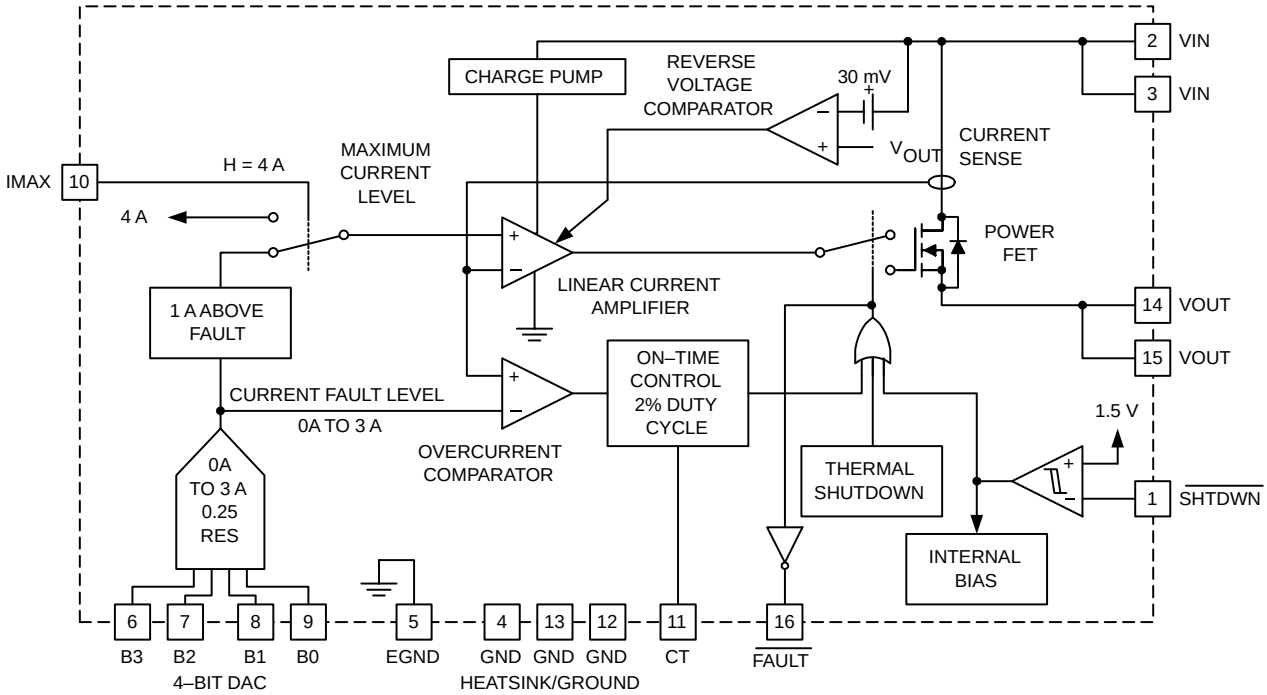
$\overline{SHTDWN}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Shutdown threshold voltage		1.1	1.5	1.9	V
Shutdown hysteresis			150		mV
Input current			100	500	nA

TTL input dc characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TTL high-level input voltage		2.0			V
TTL low-level input voltage				0.8	V
TTL high-level input current	V_{IH} = 2.4 V		3	10	µA
TTL low-level input current	V_{IL} = 0.4 V			1	µA

block diagram (16–pin package)



Pin numbers refer to N and DP packages.

UDG–01044

Terminal Functions

TERMINAL				I/O	DESCRIPTION
NAME	PACKAGE				
	DP	N	PWP		
B0	9	9	13	I	Provides digital input to the DAC, which sets the fault current threshold. These can be used to provide a digital soft-start and adaptive current limiting.
B1	8	8	12	I	
B2	7	7	11	I	
B3	6	6	10	I	
CT	11	11	15	I/O	Capacitor connects to ground and sets the maximum fault time.
EGND	5	5	9	–	Serves as lowest impedance to the electrical ground.
$\overline{\text{FAULT}}$	16	16	24	O	Open-drain output, which pulls low upon any fault or interrupt condition, or thermal shutdown.
GND	4, 12, 13	–	5, 6, 7, 8, 17, 18, 19, 20	–	Heat sink/ground pins. These pins should be connected to large etch areas to help dissipate heat.
IMAX	10	10	14	I	When this pin is set low, the maximum sourcing current is 1 A above the programmed fault level. When set high, the maximum sourcing current is a constant 4 A for applications which require fast charging of load capacitance.
$\overline{\text{SHTDWN}}$	1	1	1	I	When this pin is brought low, the device is put into a sleep mode drawing typically less than 100 μA of I_{CC} (with VOUT unloaded). The input threshold is hysteretic, allowing the user to program a start-up delay with an external RC circuit.
VIN	2, 3	2, 3	2, 3	I	Input voltage. The recommended voltage range is 7 V to 15 V. Both VIN pins should be connected together and connected to power source.
VOUT	14, 15	14, 15	22, 23	O	Output voltage.VOUT must not exceed VIN by more than 0.3 V.

detailed pin descriptions

CT: A capacitor connected to ground sets the maximum fault time. The maximum fault time must be more than the time required to charge the external capacitance in one cycle. The maximum fault time is defined as:

$$t_{FAULT} = 16.1 \times 10^3 \times C_T \quad (1)$$

Once the fault time is reached the output shuts down for a time given by:

$$t_{SD} = 833 \times 10^3 \times C_T \quad (2)$$

This equates to a 1.9% duty cycle.

VOUT: Output voltage from the UCC39151. Both VOUT pins should be connected together and connected to the load. When switched:

$$V_{OUT} \cong V_{IN} - \left(0.15\ \Omega \times I_{OUT}\right) \quad (3)$$

VOUT must not exceed VIN by more than 0.3V.

APPLICATION INFORMATION

protecting the UCC39151 from voltage transients

The parasitic inductance associated with the power distribution can cause a voltage spike at VIN if the load current is suddenly interrupted by the UCC39151. It is important to limit the peak of this spike to less than 15 V to prevent damage to the UCC39151. This voltage spike can be minimized by:

- Reducing the power distribution inductance (e.g., twist the positive (+) and negative (–) leads of the power supply feeding VIN, locate the power supply close to the UCC39151 or use PCB power and ground planes).
- Decoupling VIN with a capacitor, C_{IN} (refer to Typical Application diagram), located close to the VIN pins. This capacitor is typically 1 μF or less to limit the inrush current.
- Clamping the voltage at VIN below 15 V with a Zener diode, D1 (refer to Typical Application diagram), located close to the VIN pins.

estimating maximum load capacitance

For hot swap applications, the rate at which the total output capacitance can be charged depends on the maximum output current available and the nature of the load. For a constant-current, current-limited application, the output comes up if the load asks for less than the maximum available short-circuit current.

To guarantee recovery of a duty-cycle from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit on-time (fault-time). The design value of on-time or fault-time can be adjusted by changing the timing capacitor C_T.

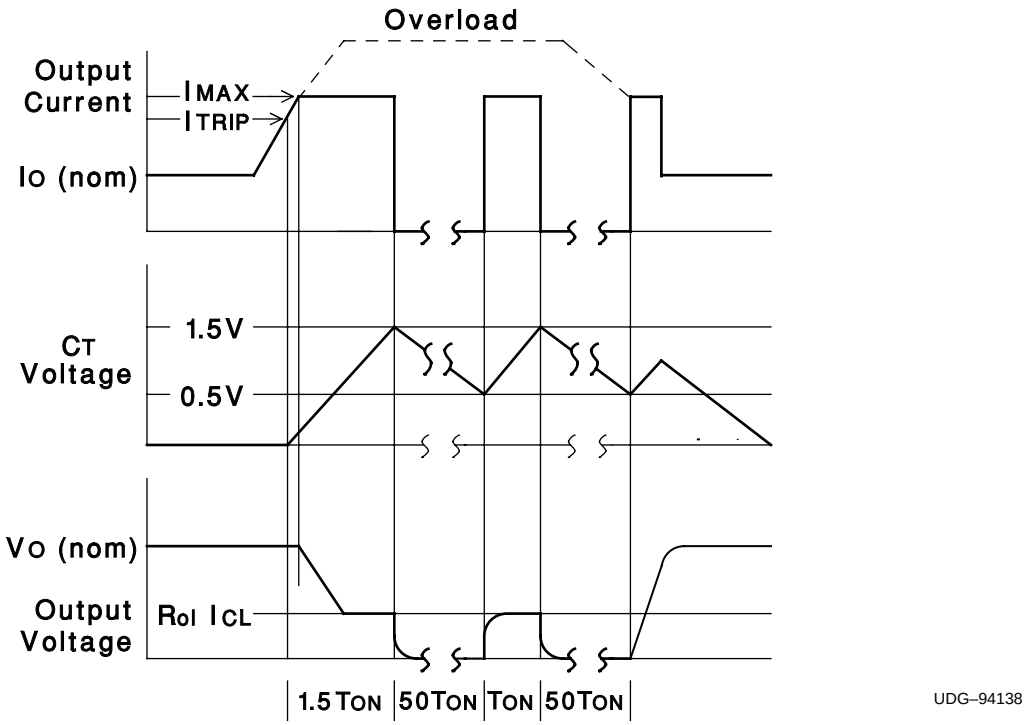


Figure 1. Output Waveforms Under Fault Conditions

APPLICATION INFORMATION

For worst-case constant-current load of value just less than the trip limit; $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} \approx \left(I_{MAX} - I_{LOAD}\right) \times \left(\frac{16.1 \times 10^3 \times C_T}{V_{OUT}}\right) \quad (4)$$

Where V_{OUT} is the output voltage.

For a resistive load of value R_L, the value of $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} \approx \left[\frac{16.1 \times 10^3 \times C_T}{R_L \times \ell n\left[\frac{1}{1 - \frac{V_{OUT}}{I_{MAX} \times R_L}}\right]}\right] \quad (5)$$

Long C_T times must consider the maximum temperature. Thermal shutdown protection may be the limiting fault-time.

safety recommendations

Although the UCC39151 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC39151 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC39151 prevents the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

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