

# FDG6332C\_F085

## 20V N & P-Channel PowerTrench® MOSFETs

### Features

- **Q1** 0.7 A, 20V.  $R_{DS(ON)} = 300 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$   
 $R_{DS(ON)} = 400 \text{ m}\Omega @ V_{GS} = 2.5 \text{ V}$
- **Q2** -0.6 A, -20V.  $R_{DS(ON)} = 420 \text{ m}\Omega @ V_{GS} = -4.5 \text{ V}$   
 $R_{DS(ON)} = 630 \text{ m}\Omega @ V_{GS} = -2.5 \text{ V}$
- Low gate charge
- High performance trench technology for extremely low  $R_{DS(ON)}$
- SC70-6 package: small footprint (51% smaller than SSOT-6); low profile (1mm thick)
- Qualified to AEC Q101
- RoHS Compliant



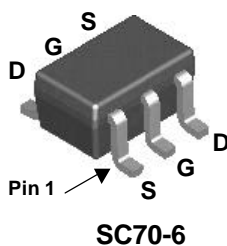
### General Description

The N & P-Channel MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

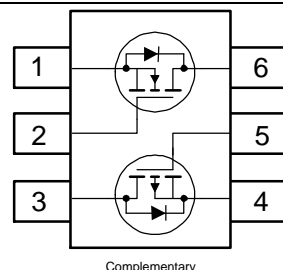
These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive TSSOP-8 and SSOP-6 packages are impractical.

### Applications

- DC/DC converter
- Load switch
- LCD display inverter



SC70-6



### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
$V_{DSS}$	Drain-Source Voltage	20	-20	V
$V_{GSS}$	Gate-Source Voltage	$\pm 12$	$\pm 12$	V
$I_D$	Drain Current – Continuous (Note 1)	0.7	-0.6	A
	– Pulsed	2.1	-2	
$P_D$	Power Dissipation for Single Operation (Note 1)	0.3		W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	415	$^\circ\text{C/W}$
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### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.32	FDG6332C_F085	7"	8mm	3000 units

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Off Characteristics							
BV <sub>DSS</sub>	Drain–Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA V <sub>GS</sub> = 0 V, I <sub>D</sub> = −250 μA	Q1 Q2	20 −20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Ref. to 25°C I <sub>D</sub> = −250 μA, Ref. to 25°C	Q1 Q2		14 −14		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 16 V, V <sub>GS</sub> = 0 V V <sub>DS</sub> = −16 V, V <sub>GS</sub> = 0 V	Q1 Q2			1 −1	μA
I <sub>GSSF</sub> / I <sub>GSSR</sub>	Gate–Body Leakage, Forward	V <sub>GS</sub> = ± 12 V, V <sub>DS</sub> = 0 V				±100	nA
I <sub>GSSF</sub> / I <sub>GSSR</sub>	Gate–Body Leakage, Reverse	V <sub>GS</sub> = ± 12V , V <sub>DS</sub> = 0 V				±100	nA
On Characteristics (Note 2)							
V <sub>GS(th)</sub>	Gate Threshold Voltage	Q1	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	0.6	1.1	1.5	V
		Q2	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = −250 μA	−0.6	−1.2	−1.5	
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	Q1 Q2	I <sub>D</sub> = 250 μA, Ref. To 25°C I <sub>D</sub> = −250 μA, Ref. to 25°C		−2.8 3		mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	Q1	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 0.7 A V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 0.6 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 0.7 A, T <sub>J</sub> = 125°C		180 293 247	300 400 442	mΩ
		Q2	V <sub>GS</sub> = −4.5 V, I <sub>D</sub> = −0.6 A V <sub>GS</sub> = −2.5 V, I <sub>D</sub> = −0.5 A V <sub>GS</sub> = −4.5 V, I <sub>D</sub> = −0.6 A, T <sub>J</sub> = 125°C		300 470 400	420 630 700	
g <sub>FS</sub>	Forward Transconductance	Q1	V <sub>DS</sub> = 5 V I <sub>D</sub> = 0.7 A		2.8		S
		Q2	V <sub>DS</sub> = −5 V I <sub>D</sub> = −0.6 A		1.8		
I <sub>D(on)</sub>	On–State Drain Current	Q1	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 5 V	1			A
		Q2	V <sub>GS</sub> = −4.5 V, V <sub>DS</sub> = −5 V	−2			
Dynamic Characteristics							
C <sub>iss</sub>	Input Capacitance	Q1	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		113		pF
		Q2	V <sub>DS</sub> = −10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		114		
C <sub>oss</sub>	Output Capacitance	Q1	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		34		pF
		Q2	V <sub>DS</sub> = −10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		24		
C <sub>rss</sub>	Reverse Transfer Capacitance	Q1	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		16		pF
		Q2	V <sub>DS</sub> = −10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		9		
Switching Characteristics (Note 2)							
t <sub>d(on)</sub>	Turn–On Delay Time	Q1 Q2	For Q1: V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 A V <sub>GS</sub> = 4.5 V, R <sub>GEN</sub> = 6 Ω		5 5.5	10 11	ns
t <sub>r</sub>	Turn–On Rise Time	Q1 Q2	For Q1: V <sub>GS</sub> = 4.5 V, R <sub>GEN</sub> = 6 Ω For Q2: V <sub>DS</sub> = −10 V, I <sub>D</sub> = −1 A V <sub>GS</sub> = −4.5 V, R <sub>GEN</sub> = 6 Ω		7 14	15 25	ns
t <sub>d(off)</sub>	Turn–Off Delay Time	Q1 Q2			9 6	18 12	ns
t <sub>f</sub>	Turn–Off Fall Time	Q1 Q2			1.5 1.7	3 3.4	ns
Q <sub>g</sub>	Total Gate Charge	Q1 Q2	For Q1: V <sub>DS</sub> = 10 V, I <sub>D</sub> = 0.7 A V <sub>GS</sub> = 4.5 V, R <sub>GEN</sub> = 6 Ω		1.1 1.4	1.5 2	nC
		Q1 Q2	For Q2: V <sub>DS</sub> = −10 V, I <sub>D</sub> = −0.6 A V <sub>GS</sub> = −4.5 V, R <sub>GEN</sub> = 6 Ω		0.24 0.3		
Q <sub>gs</sub>	Gate–Source Charge	Q1 Q2			0.3 0.3		nC
		Q1 Q2			0.3 0.4		

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Drain–Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain–Source Diode Forward Current	<b>Q1</b>			0.25	A
		<b>Q2</b>			–0.25	
$V_{SD}$	Drain–Source Diode Forward Voltage	<b>Q1</b>	$V_{GS} = 0\text{ V}, I_S = 0.25\text{ A}$ (Note 2)	0.74	1.2	V
		<b>Q2</b>	$V_{GS} = 0\text{ V}, I_S = -0.25\text{ A}$ (Note 2)	–0.77	–1.2	

**Notes:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.  $R_{\theta JA} = 415^\circ\text{C/W}$  when mounted on a minimum pad of FR-4 PCB in a still air environment.

2. Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

## Typical Characteristics: N-Channel

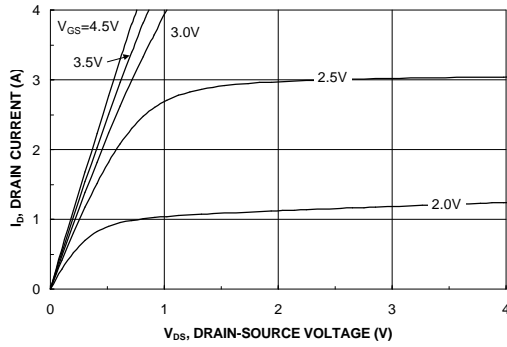


Figure 1. On-Region Characteristics.

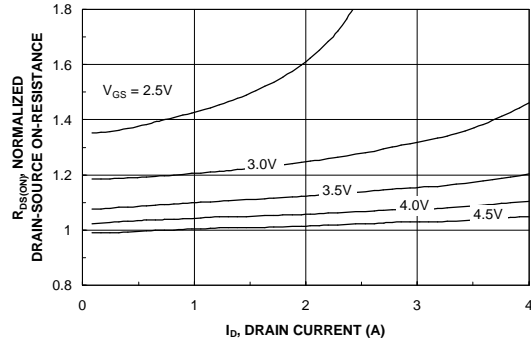


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

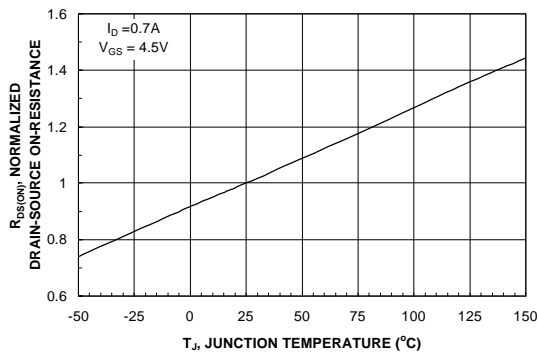


Figure 3. On-Resistance Variation with Temperature.

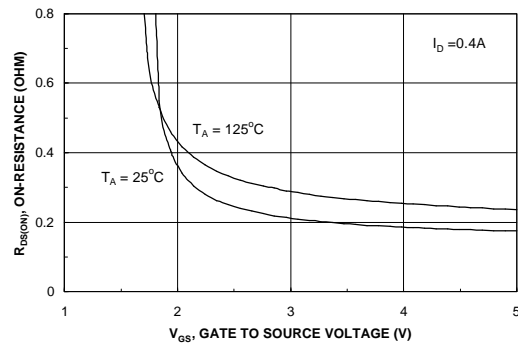


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

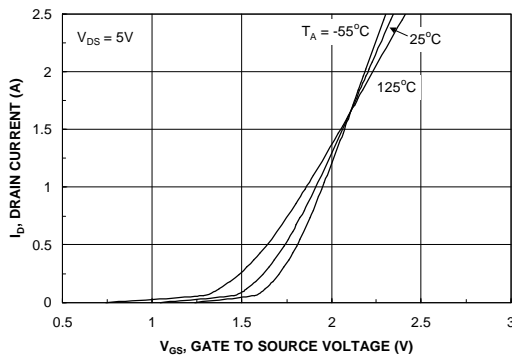


Figure 5. Transfer Characteristics.

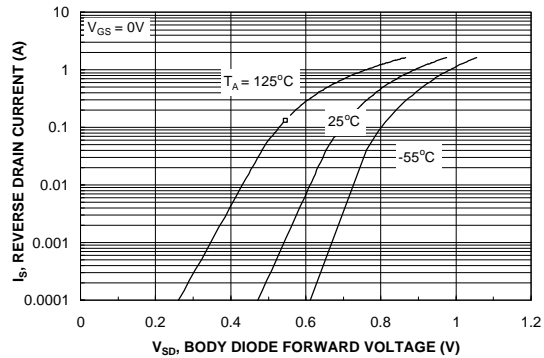


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Characteristics: N-Channel

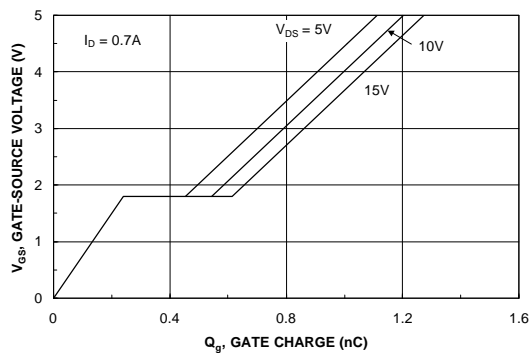


Figure 7. Gate Charge Characteristics.

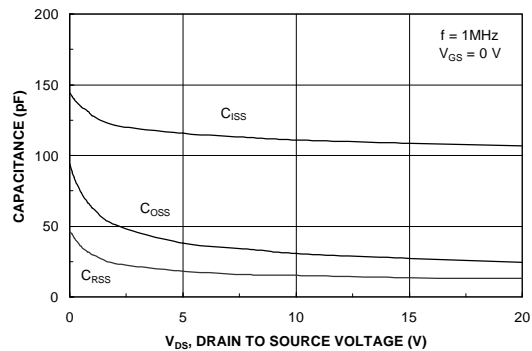


Figure 8. Capacitance Characteristics.

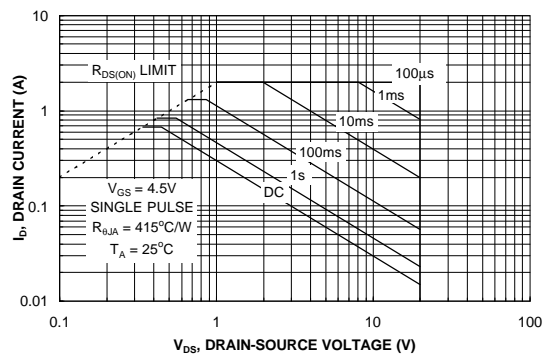


Figure 9. Maximum Safe Operating Area.

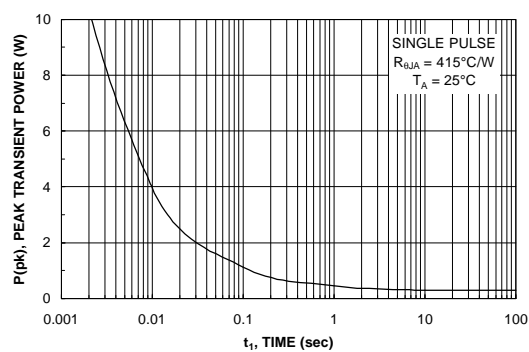


Figure 10. Single Pulse Maximum Power Dissipation.

## Typical Characteristics: P-Channel

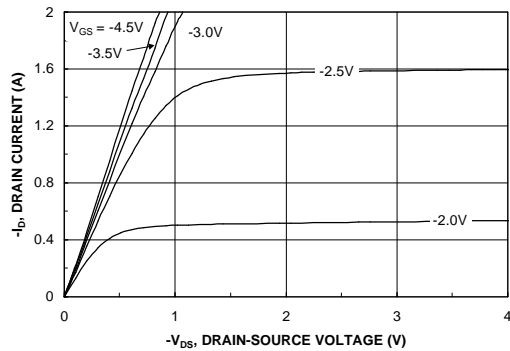


Figure 11. On-Region Characteristics.

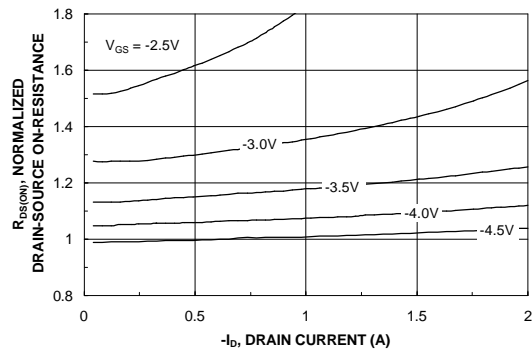


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

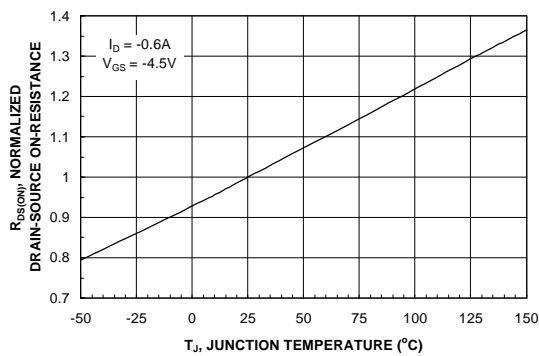


Figure 13. On-Resistance Variation with Temperature.

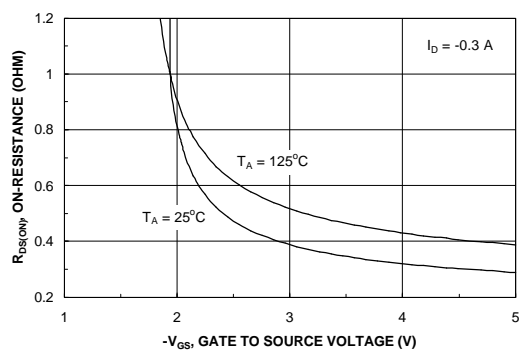


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

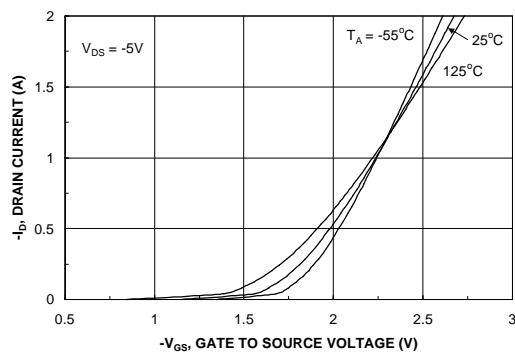


Figure 15. Transfer Characteristics.

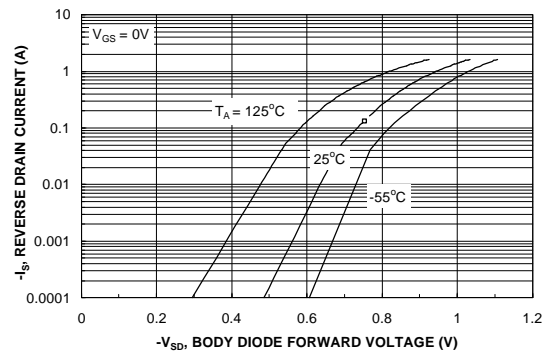


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Characteristics: P-Channel

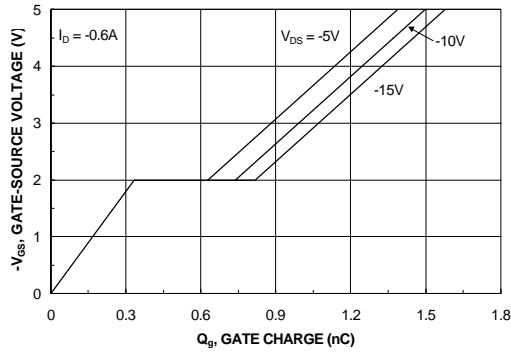


Figure 17. Gate Charge Characteristics.

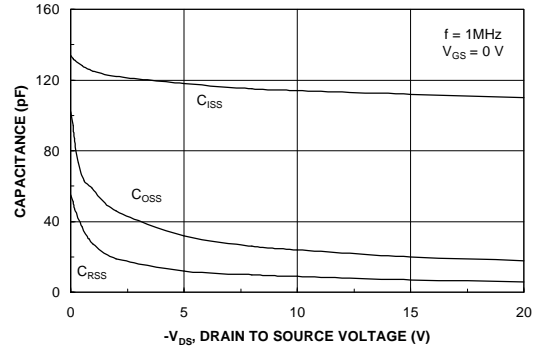


Figure 18. Capacitance Characteristics.

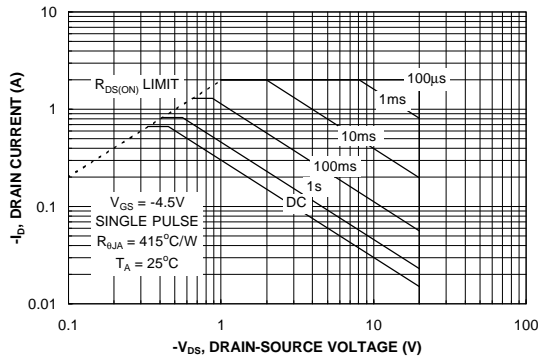


Figure 19. Maximum Safe Operating Area.

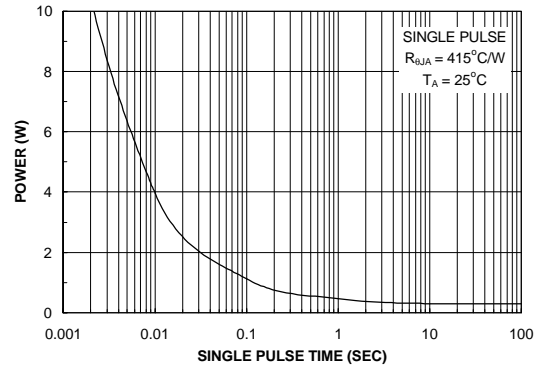


Figure 20. Single Pulse Maximum Power Dissipation.

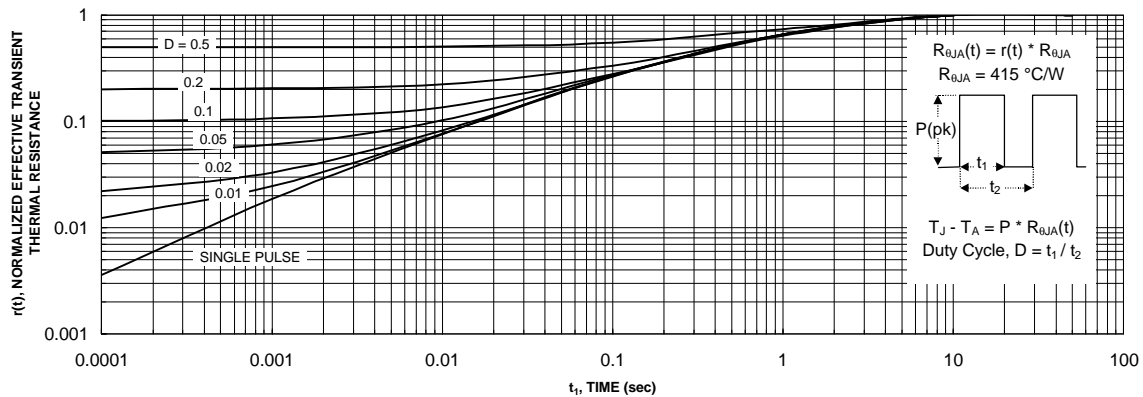







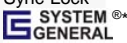
Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1.  
Transient thermal response will change depending on the circuit board design.



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