



SPE0514

4-Line ESD Protection Array

DESCRIPTION

The SPE0514 are designed by TVS array that is to protect sensitive electronics from damage or latch-up due to ESD. They are designed for use in applications where board space is at a premium. SPE0514 will protect up to four lines, and may be used on lines where the signal polarities swing above and below ground.

SPE0514 offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

SPE0514 may be used to meet the immunity requirements of IEC 61000-4-2, level 4. The small SOT-563 package makes them ideal for use in portable electronics such as cell phones, PDA's, notebook computers, and digital cameras.

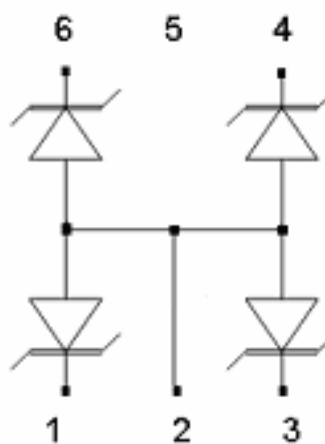
APPLICATIONS

- ◆ Cellular Handsets and Accessories
- ◆ Cordless Phone
- ◆ PDA
- ◆ Notebooks and Handhelds
- ◆ Portable Instrumentation
- ◆ Digital Cameras
- ◆ MP3 Player

FEATURES

- ◆ Transient protection for data lines to IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 8\text{kV}$ (contact)
IEC 61000-4-4 (EFT) 40A (5/50ns)
- ◆ Protects four I/O lines
- ◆ Working voltage: 5V
- ◆ Low leakage current
- ◆ Low operating and clamping voltages

PIN CONFIGURATION (SOT-563 / SC-89)



PART MARKING





SPE0514

4-Line ESD Protection Array

ORDERING INFORMATION

Part Number	Package	Part Marking
SPE0514S56RG	SOT-563	4

※ SPE0514S56RG : Tape Reel ; Pb – Free

ABSOLUTE MAXIMUM RATINGS

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Peak Pulse Power (t _p = 8/20 μs)	P _{pk}	250	W
Maximum Peak Pulse Current (t _p = 8/20 μs)	I _{pp}	7	A
ESD per ICE 61000 – 4 – 2 (Air)	V _{pp}	±15	KV
ESD per ICE 61000 – 4 – 2 (Contact)	V _{pp}	±8	KV
Operating Junction Temperature	T _J	-55 ~ 150	°C
Storage Temperature Range	T _{STG}	-55 ~ 150	°C
Lead Soldering Temperature	T _L	260 (10sec)	°C

ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

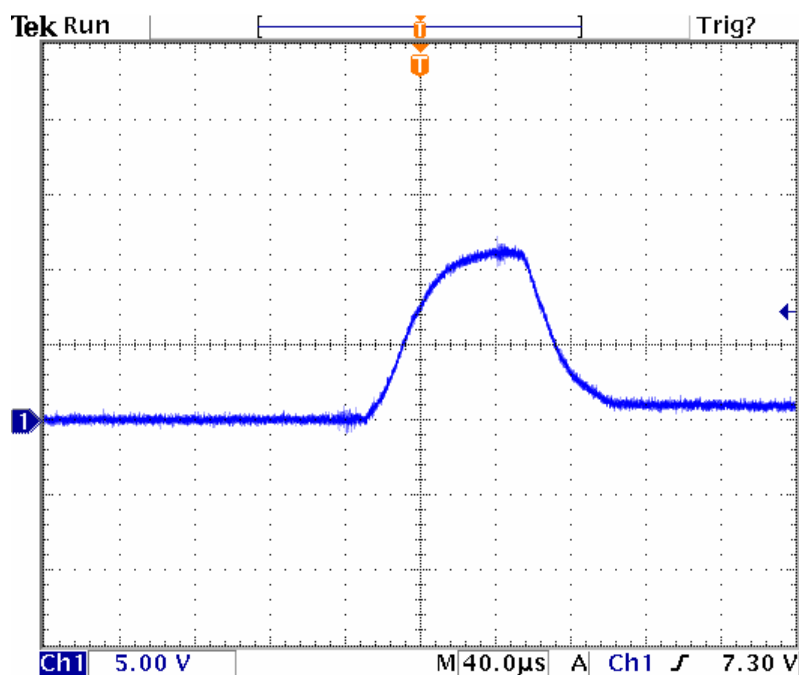
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Reverse Stand – Off Voltage	V _{RWM}				5	V
Reverse Breakdown Voltage	V _{BR}	I _t = 1mA	6		8.5	V
Reverse Leakage Current	I _R	V _{RWM} = 5V , T=25°C		0.01	1	μA
Reverse Leakage Current	I _R	V _{RWM} = 3V , T=25°C		0.01	0.5	μA
Clamping Voltage	V _C	I _{pp} = 1A , t _p = 8/20 μs			11.5	V
Clamping Voltage	V _C	I _{pp} = 7A , t _p = 8/20 μs			15	V
Junction Capacitance	C _j	Between I/O Pin and GND V _R = 0V , f = 1MHz		10	20	pF



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4-Line ESD Protection Array

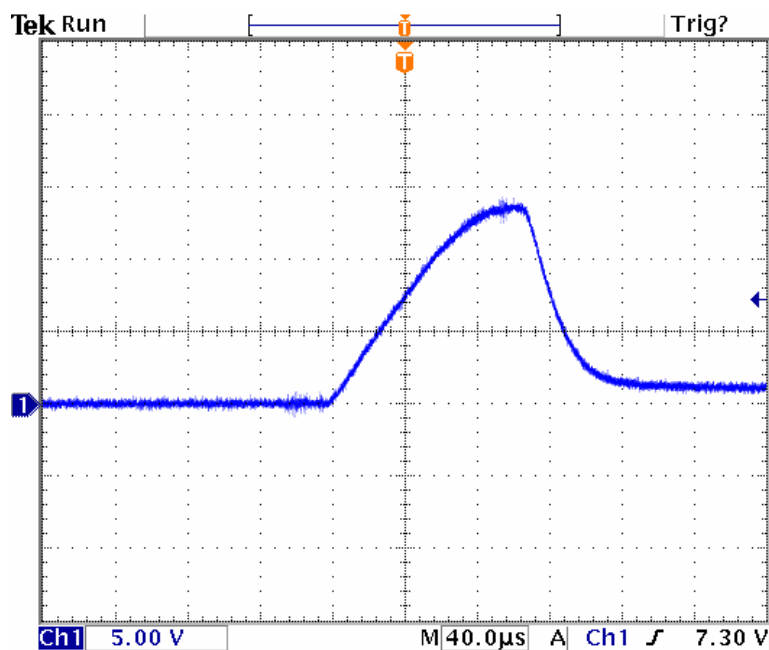
TYPICAL CHARACTERISTICS



40.0000ns

Clamping Voltage ($I_{pp} = 1A$, $t_p = 8/20 \mu s$)

26 Oct 2005
12:15:46



40.0000ns

Clamping Voltage ($I_{pp} = 7A$, $t_p = 8/20 \mu s$)

26 Oct 2005
12:08:20



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4-Line ESD Protection Array

TYPICAL CHARACTERISTICS

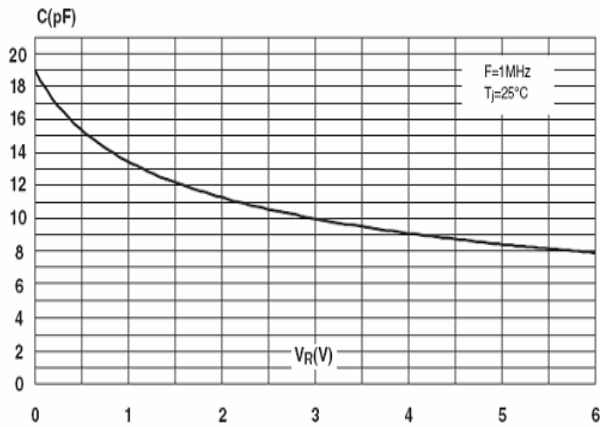


Fig 1 : Junction Capacitance V.S Reverse Voltage Applied

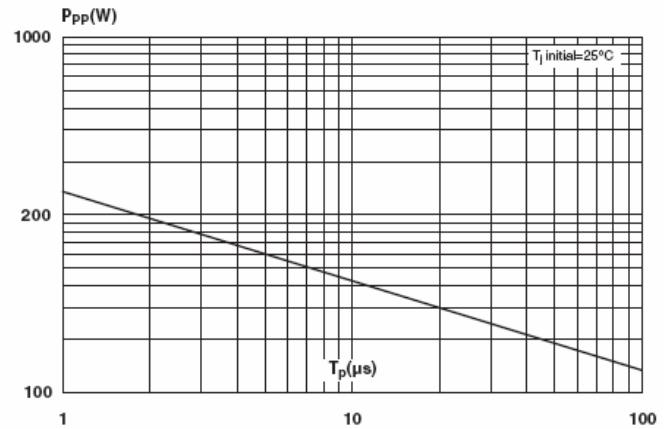


Fig 2 : Peak Plus Power V.S Exponential Plus Duration

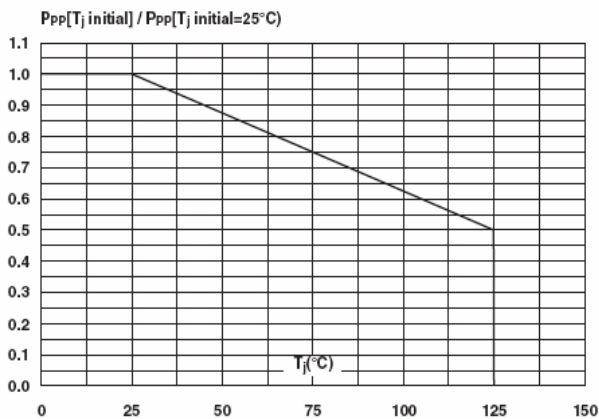


Fig 3 : Relative Variation of Peak Plus Power V.S Initial Junction Temperature

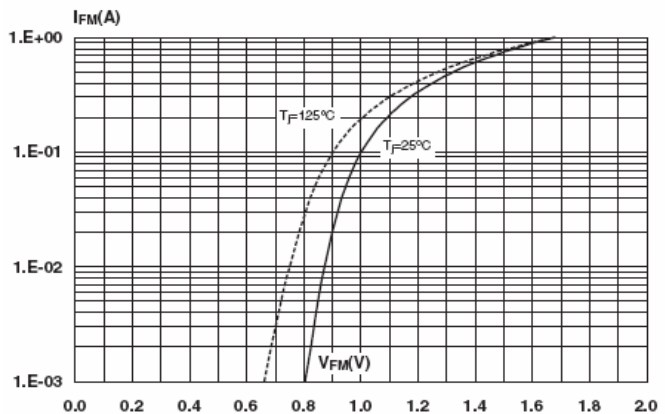


Fig 4 : Forward Voltage Drop V.S Peak Forward Current



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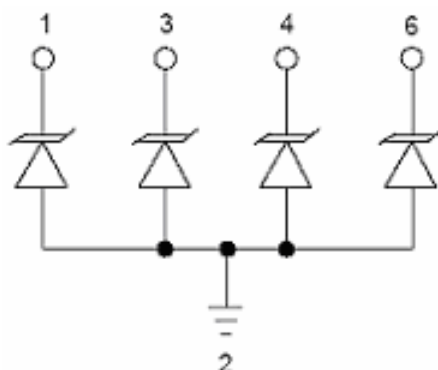
4-Line ESD Protection Array

APPLICATION NOTE

Device Connection for Protection of Four Data Lines

SPE0514 is designed to protect up to four data lines. The device is connected as follows:

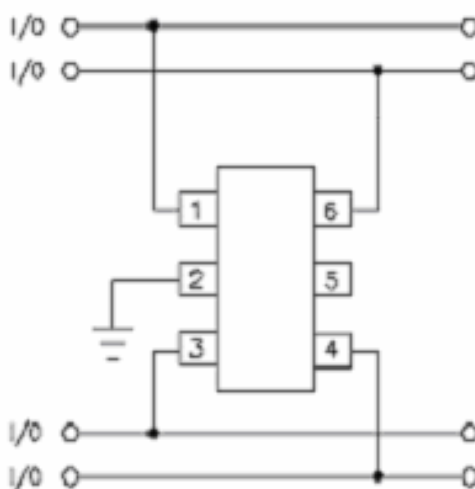
1. The TVS protection of four I/O lines is achieved by connecting pins 1, 3, 4 and 6 to the data lines. Pin 2 is connected to ground. The ground connection should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance.



Circuit Board Layout Recommendations for Suppression of ESD

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

1. Place the TVS near the input terminals or connectors to restrict transient coupling.
2. Minimize the path length between the TVS and the protected line.
3. Minimize all conductive loops including power and ground loops.
4. The ESD transient return path to ground should be kept as short as possible.
5. Never run critical signals near board edges
6. Use ground planes whenever possible.

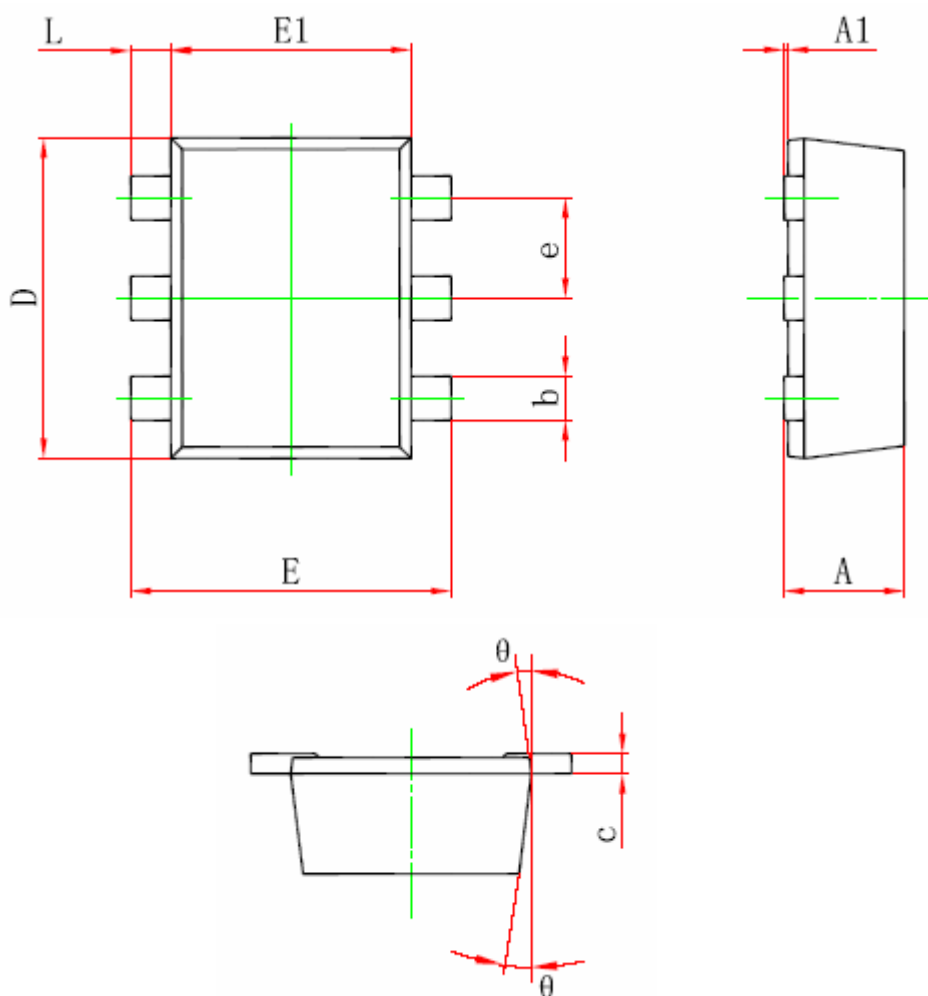




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4-Line ESD Protection Array

SOT-563 PACKAGE OUTLINE



Symbol	Dimenlons In Millimeters		Dimenlons In Inches	
	Min.	Max.	Min.	Max.
A	0.525	0.600	0.021	0.024
A1	0.000	0.050	0.000	0.002
e	0.450	0.550	0.018	0.022
c	0.090	0.160	0.004	0.006
D	1.500	1.700	0.059	0.067
b	0.170	0.270	0.007	0.011
E1	1.100	1.300	0.043	0.051
E	1.500	1.700	0.059	0.067
L	0.100	0.300	0.004	0.012
theta	7 °REF.		7 °REF.	



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4-Line ESD Protection Array

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