19-2959; Rev 3; 5/04

EVALUATION KIT AVAILABLE

3.5- and 4.5-Digit, Single-Chip ADCs with LCD Drivers

General Description

The MAX1492/MAX1494 low-power, 3.5- and 4.5-digit, analog-to-digital converters (ADCs) with integrated liquid crystal display (LCD) drivers operate from a single 2.7V to 5.25V power supply. They include an internal reference, a high-accuracy on-chip oscillator, and a triplexed LCD driver. An internal charge pump generates the negative supply needed to power the integrated input buffer for single-supply operation. The ADC is configurable for either a ±2V or ±200mV input range and outputs its conversion results to an LCD and/or to a microcontroller (µC). µC communication is facilitated through an SPI™-/QSPI™-/MICROWIRE™-compatible serial interface. The MAX1492 is a 3.5-digit (±1999 count) device, and the MAX1494 is a 4.5-digit (±19,999 count) device.

The MAX1492/MAX1494 do not require external-precision integrating capacitors, autozero capacitors, crystal oscillators, charge pumps, or other circuitry required with dual-slope ADCs (commonly used in panel meter circuits).

These devices also feature on-chip buffers for the differential signal and reference inputs, allowing direct interface with high-impedance signal sources. In addition, they use continuous internal-offset calibration and offer >100dB simultaneous rejection of 50Hz and 60Hz line noise. Other features include data hold and peak hold, overrange and underrange detection, and a low-battery monitor.

The MAX1494 comes in a 32-pin, 7mm x 7mm TQFP package, and the MAX1492 comes in 28-pin SSOP and 28-pin PDIP packages. All devices in this family operate over the 0°C to +70°C commercial temperature range.

Applications

Digital Panel Meters

Hand-Held Meters

Digital Voltmeters

Digital Multimeters

Features

- **High Resolution**
  MAX1494: 4.5 Digits (±19,999 Count)
  MAX1492: 3.5 Digits (±1999 Count)
- **Sigma-Delta ADC Architecture**
  No Integrating Capacitors Required
  No Autozeroing Capacitors Required
  >100dB of Simultaneous 50Hz and 60Hz Rejection
- **Operate from a Single 2.7V or 5.25V Supply**
- **Selectable Input Range of ±200mV or ±2V**
- **Selectable Voltage Reference: Internal 2.048V or External**
- **Internal High-Accuracy Oscillator Needs No External Components**
- **Automatic Offset Calibration**
- **Low Power**
  Maximum 960µA Operating Current
  Maximum 400µA Shutdown Current
- **Small 32-Pin 7mm x 7mm TQFP Package (4.5 Digits), 28-Pin SSOP Package (3.5 Digits)**
- **Triplexed LCD Driver**
- **SPI-/QSPI-/MICROWIRE-Compatible Serial Interface**
- **Evaluation Kit Available (Order MAX1494EVKIT)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	RESOLUTION (DIGITS)
MAX1492CAI	0°C to +70°C	28 SSOP	3.5
MAX1492CNI	0°C to +70°C	28 PDIP	3.5
MAX1494CCJ	0°C to +70°C	32 TQFP	4.5

Pin Configurations appear at end of data sheet.

SPI/QSPI are trademarks of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor Corp.

3.5- and 4.5-Digit, Single-Chip ADCs with LCD Drivers

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to GND .....-0.3V to +6V
DV_{DD} to GND .....-0.3V to +6V
AIN+, AIN- to GND .....V_{NEG} to +(AV_{DD} + 0.3V)
REF+, REF- to GND.....V_{NEG} to +(AV_{DD} + 0.3V)
LOWBATT to GND .....-0.3V to (AV_{DD} + 0.3V)
CLK, $\overline{EOC}$, $\overline{CS}$, DIN, SCLK, DOUT to GND .....-0.3V to (DV_{DD} + 0.3V)
SEG_ and BP_ to GND .....-0.3V to (DV_{DD} + 0.3V)
V_{NEG} to GND .....-2.6V to (AV_{DD} + 0.3V)
V_{DISP} to GND.....-0.3V to (DV_{DD} + 0.3V)
Maximum Current into Any Pin 50mA

Continuous Power Dissipation (T_A = +70°C)
28-Pin SSOP (derate 9.5mW/°C above +70°C) 762mW
28-Pin PDIP (derate 14.3mW/°C above +70°C).....1142.9mW
32-Pin TQFP (derate 20.7mW/°C above +70°C).....1652.9mW
Operating Temperature Range.....0°C to +70°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DD} = +2.7V to +5.25V, GND = 0, V_{REF+} - V_{REF-} = 2.048V (external reference). Internal clock mode, unless otherwise noted. All specifications are at T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Noise-Free Resolution		MAX1494	-19,999		+19,999	Count
		MAX1492	-1999		+1999	
Integral Nonlinearity (Note 1)	INL	2.000V range		±1		Count
		200mV range		±1		
Range Change Accuracy		(V_{AIN+} - V_{AIN-} = 0.100V) on 200mV range / (V_{AIN+} - V_{AIN-} = 0.100V) on 2.0V range		10:1		Ratio
Rollover Error (See the *Definitions* Section)		V_{AIN+} - V_{AIN-} = full scale, V_{AIN-} - V_{AIN+} = full scale		±1		Count
Output Noise				10		μV_{P-P}
Offset Error (Zero Input Reading)	Offset	V_{IN} = 0 (Note 2)	-0		0	Reading
Gain Error		(Note 3)	-0.5		+0.5	%FSR
Offset Drift (Zero-Reading Drift)		V_{IN} = 0 (Note 4)		0.1		µV/°C
Gain Drift				±1		ppm/°C
INPUT CONVERSION RATE						
External Clock Frequency				4.915		MHz
External-Clock Duty Cycle			40		60	%
Conversion Rate		Internal clock		5		Hz
		External clock, f_{CLK} = 4.915MHz		5		
ANALOG INPUTS (AIN+, AIN-, bypass to GND with 0.1µF or greater capacitors)						
AIN Input-Voltage Range (Note 5)		RANGE bit = 0, ±2V	-2.0		+2.0	V
		RANGE bit = 1, ±200mV	-0.2		+0.2	
AIN Absolute Input Voltage to GND			-2.2		+2.2	V

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +2.7V to +5.25V, GND = 0, V_{REF+} - V_{REF-} = 2.048V (external reference). Internal clock mode, unless otherwise noted. All specifications are at T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Normal-Mode 50Hz and 60Hz Rejection (Simultaneously)		Internal clock mode, 50Hz and 60Hz ±2%		100		dB
		External clock mode, 50Hz and 60Hz ±2%, f_{CLK} = 4.915MHz		120		
Common-Mode 50Hz and 60Hz Rejection (Simultaneously)	CMR	For 50Hz and 60Hz ±2%, R_{SOURCE} < 10kΩ		150		dB
Common-Mode Rejection	CMR	At DC		100		dB
Input Leakage Current				10		nA
Input Capacitance				10		pF
Dynamic Input Current		(Note 6)	-20		+20	nA
LOW-BATTERY VOLTAGE MONITOR (LOWBATT)						
LOWBATT TripThreshold				2.048		V
LOWBATT Leakage Current				10		pA
Hysteresis				20		mV
INTERNAL REFERENCE (INTREF BIT = 1, REF- = GND, bypass REF+ to GND with a 4.7µF capacitor)						
REF Output Voltage	V_{REF}	AV_{DD} = 5V, T_A = +25°C	2.007	2.048	2.089	V
REF Output Short-Circuit Current				1		mA
REF Output Temperature Coefficient	TC_{VREF}	AV_{DD} = 5V		40		ppm/°C
Load Regulation		I_{SOURCE} = 0 to 300µA, I_{SINK} = 0 to 30µA		6		mV/µA
Line Regulation				50		µV/V
Noise Voltage		0.1Hz to 10Hz		25		$µV_{P-P}$
		10Hz to 10kHz		400		
EXTERNAL REFERENCE (INTREF BIT = 0, bypass REF+ and REF- to GND with 0.1µF or larger capacitors)						
REF Input Voltage		Differential (V_{REF+} - V_{REF-})		2.048		V
Absolute REF Input Voltage to GND			-2.2		+2.2	V
Normal-Mode 50Hz and 60Hz Rejection (Simultaneously)		Internal clock mode, 50Hz and 60Hz ±2%		100		dB
		External clock mode, 50Hz and 60Hz ±2%, f_{CLK} = 4.915MHz		120		
Common-Mode 50Hz and 60Hz Rejection (Simultaneously)	CMR	For 50Hz and 60Hz ±2%, R_{SOURCE} < 10kΩ		150		dB
Common-Mode Rejection	CMR	At DC		100		dB
Input Leakage Current				10		nA
Input Capacitance				10		pF
Dynamic Input Current		(Note 6)	-20		+20	nA

3.5- and 4.5-Digit, Single-Chip ADCs with LCD Drivers

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +2.7V to +5.25V, GND = 0, V_{REF+} - V_{REF-} = 2.048V (external reference). Internal clock mode, unless otherwise noted. All specifications are at T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGE PUMP (C_{NEG} = 0.1µF)						
Output Voltage	V_{NEG}		-2.60	-2.42	-2.30	V
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, CLK)						
Input Current	I_{IN}	V_{IN} = 0 or DV_{DD}	-10		+10	µA
Input Low Voltage	V_{INL}				0.3 x DV_{DD}	V
Input High Voltage	V_{INH}		0.7 x DV_{DD}			V
Input Hysteresis	V_{HYST}	DV_{DD} = 3.0V		200		mV
DIGITAL OUTPUTS (DOUT, $\overline{EOC}$)						
Output Low Voltage	V_{OL}	I_{SINK} = 1mA			0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 200µA	0.8 x DV_{DD}			V
Tri-State Leakage Current	I_L	D_{OUT} only	-10		+10	µA
Tri-State Output Capacitance	C_{OUT}	D_{OUT} only		15		pF
POWER SUPPLY						
AV_{DD} Voltage	AV_{DD}		2.70		5.25	V
DV_{DD} Voltage	DV_{DD}		2.70		5.25	V
Power-Supply Rejection AV_{DD}	$PSRR_A$	(Note 7)		80		dB
Power-Supply Rejection DV_{DD}	$PSRR_D$	(Note 7)		100		dB
AV_{DD} Current (Notes 8, 9)	I_{AVDD}	AV_{DD} = 5V		580	660	µA
		Standby		240	380	
DV_{DD} Current (Notes 8, 9)	I_{DVDD}	DV_{DD} = 5V		260	320	µA
		DV_{DD} = 3.3V		130	180	
		Standby		10	20	
LCD DRIVER						
RMS Segment On Voltage		MAX1492		1.92 x DV_{DD}		V
		MAX1494		1.92 x (DV_{DD} - V_{DISP})		
RMS Segment Off Voltage		MAX1492		1/3 x DV_{DD}		V
		MAX1494		1/3 x (DV_{DD} - V_{DISP})		
Display Voltage Setup Resistor	R_{DISP}	MAX1494 only		157.5		kΩ
Display Multiplex Rate				107		Hz
LCD Data-Update Rate				2.5		Hz

TIMING CHARACTERISTICS (Notes 10, 11 and Figure 13)

(AV_{DD} = DV_{DD} = 2.7V to +5.25V, GND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Operating Frequency	f_{SCLK}		0		4.2	MHz
SCLK Pulse-Width High	t_{CH}		100			ns
SCLK Pulse-Width Low	t_{CL}		100			ns
DIN to SCLK Setup	t_{DS}		50			ns
DIN to SCLK Hold	t_{DH}		0			ns
$\overline{CS}$ Fall to SCLK Rise Setup	t_{CSS}		50			ns
SCLK Rise to $\overline{CS}$ Rise Hold	t_{CSH}		0			ns
SCLK Fall to DOUT Valid	t_{DO}	C_{LOAD} = 50pF (Figures 18, 19)			120	ns
$\overline{CS}$ Rise to DOUT Disable	t_{TR}	C_{LOAD} = 50pF (Figures 18, 19)			120	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DV}	C_{LOAD} = 50pF (Figures 18, 19)			120	ns

Note 1: Integral nonlinearity is the deviation of the analog value at any code from its theoretical value after nulling the gain error and offset error.

Note 2: Offset calibrated. See the *$\overline{OFFSET}$_$\overline{CAL1}$* and *OFFSET_CAL2* sections in the *On-Chip Registers* section.

Note 3: Offset nulled.

Note 4: Drift error is eliminated by recalibration at the new temperature.

Note 5: The input voltage range for the analog inputs is given with respect to the voltage on the negative input of the differential pair.

Note 6: V_{AIN+} or V_{AIN-} = -2.2V to +2.2V. V_{REF+} or V_{REF-} = -2.2V to +2.2V. All input structures are identical. Production tested on AIN+ and REF+ only.

Note 7: Measured at DC by changing the power-supply voltage from 2.7V to 5.25V and measuring the effect on the conversion error with external reference. PSRR at 50Hz and 60Hz exceeds 120dB with filter notches at 50Hz and 60Hz (Figure 2).

Note 8: CLK and SCLK are idle.

Note 9: Power-supply currents are measured with all digital inputs at either GND or DV_{DD} and with the device in internal clock mode.

Note 10: All input signals are specified with t_{RISE} = t_{FALL} = 5ns (10% to 90% of DV_{DD}) and are timed from a voltage level of 50% of DV_{DD}, unless otherwise noted.

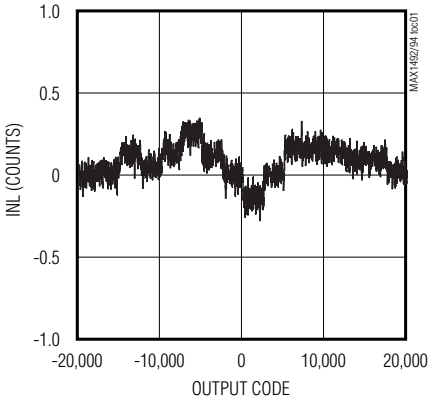
Note 11: See the serial-interface timing diagrams.

3.5- and 4.5-Digit, Single-Chip ADCs with LCD Drivers

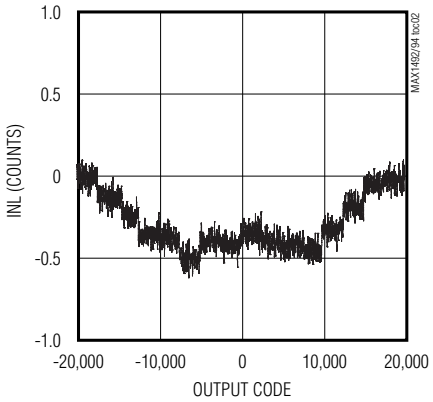
Typical Operating Characteristics

(AV_{DD} = DV_{DD} = 5V, GND = 0, external reference mode, REF+ = 2.048V, REF- = GND, RANGE bit = 1, internal clock mode, T_A = +25°C, unless otherwise noted.)

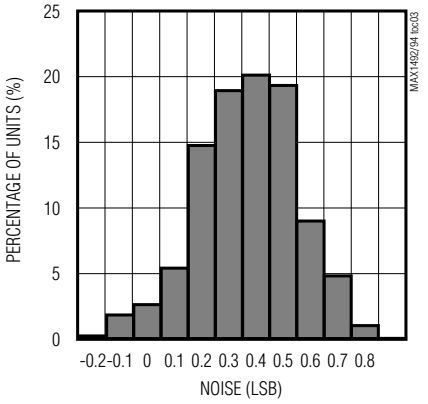
MAX1494 (±200mV INPUT RANGE) INL vs. OUTPUT CODE



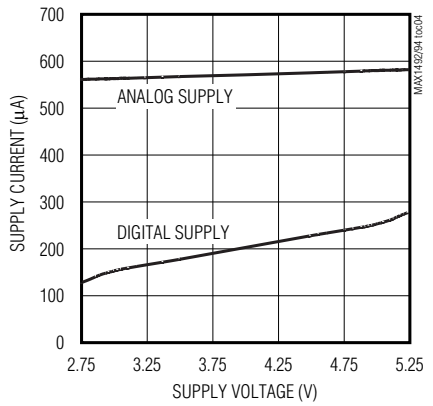
MAX1494 (±2V INPUT RANGE) INL vs. OUTPUT CODE



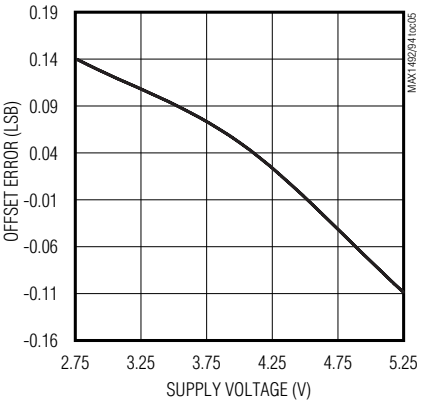
NOISE DISTRIBUTION



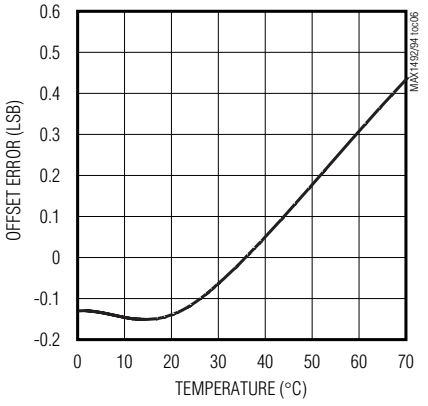
SUPPLY CURRENT vs. SUPPLY VOLTAGE



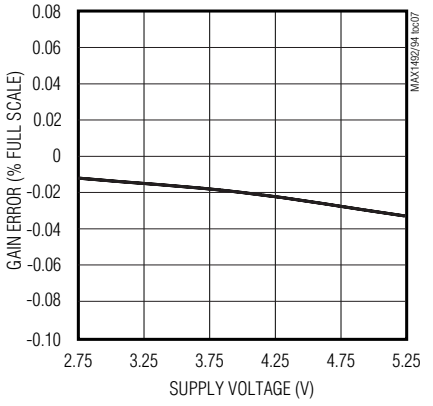
MAX1494 OFFSET ERROR vs. SUPPLY VOLTAGE



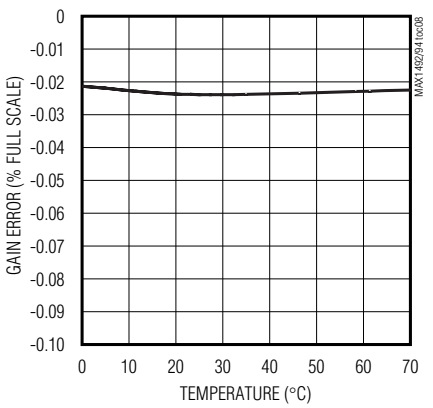
MAX1494 OFFSET ERROR vs. TEMPERATURE



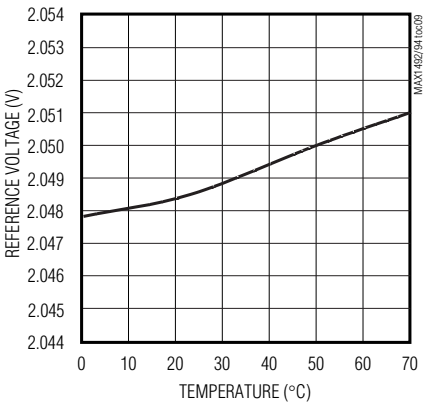
MAX1494 GAIN ERROR vs. SUPPLY VOLTAGE



MAX1494 GAIN ERROR vs. TEMPERATURE



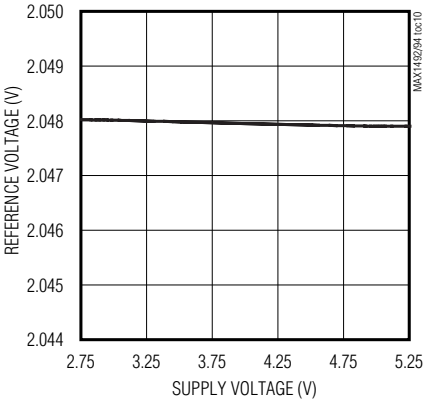
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



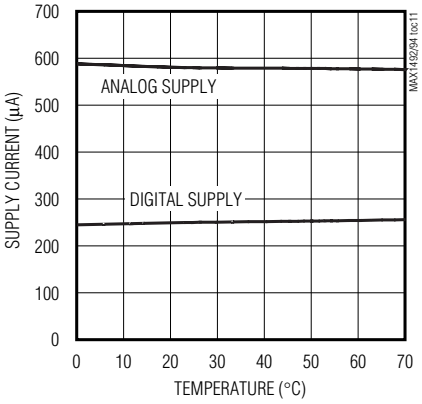
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = 5V, GND = 0, external reference mode, REF+ = 2.048V, REF- = GND, RANGE bit = 1, internal clock mode, T_A = +25°C, unless otherwise noted.)

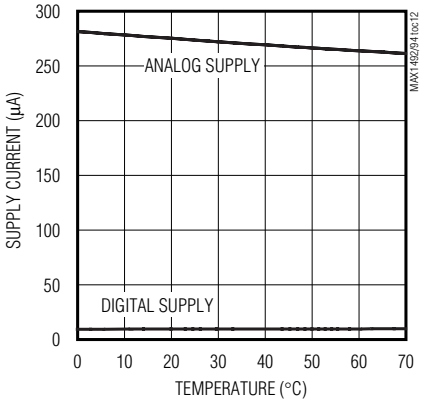
INTERNAL REFERENCE VOLTAGE vs. ANALOG SUPPLY VOLTAGE



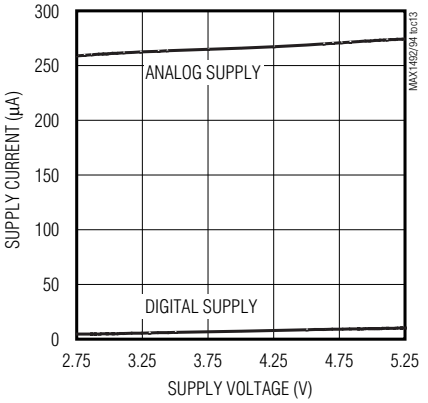
SUPPLY CURRENT vs. TEMPERATURE



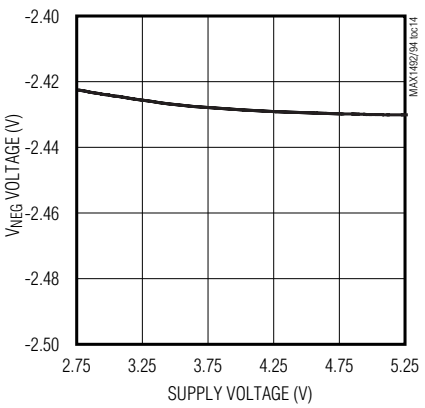
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



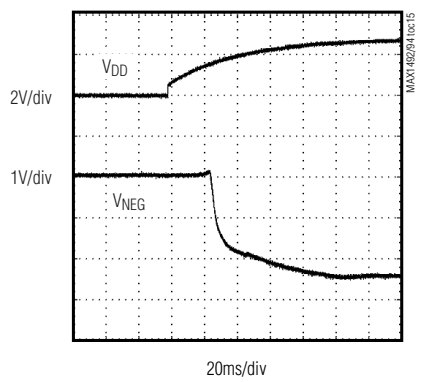
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



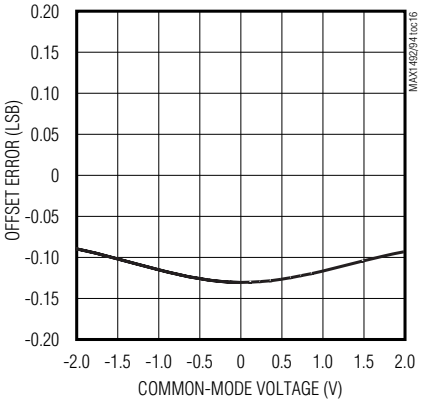
CHARGE-PUMP OUTPUT VOLTAGE vs. ANALOG SUPPLY VOLTAGE



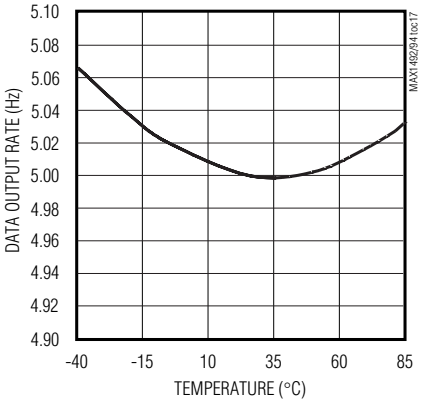
V_{NEG} STARTUP SCOPE SHOT



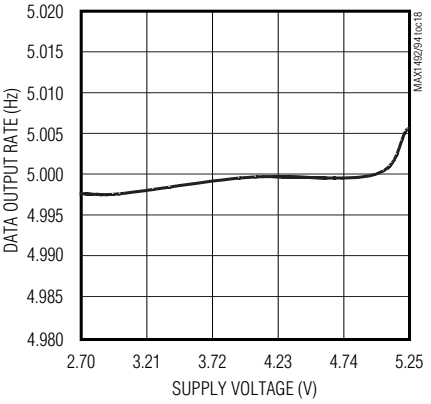
OFFSET ERROR vs. COMMON-MODE VOLTAGE



DATA OUTPUT RATE vs. TEMPERATURE



DATA OUTPUT RATE vs. SUPPLY VOLTAGE



3.5- and 4.5-Digit, Single-Chip ADCs with LCD Drivers

Pin Description

PIN		NAME	FUNCTION
MAX1492	MAX1494		
1	30	CLK	External Clock Input. When the EXTCLK bit in the control register is set, CLK is the master clock input for the modulator and the filter (frequency = 4.9152MHz). When the EXTCLK bit in the control register is reset, the internal clock is used. Connect CLK to GND or DV_{DD} when the internal oscillator is used.
2	31	DV_{DD}	Digital Power Input. Connect DV_{DD} to a 2.7V to 5.25V power supply. Bypass DV_{DD} to GND with 0.1µF and 4.7µF capacitors.
3	32	GND	Ground
4	1	AV_{DD}	Analog Power Input. Connect AV_{DD} to a 2.7V to 5.25V power supply. Bypass AV_{DD} to GND with 0.1µF and 4.7µF capacitors.
5	2	AIN+	Positive Analog Input. Positive side of fully differential analog input. Bypass AIN+ to GND with a 0.1µF or greater capacitor.
6	3	AIN-	Negative Analog Input. Negative side of fully differential analog input. Bypass AIN- to GND with a 0.1µF or greater capacitor.
7	4	REF-	Negative Reference Input. During internal reference operation, connect REF- to GND. For external reference operation, bypass REF- to GND with a 0.1µF capacitor and set V_{REF-} from -2.2V to +2.2V, provided $V_{REF+} > V_{REF-}$.
8	5	REF+	Positive Reference Input. During internal reference operation, connect a 4.7µF capacitor from REF+ to GND. For external reference operation, bypass REF+ to GND with a 0.1µF capacitor and set V_{REF+} from -2.2V to +2.2V, provided $V_{REF+} > V_{REF-}$.
9	6	LOWBATT	Low-Battery Input. When $V_{LOWBATT}$ < 2.048V (typ), the LOWBATT symbol on LCD turns on and the LOWBATT bit latches high in the status register.
10	7	$\overline{EOC}$	Active-Low, End-of-Conversion Logic Output. A logic-low at $\overline{EOC}$ indicates that a new ADC result is available in the ADC result register.
11	8	$\overline{CS}$	Active-Low Chip-Select Input. Forcing $\overline{CS}$ low activates the serial interface.
12	9	DIN	Serial Data Input. Data present at DIN is shifted into the internal registers in response to a rising edge at SCLK when $\overline{CS}$ is low.
13	10	SCLK	Serial Clock Input. Apply an external clock to SCLK to facilitate communication through the serial bus. SCLK can idle high or low.
14	11	DOUT	Serial Data Output. DOUT presents serial data in response to register queries. Data shifts out on the falling edge of SCLK. DOUT goes high impedance when $\overline{CS}$ is high.
15	12	SEG1	LCD Segment 1 Driver
16	13	SEG2	LCD Segment 2 Driver
17	14	SEG3	LCD Segment 3 Driver
18	15	SEG4	LCD Segment 4 Driver
19	16	SEG5	LCD Segment 5 Driver
20	17	SEG6	LCD Segment 6 Driver
21	18	SEG7	LCD Segment 7 Driver
22	19	SEG8	LCD Segment 8 Driver
23	20	SEG9	LCD Segment 9 Driver

Pin Description (continued)

PIN		NAME	FUNCTION
MAX1492	MAX1494		
24	21	SEG10	LCD Segment 10 Driver
25	25	BP3	LCD Backplane 3 Driver
26	26	BP2	LCD Backplane 2 Driver
27	27	BP1	LCD Backplane 1 Driver
28	29	V_{NEG}	-2.42V Charge-Pump Output. Bypass V_{NEG} to GND with a 0.1µF capacitor.
—	22	SEG11	LCD Segment 11 Driver
—	23	SEG12	LCD Segment 12 Driver
—	24	SEG13	LCD Segment 13 Driver
—	28	V_{DISP}	Temperature-Compensation Voltage Input for LCD. If not using temperature compensation, connect V_{DISP} to GND. See the *V_{DISP} LCD Compensation* section.

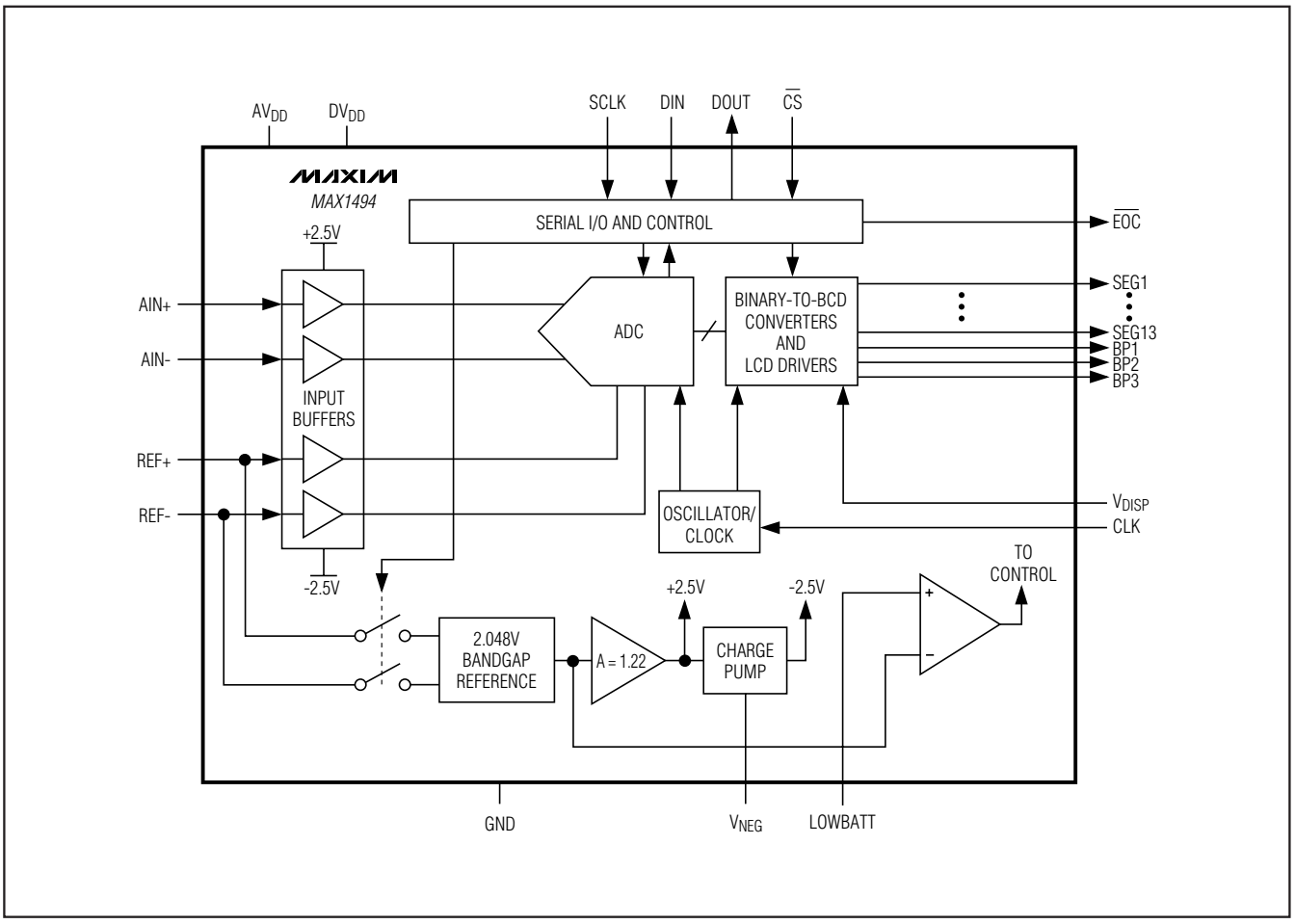


Figure 1. MAX1494 Functional Diagram

3.5- and 4.5-Digit, Single-Chip ADCs with LCD Drivers

Detailed Description

The MAX1492/MAX1494 low-power, highly integrated ADCs with LCD drivers convert a ±2V differential input voltage (one count is equal to 100µV for the MAX1494 and 1mV for the MAX1492) with a sigma-delta ADC and output the result to an LCD or µC. An additional ±200mV input range (one count is equal to 10µV for the MAX1494 and 100µV for the MAX1492) is available to measure small signals with increased resolution.

The devices operate from a single 2.7V to 5.25V power supply and offer 3.5-digit (MAX1492) or 4.5-digit (MAX1494) conversion results. An internal 2.048V reference, an internal charge pump, and a high-accuracy on-chip oscillator eliminate external components.

The MAX1492 and MAX1494 interface with a µC using an SPI/QSPI/MICROWIRE-compatible serial interface. Data can either be sent directly to the display or to the µC first for processing before being displayed.

The devices also feature on-chip buffers for the differential input signal and external reference inputs, allowing direct interface with high-impedance signal sources. In addition, they use continuous internal-offset calibration and offer >100dB of 50Hz and 60Hz line noise rejection. Other features include data hold and peak hold, overrange and underrange detection, and a low-battery monitor.

Analog Input Protection

Internal protection diodes limit the analog input range from V_{NEG} to (AV_{DD} + 0.3V). If the analog input exceeds this range, limit the input current to 10mA.

Internal Analog Input/Reference Buffers

The MAX1492/MAX1494 analog input/reference buffers allow the use of high-impedance signal sources. The input buffer's common-mode input range allows the analog inputs and the reference to range from -2.2V to +2.2V.

Modulator

The MAX1492/MAX1494 perform analog-to-digital conversions using a single-bit, 3rd-order, sigma-delta modulator. The sigma-delta modulator converts the input signal into a digital pulse train whose average duty cycle represents the digitized signal information. The modulator quantizes the input signal at a much higher sample rate than the bandwidth of the input.

The MAX1492/MAX1494 modulator provides 3rd-order frequency shaping of the quantization noise resulting from the single-bit quantizer. The modulator is fully differential for maximum signal-to-noise ratio and minimum susceptibility to power-supply noise. A single-bit data stream is then presented to the digital filter to remove the frequency-shaped quantization noise.

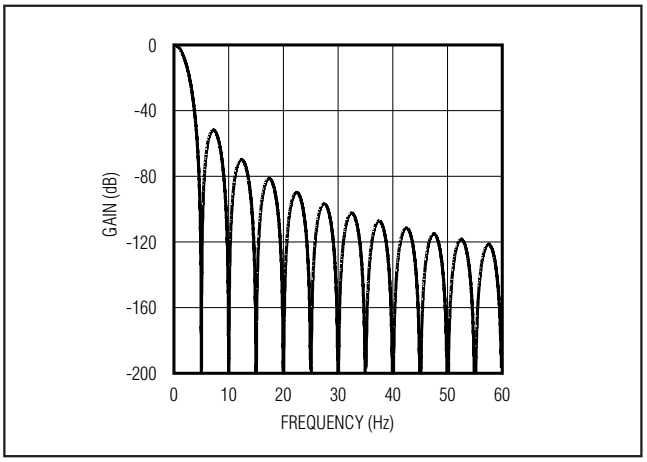


Figure 2. Frequency Response of the SINC^4 Filter (Notch at 60Hz)

Digital Filtering

The MAX1492/MAX1494 contain an on-chip digital lowpass filter that processes the data stream from the modulator using a SINC^4 ((sinx/x)^4) response. The SINC^4 filter has a settling time of four output data periods (4 x 200ms).

The MAX1492/MAX1494 have 25% overrange capability built into the modulator and digital filter.

The digital filter is optimized for f_{CLK} equal to 4.9152MHz. Lower clock frequencies can be used; however, 50Hz/60Hz noise rejection decreases. The frequency response of the SINC^4 filter is measured as follows:

$$H(z) = \left[\frac{1}{N}\frac{(1-z^{-N})}{(1-z^{-1})}\right]^4$$

$$H(f) = \left[\frac{1}{N}\frac{\sin\left(N\pi\frac{f}{fm}\right)}{\sin\left(\pi\frac{f}{fm}\right)}\right]^4$$

where N is the oversampling ratio, and fm = N × output data rate = 5Hz.

Filter Characteristics

Figure 2 shows the filter frequency response. The SINC^4 characteristic -3dB cutoff frequency is 0.228 times the first-notch frequency (5Hz).

The output data rate for the digital filter corresponds with the positioning of the first notch of the filter's frequency response. The notches of the SINC^4 filter are repeated at multiples of the first-notch frequency. The SINC^4 filter provides an attenuation of better than 100dB at these notches. For example, 50Hz is equal to

ten times the first-notch frequency and 60Hz is equal to 12 times the first-notch frequency.

For large step changes at the input, allow a settling time of 800ms before valid data is read.

Clock Modes

Configure the MAX1492/MAX1494 to use either the internal oscillator or an externally applied clock to drive the modulator and filter. Set the EXTCLK bit in the control register to 0 to put the device in internal clock mode. Set the EXTCLK bit high to put the device in external clock mode. Connect CLK to GND or DV_{DD} when using the internal oscillator. The MAX1492/MAX1494 ideally operate with a 4.9152MHz clock to achieve maximum rejection of 50Hz/60Hz common-mode, power-supply, and normal-mode noise.

Internal Clock Mode

The MAX1492/MAX1494 contain an internal oscillator. The power-up condition for the MAX1492/MAX1494 is internal clock operation with the EXTCLK bit in the control register equal to 0. Using the internal oscillator saves board space by removing the need for an external clock source.

External Clock Mode

For external clock operation, set the EXTCLK bit in the control register high and drive CLK with a 4.9152MHz clock source. Using an external clock allows for custom conversion rates. A 2.4576MHz clock signal reduces the conversion rate and the LCD update rate by a factor of two. The MAX1492/MAX1494 operate with an external clock source of up to 5.05MHz.

Charge Pump

The MAX1492/MAX1494 contain an internal charge pump to provide the negative supply voltage for the internal analog input/reference buffers. The bipolar input range of the analog input/reference buffers allows this device to accept negative inputs with high source impedances. Connect a 0.1µF capacitor from V_{NEG} to GND.

LCD Driver

The MAX1492/MAX1494 contain the necessary backplane and segment-driver outputs to drive 3.5-digit (MAX1492) and 4.5-digit (MAX1494) LCDs. The LCD update rate is 2.5Hz. Figures 4–7 show the connection schemes for a standard LCD. The MAX1492/MAX1494 automatically display the results of the ADC, if desired. The MAX1492/MAX1494 also allow independent control of the LCD driver through the serial interface, allowing for data processing of the ADC result before showing the result on the LCD. Additionally, each LCD segment can be individually controlled (see the *LCD Segment-Display Register* sections).

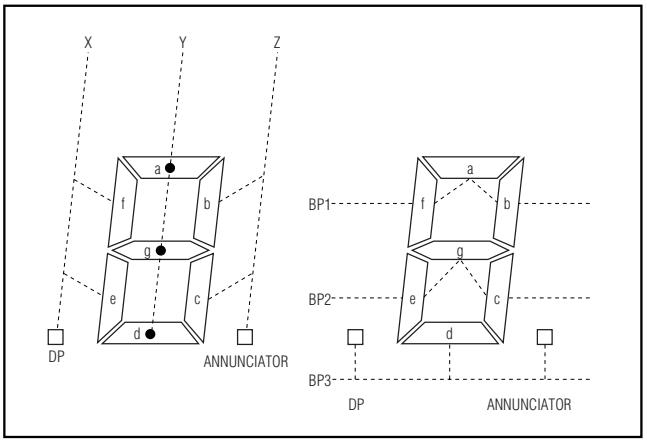


Figure 3. Connection Diagrams for Typical 7-Segment Displays

Triplexing

An internal resistor string comprised of three equal-value resistors (52kΩ, 1% matching) is used to generate the display drive voltages. On the MAX1492, one end of the string is connected to DV_{DD} and the other end is connected to GND. On the MAX1494, the other end of the resistor string is connected to V_{DISP}. Note that V_{LCD} should be three times the threshold voltage for the liquid crystal material used (Figure 9).

The connection diagrams for a typical 7-segment display-font decimal point and annunciators are illustrated in Figures 3 and 8. The MAX1494/MAX1492 numeric display drivers (4.5 digits, 3.5 digits) use this configuration to drive a triplexed LCD with three backplanes and 13 segment-driver lines (10 for 3.5 digits). Figures 4

Table 1. List of Custom LCD Manufacturers

MANUFACTURER	WEBSITE	PART NUMBER	DESCRIPTION
DCI, Inc.	www.dciincorporated.com	04-0924-00	3.5 digit, 5V
		04-0924-01	3.5 digit, 3V
		04-0925-00	4.5 digit, 5V
		04-0925-01	4.5 digit, 3V
The following site has links to other custom LCD manufacturers: www.earthlcd.com/mfr.htm			

3.5- and 4.5-Digit, Single-Chip ADCs with LCD Drivers

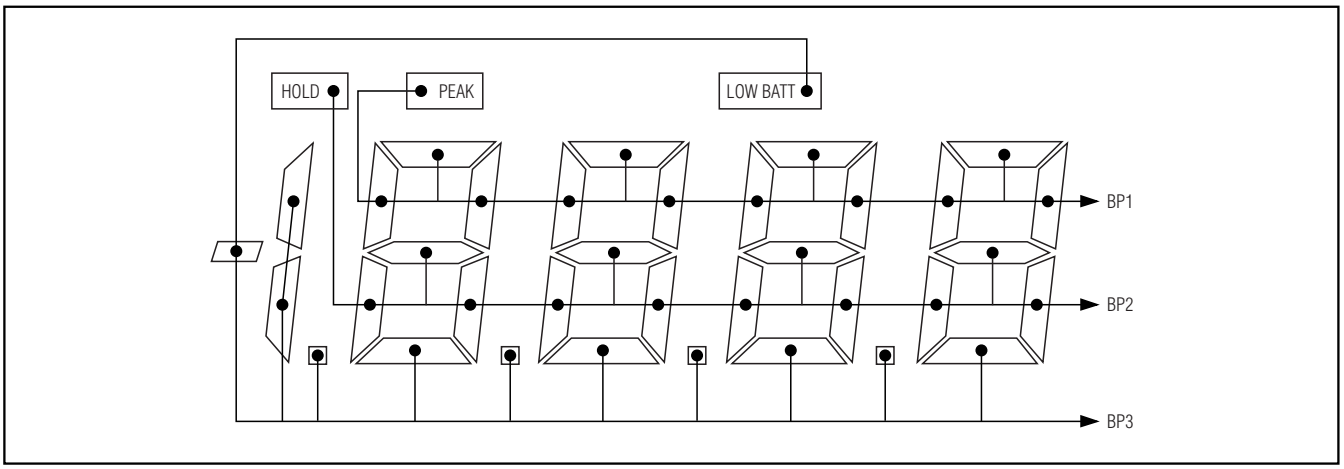


Figure 4. Backplane Connection for the MAX1494 (4.5 Digits)

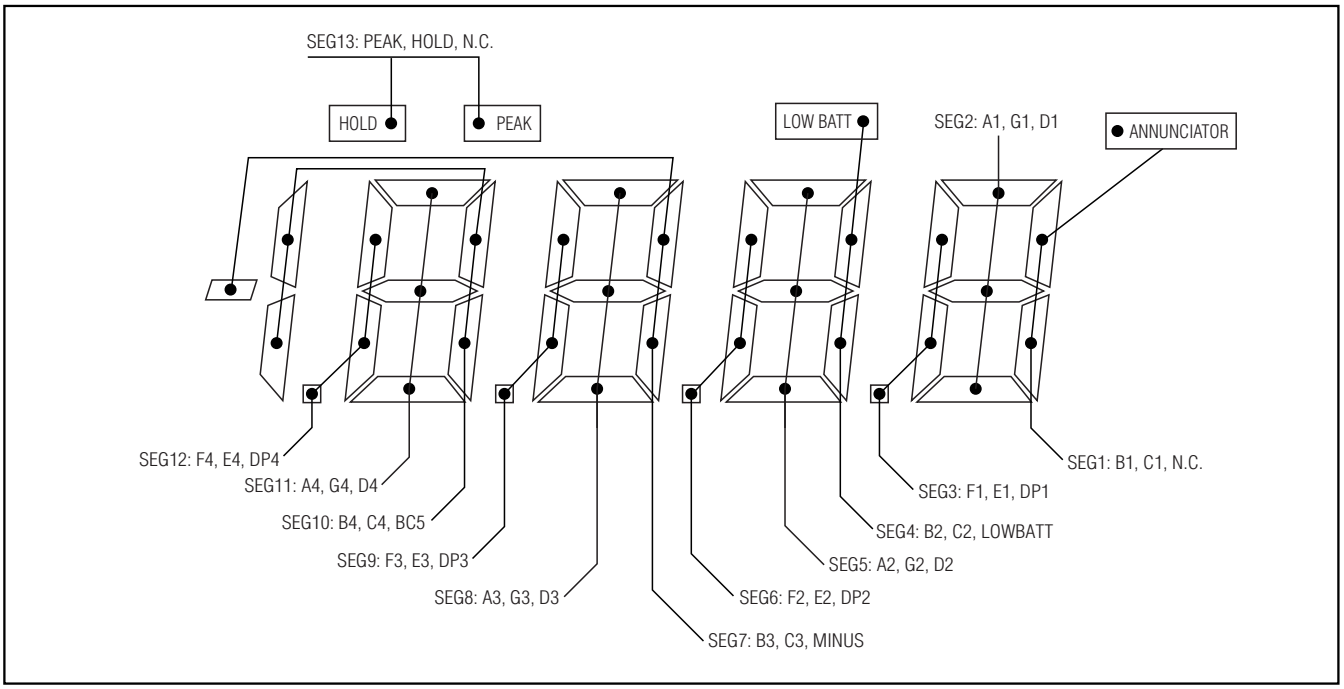


Figure 5. Segment Connection for the MAX1494 (4.5 Digits)

and 5 show the assignment of the 4.5-digit display segments, and Figures 6 and 7 show the assignment of the 3.5-digit display segments.

The voltage waveforms of the backplane lines and Y segment line (Figure 3) have been chosen as an example. This line intersects with BP1 to form the a segment, with BP2 to form the g segment, and with BP3 to form the d segment. Eight different ON/OFF combinations of the a, g, and d segments and their corresponding waveforms of the Y segment line are illustrated in Figures 9 and 10. The schematic diagram in Figure 8 shows each intersection as a capacitance from segment line to common line. Figure 11 illustrates the voltage across the g segment.

The RMS voltage across the segment determines the degree of polarization for the liquid crystal material and

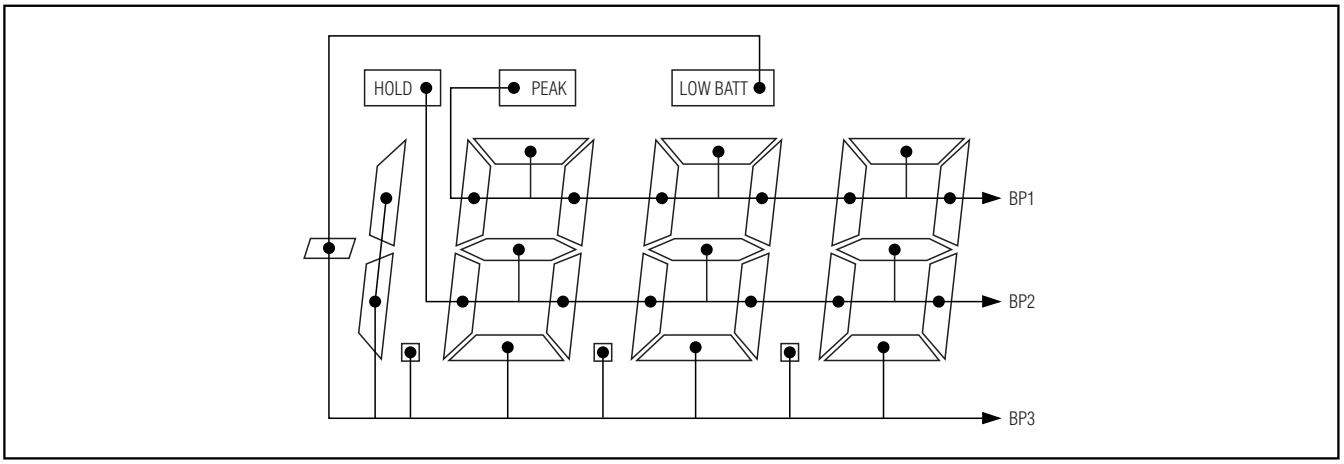


Figure 6. Backplane Connection for the MAX1492 (3.5 Digits)

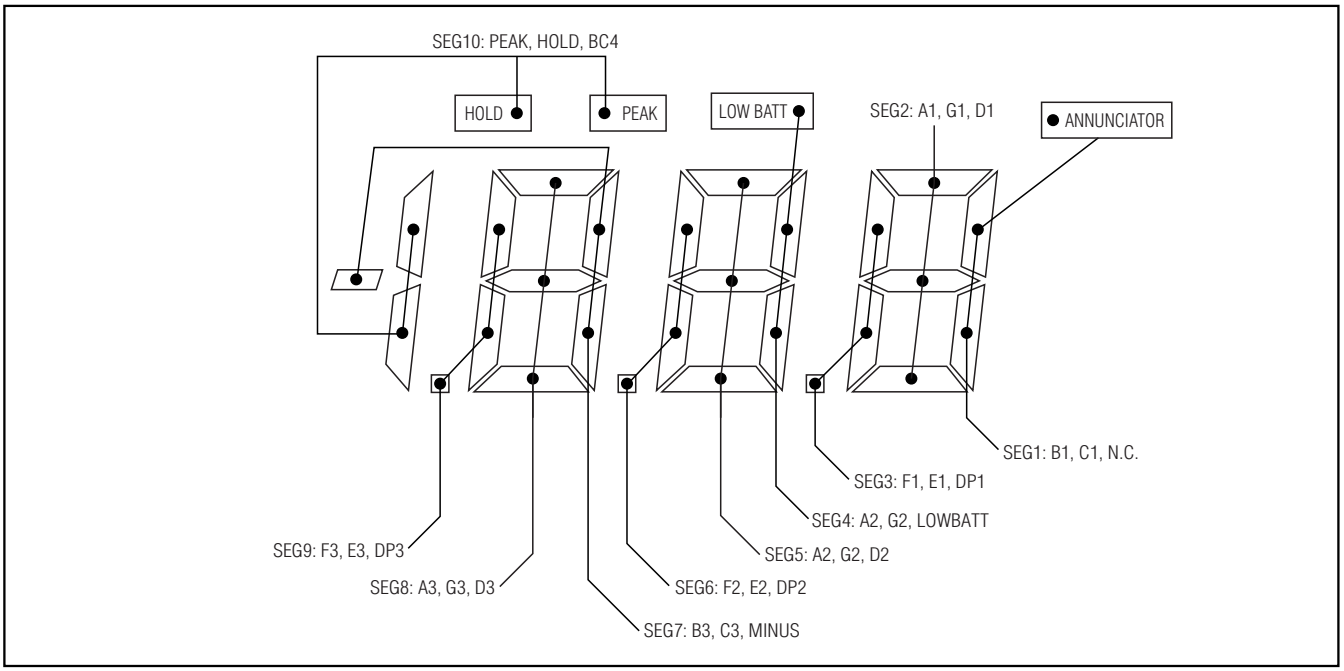


Figure 7. Segment Connection for the MAX1492 (3.5 Digits)

thus the contrast of the segment. The RMS OFF voltage is always V_{LCD} / 3, whereas the RMS ON voltage is always $1.92V_{LCD}$ / 3. This is illustrated in Figure 11. The ratio of RMS ON to RMS OFF voltage is fixed at 1.92 for a triplexed LCD.

Figure 12 illustrates contrast vs. applied RMS voltage with a V_{LCD} of 3.1V. The RMS ON voltage is 2.1V, and the RMS OFF voltage is 1.1V. The OFF segment has a contrast of less than 5%, while the ON segments have greater than 85% contrast.

If ghosting is present on the LCD, the RMS OFF voltage is too high. Choose an LCD with a higher RMS OFF voltage. Alternatively, lower the supply or apply a voltage on V_{DISP} to lower the RMS OFF voltage.

Figures 9 and 10 show the voltage on the LCD's BP_ inputs and the segment inputs during normal operation.

3.5- and 4.5-Digit, Single-Chip ADCs with LCD Drivers

Table 2. Decimal-Point Control Table (MAX1494)

DP_EN	DPSET1	DPSET2	DISPLAY OUTPUT	ZERO INPUT READING
0	0	0	1 8 8 8 8	0
0	0	1	1 8 8 8 8	0
0	1	0	1 8 8 8 8	0
0	1	1	1 8 8 8 8	0
1	0	0	1 8 8 8.8	0.0
1	0	1	1 8 8.8 8	0.00
1	1	0	1 8.8 8 8	0.000
1	1	1	1.8 8 8 8	0.0000

Table 3. Decimal-Point Control Table (MAX1492)

DP_EN	DPSET1	DPSET2	DISPLAY OUTPUT	ZERO INPUT READING
X	0	0	1 8 8.8	0.0
X	0	1	1 8.8 8	0.00
X	1	0	1.8 8 8	0.000
X	1	1	1 8 8 8	000

X = Don't care.

Table 4. LCD During Overrange and Underrange Conditions

CONDITION	MAX1492	MAX1494
OVERRANGE	1– – –	1– – – –
UNDERRANGE	-1– – –	-1– – – –

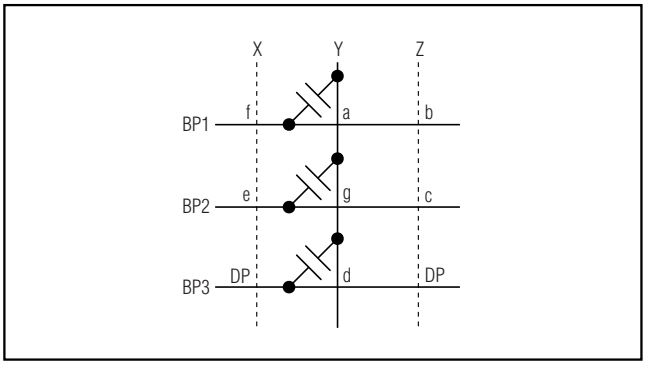


Figure 8. Schematic of Display Digit

The MAX1492/MAX1494 allow for full decimal-point control and feature leading zero suppression. Use the DP_EN, DPSET1, and DPSET2 bits in the control register to set the value of the decimal point. Tables 2 and 3 show the truth tables of the DP_EN, DPSET1, and DPSET2. The truth tables determine decimal-point usage.

The MAX1492/MAX1494 overrange and underrange display is shown in Table 4.

Reference

The MAX1492/MAX1494 reference sets the full-scale range of the ADC transfer function. With a nominal 2.048V reference, the ADC full-scale range is ±2V with the RANGE bit equal to 0. With the RANGE bit set to 1, the full-scale range is ±200mV. A decreased reference voltage decreases full-scale range (see the *Transfer Functions* section).

The MAX1492/MAX1494 accept either an external reference or an internal reference. The INTREF bit selects the reference mode (see the *Control Register (Read/Write)* section).

For internal-reference operation, set INTREF to 1, connect REF- to GND and bypass REF+ to GND with a 4.7µF capacitor. The internal reference provides a nominal 2.048V source between REF+ and GND. The internal-reference temperature coefficient is typically 40ppm/°C.

The default power-on state sets the MAX1492/MAX1494 to use the external reference with INTREF cleared to 0. The external reference inputs, REF+ and REF-, are fully differential. For a valid external-reference input, V_{REF+} must be greater than V_{REF-}. Bypass REF+ and REF- with a 0.1µF or greater capacitor to GND in external-reference mode.

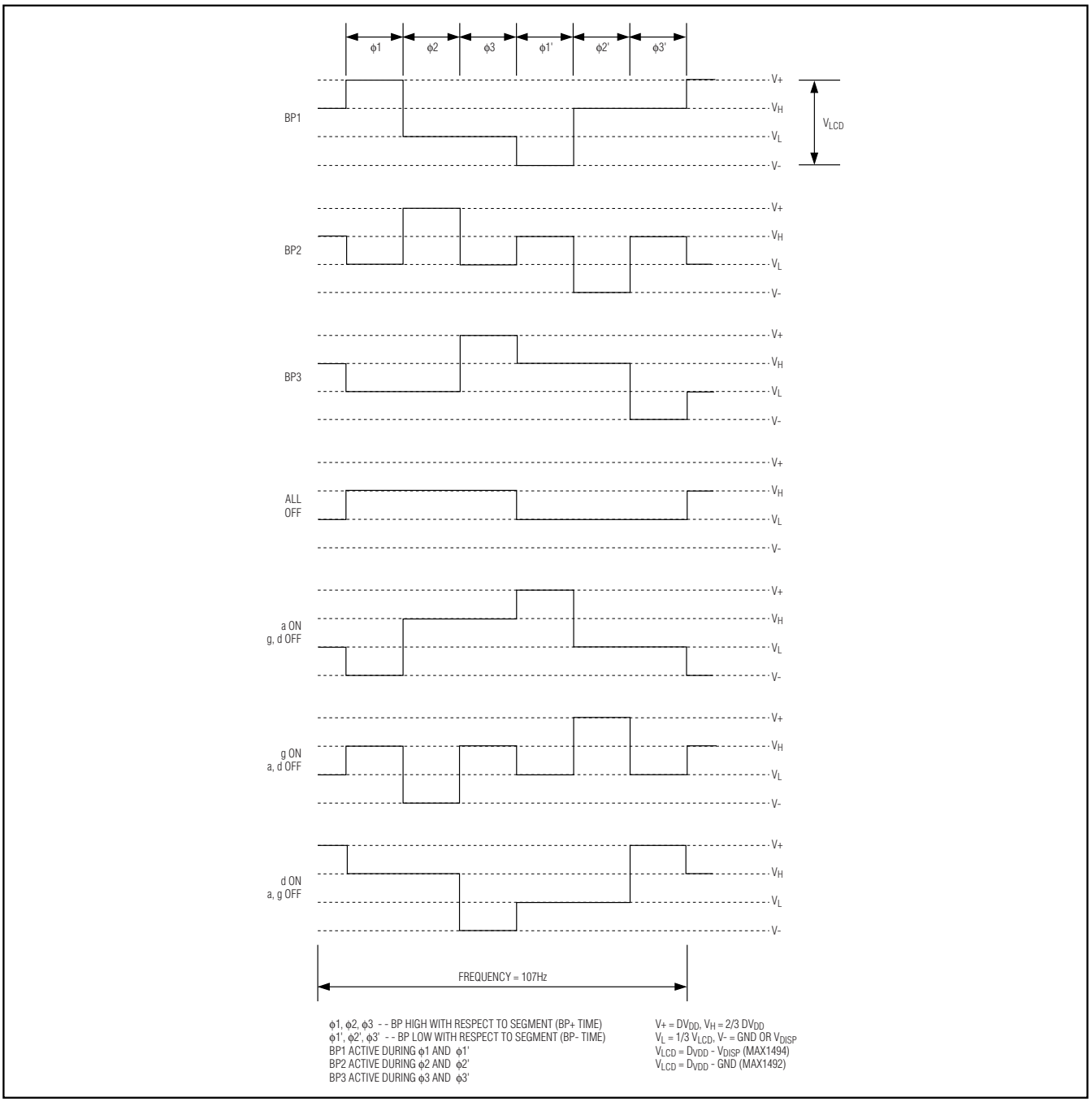


Figure 9. LCD Voltage Waveform—Combinations 1–4 (BP_, SEG2/5/8)

Figure 21 shows the MAX1492/MAX1494 operating with an external single-ended reference. In this mode, REF- is connected to GND and REF+ is driven with an external 2.048V reference. Bypass REF+ to GND with a 0.47µF capacitor.

Figure 20 shows the MAX1492/MAX1494 operating with an external differential reference. In this mode, REF- is connected to the top of the strain gauge and REF+ is connected to the midpoint of the resistor-divider of the supply.

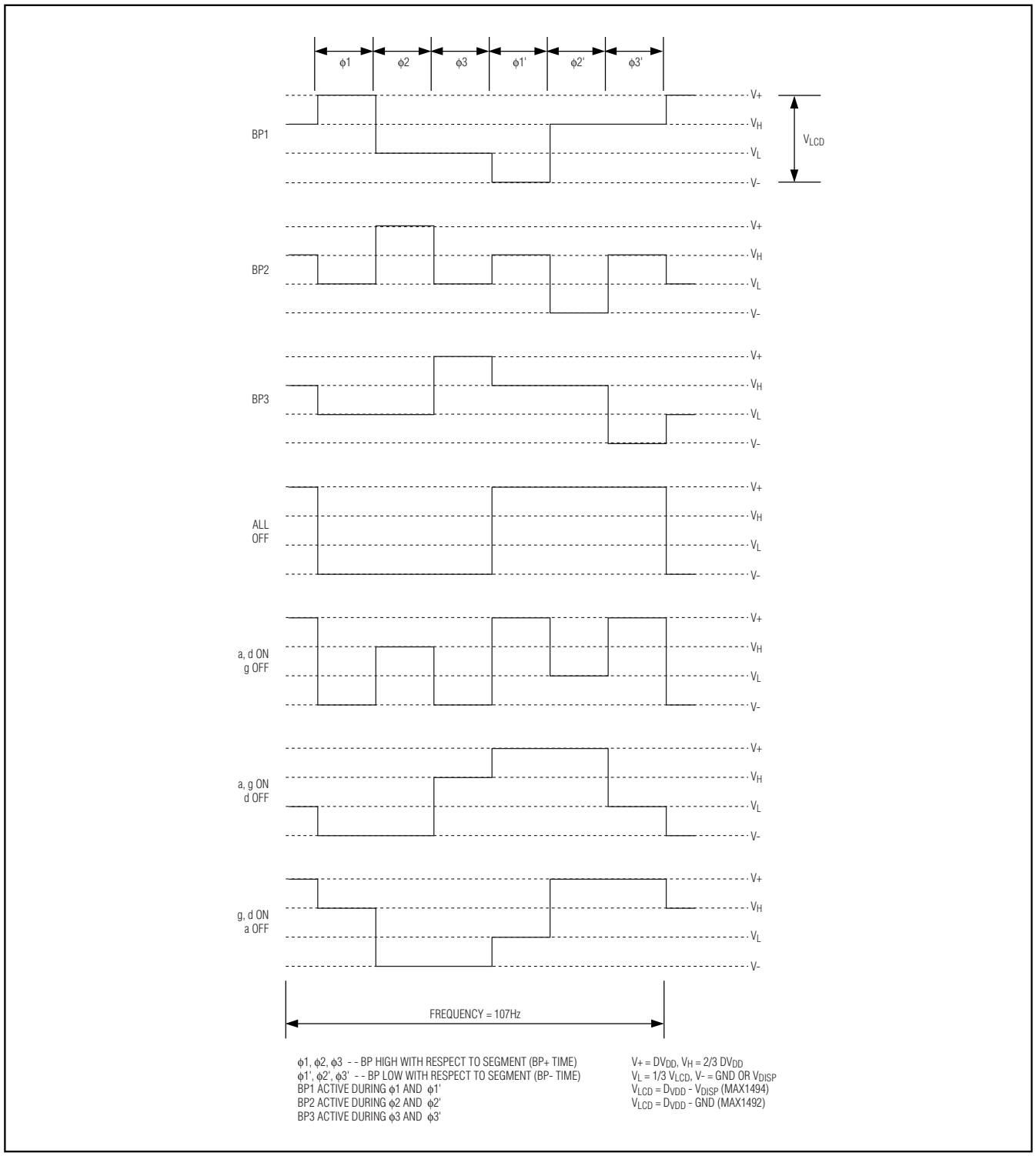
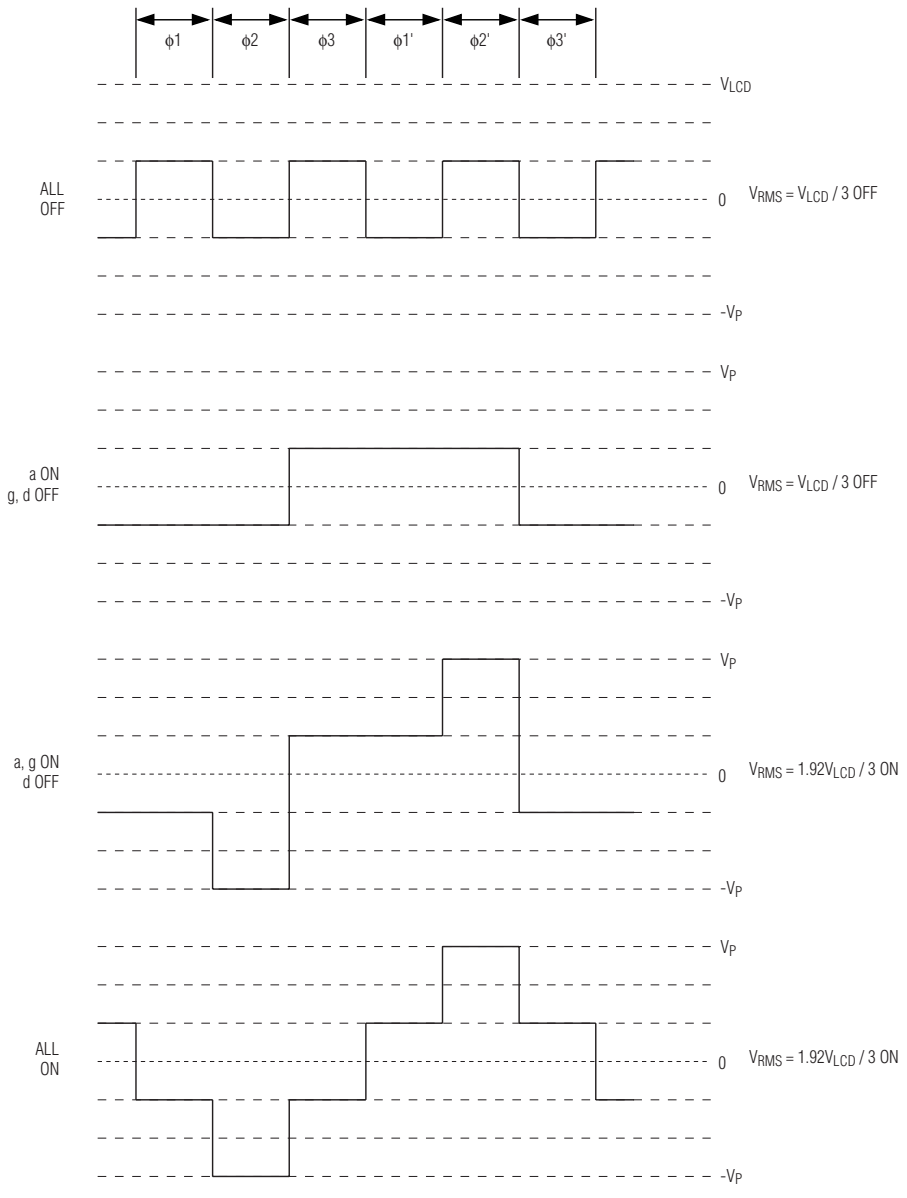


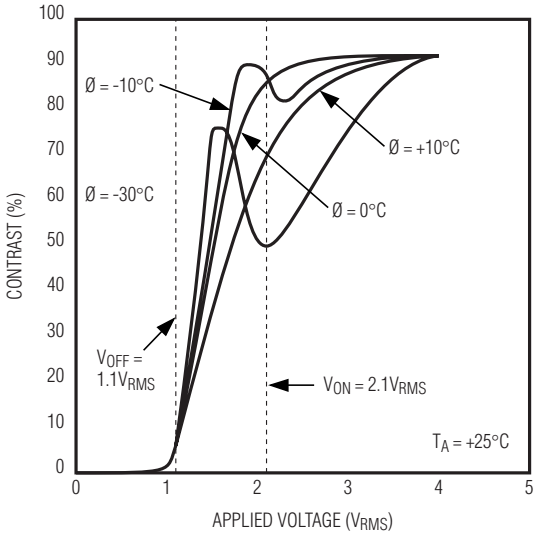
Figure 10. LCD Voltage Waveform—Combinations 5–8 (BP_, SEG2/5/8)



$V_G = V_Y - V_{BP2}$ (DIFFERENCE BETWEEN SEGMENT LINE Y AND BP2 VOLTAGE)
VOLTAGE CONTRAST RATIO = V_{RMS} ON / V_{RMSOFF} = 1.922V

ϕ1, ϕ2, ϕ3 - - BP HIGH WITH RESPECT TO SEGMENT (BP+ TIME)
ϕ1', ϕ2', ϕ3' - - BP LOW WITH RESPECT TO SEGMENT (BP- TIME)
BP1 ACTIVE DURING ϕ1 AND ϕ1'
BP2 ACTIVE DURING ϕ2 AND ϕ2'
BP3 ACTIVE DURING ϕ3 AND ϕ3'

Figure 11. Voltage Waveforms on the g Segment



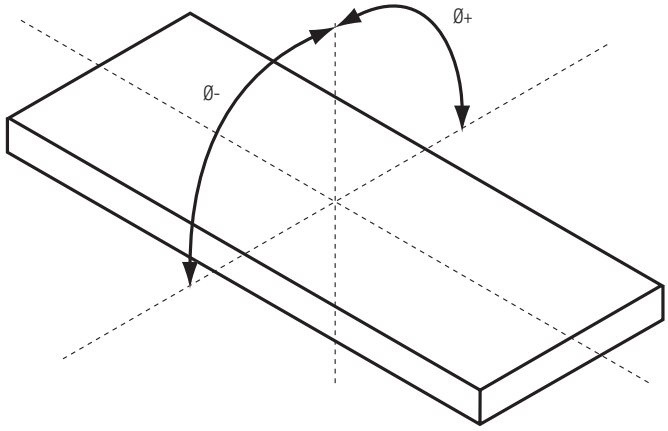


Figure 12. Contrast vs. Applied RMS Voltage

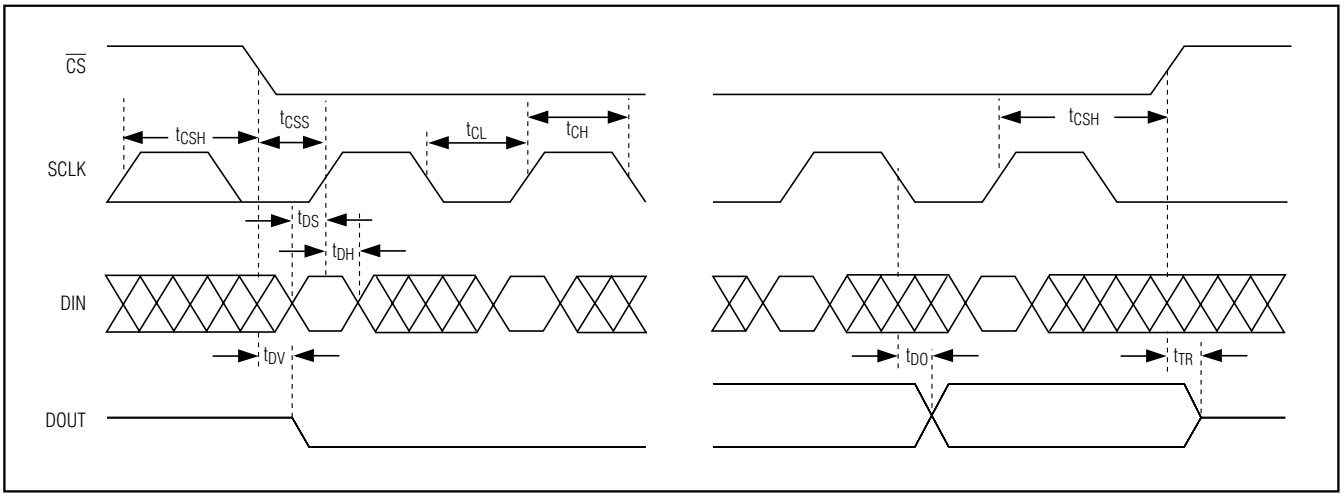


Figure 13. Detailed Timing Diagram

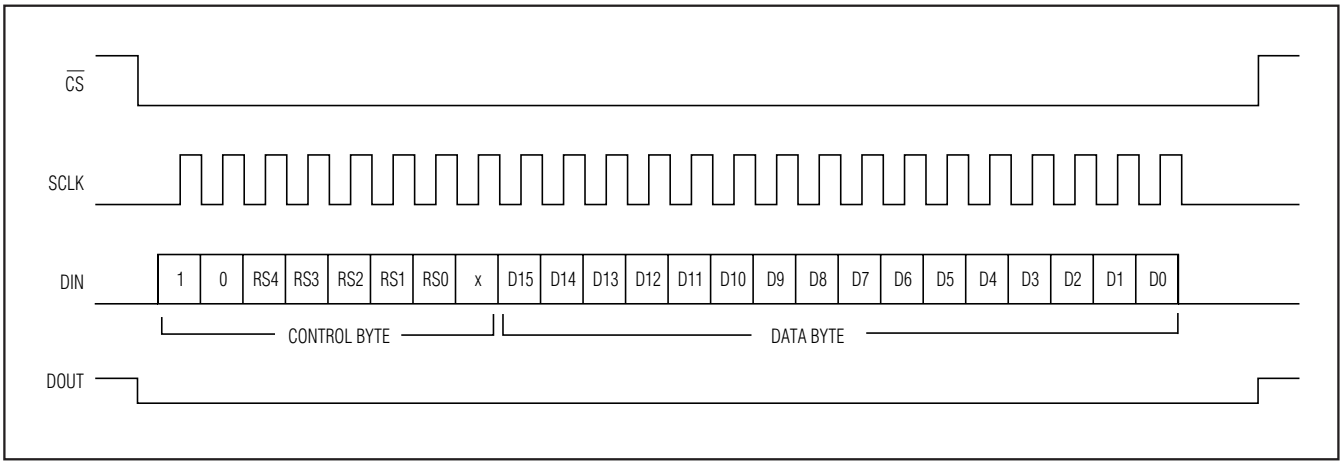


Figure 14. Serial-Interface 16-Bit Write Timing Diagram

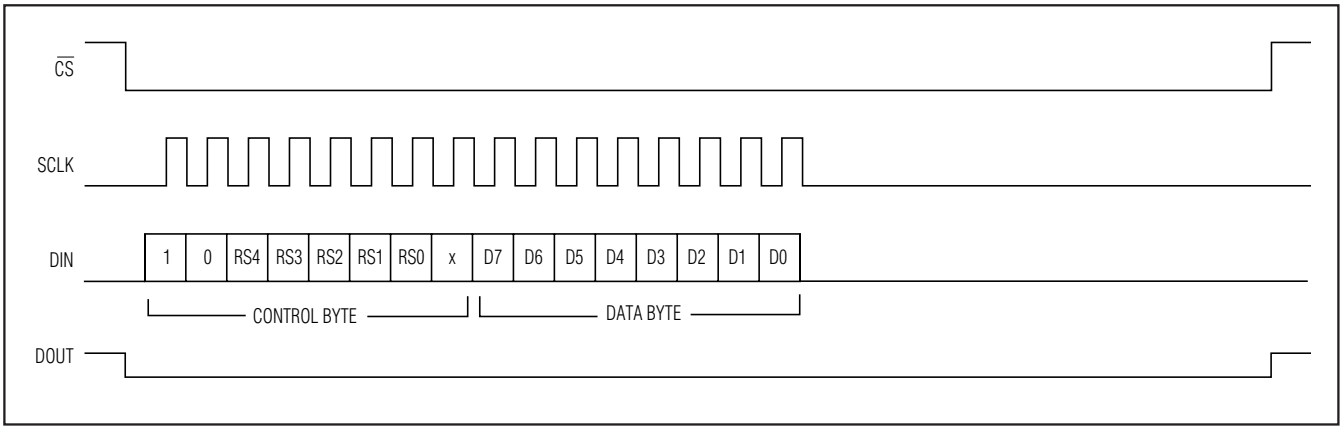


Figure 15. Serial-Interface 8-Bit Write Timing Diagram

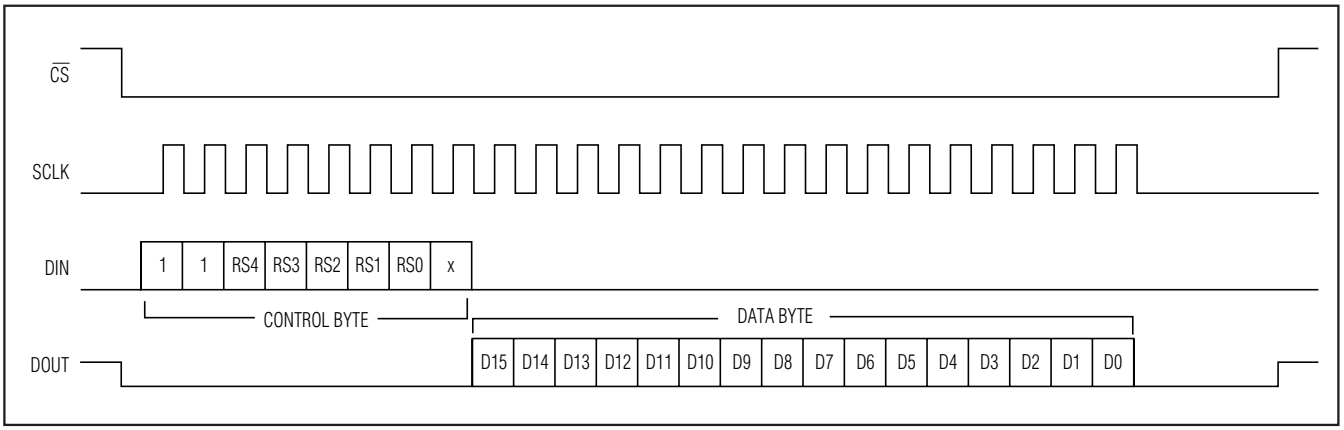


Figure 16. Serial-Interface 16-Bit Read Timing Diagram

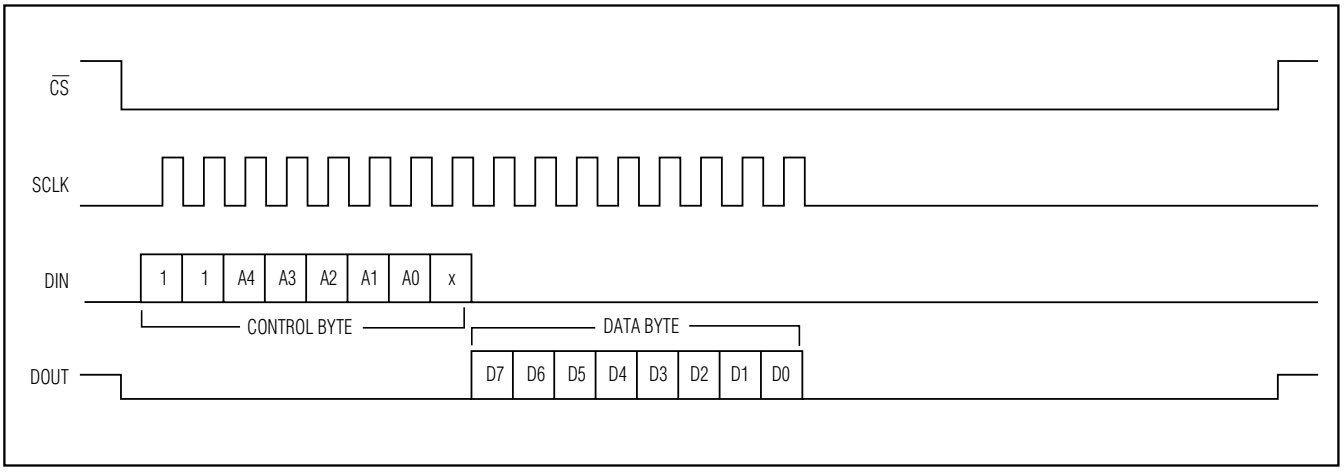


Figure 17. Serial-Interface 8-Bit Read Timing Diagram

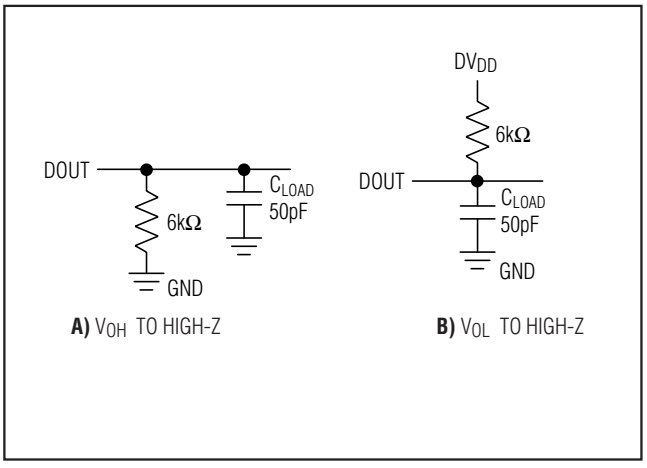


Figure 18. Load Circuits for Disable Time

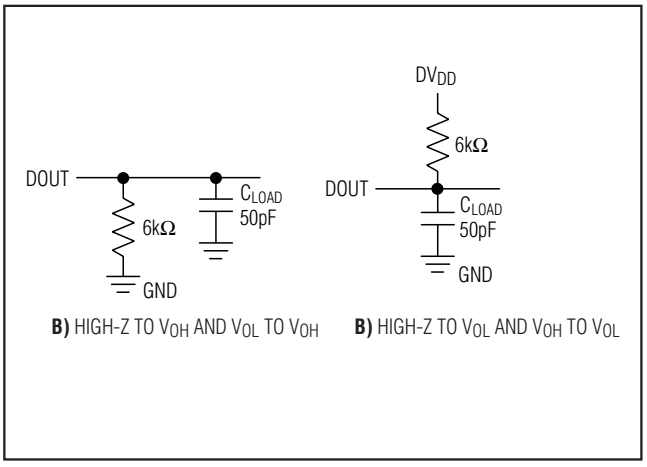


Figure 19. Load Circuits for Enable Time

Applications Information

Serial Interface

The SPI/QSPI/MICROWIRE serial interface consists of a chip select ($\overline{CS}$), a serial clock (SCLK), a data in (DIN), a data out (DOUT), and an asynchronous $\overline{EOC}$ output. $\overline{EOC}$ provides an asynchronous end-of-conversion signal with a period of 200ms (f_{CLK} = 4.9152MHz or internal clock mode). The MAX1492 updates the data register when $\overline{EOC}$ goes high. Data is valid in the ADC result registers when $\overline{EOC}$ returns low. The serial interface provides access to 12 on-chip registers, allowing control to all the power modes and functional blocks. Table 5 lists the address and read/write accessibility of all the registers.

A logic-high on $\overline{CS}$ tri-states DOUT and causes the MAX1492/MAX1494 to ignore any signals on SCLK and DIN. To clock data into or out of the internal shift register, drive $\overline{CS}$ low. SCLK synchronizes the data transfer. The rising edge of SCLK clocks DIN into the shift register, and the falling edge of SCLK clocks DOUT out of the shift register. DIN and DOUT are transferred MSB-first (data is left justified). Figures 13–17 show the detailed serial-interface timing diagrams for the 8- and 16-bit read/write operations.

All communication with the MAX1492/MAX1494 begins with a command byte on DIN, where the first logic 1 on DIN is recognized as the START bit (MSB) for the command byte. The following seven clock cycles load the command into a shift register. These 7 bits specify which of the registers are accessed next, and whether a read or write operation takes place. Transitions on the serial clock after the command byte transfer cause a write or read from the device until the correct number of bits have been transferred (8 or 16). Once this has occurred, the MAX1492/MAX1494 wait for the next command byte. $\overline{CS}$ must not go high between data transfers. If $\overline{CS}$ is toggled before the end of a write or read operation, the device mode may be unknown. Clock in 32 zeros to clear the device state and reset the interface so it is ready to receive a new command byte.

On-Chip Registers

The MAX1492/MAX1494 contain 12 on-chip registers. These registers configure the various functions of the device and allow independent reading of the ADC results and writing to the LCD. Table 5 lists the address and size of each register.

The first of these registers is the status register. The 8-bit status register contains the status flags for the ADC. The second register is the 16-bit control register. This register sets the LCD controls, range modes, power-down modes, offset calibration, and the reset-register function (CLR). The third register is the 16-bit overrange register, which sets the overrange limit of the analog input. The fourth register is the 16-bit underrange register, which sets the underrange limit of the analog input. Registers 5 through 7 contain the display data for the individual segments of the LCD. The eighth register contains the custom offset value. The ninth register contains the 16 MSBs of the ADC conversion result. The tenth register contains the LCD data. The eleventh register contains the peak analog input value. The last register contains the lower 4 LSBs of the 20-bit ADC conversion result.

Table 5. Register Address Table

REGISTER NUMBER	ADDRESS RS [4:0]	NAME	WIDTH	ACCESS
1	00000	Status Register	8	Read only
2	00001	Control Register	16	R/$\overline{W}$
3	00010	Overrange Register	16	R/$\overline{W}$
4	00011	Underrange Register	16	R/$\overline{W}$
5	00100	LCD Segment-Display Register 1	16	R/$\overline{W}$
6	00101	LCD Segment-Display Register 2	16	R/$\overline{W}$
7	00110	LCD Segment-Display Register 3	8	R/$\overline{W}$
8	00111	ADC Custom-Offset Register	16	R/$\overline{W}$
9	01000	ADC Result-Register 1 (16 MSBs)	16	Read only
10	01001	LCD Data Register	16	R/$\overline{W}$
11	01010	Peak Register	16	Read only
12	10100	ADC Result-Register 2 (4 LSBs)	8	Read only
—	All Other Addresses	Reserved	—	—

3.5- and 4.5-Digit, Single-Chip ADCs with LCD Drivers

Command Byte (Write Only):

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
START (1)	R/$\overline{W}$	RS4	RS3	RS2	RS1	RS0	X

START: Start Bit. The first 1 clocked into the MAX1492/MAX1494 is the first bit of the command byte.

(R/$\overline{W}$): Read/$\overline{\text{Write}}$. Set this bit to 1 to read from the specified register. Set this bit to 0 to write to the selected register. Note that certain registers are read-only. Write commands to a read-only register are ignored.

(RS4–RS0): Register Address Bits. RS4 to RS0 specify which register is accessed.

X: Don't care.

Status Register (Read Only):

MSB							LSB
SIGN	OVER	UNDER	LOW_BATT	DRDY	0	0	0

Default values: 00h

This register contains the status of the conversion results.

SIGN: Latched Negative-Polarity Indicator. Latches high when the result is negative. Clears by reading the status register, unless the condition remains true.

OVER: Overrange Bit. Latches high if an overrange condition occurs (the ADC result is larger than the value in the overrange register). Clears by reading the status register, unless the condition remains true.

UNDER: Underrange Bit. Latches high if an underrange condition occurs (the ADC result is less than the value in the underrange register). Clears by reading the status register, unless the condition remains true.

LOW_BATT: Low-Battery Bit. Latches high if the voltage at the LOWBATT is lower than 2.048V (typ). Clears by reading the status register, unless the condition remains true.

DRDY: Data-Ready Bit. Latches high to indicate a completed conversion result with valid data. Read the ADC Result-Register 1 to clear this bit.

Control Register (Read/Write):

MSB							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
SPI/$\overline{ADC}$	EXTCLK	INTREF	DP_EN	DPSET2	DPSET1	PD_DIG	PD_ANA
							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HOLD	PEAK	RANGE	CLR	SEG_SEL	$\overline{\text{OFFSET\_CAL1}}$	OFFSET_CAL2	0

Default values: 0000h

This register is the primary control register for the MAX1492/MAX1494. It is a 16-bit read/write register. It is used to indicate the desired clock and reference source. It sets the LCD controls, range modes, power-down modes, offset calibration, and the reset register function (CLR).

SPI/$\overline{ADC}$: (Default = 0) Display Select Bit. The SPI/$\overline{ADC}$ bit controls selection of the data fed into the LCD data register. A 1 in this location selects SPI/QSPI/MICROWIRE data (the user writes this data to the LCD data register). A 0 in this location selects the ADC result register data, unless hold or peak functions are active (see Table 6).

EXTCLK: (Default = 0) External Clock Select Bit. The EXTCLK bit controls selection of the internal clock or an external clock source. A 1 in this location selects the signal at the CLK input as the clock source. A 0 in this location selects the internal clock oscillator. Toggle the PD_DIG and PD_ANA after changing the EXTCLK bit.

INTREF: (Default = 0) Reference Select Bit. For internal reference operation, set INTREF to 1. For external reference operation, set INTREF to 0.

DP_EN: (Default = 0) Decimal-Point Enable Bit. See Tables 2 and 3.

DPSET[2:1]: (Default = 00) Decimal-Point Selection Bits. See Tables 2 and 3.

HOLD: (Default = 0) Hold Bit. When set to 1, the LCD register does not update from the ADC conversion results and holds the last result on the LCD. The MAX1492/MAX1494 continue to perform conversions during HOLD (see Table 6).

PEAK: (Default = 0) Peak Bit. When set to 1 (and the HOLD bit is set to 0), the LCD shows the result stored in the peak register (see Table 6).

PD_ANA: (Default = 0) Power-Down Analog Select Bit. When set to 1, the analog circuits (analog modulator and ADC input buffers) go into the power-down mode. When set to 0, the device is in full power-up mode.

PD_DIG: (Default = 0) Power-Down Digital Select Bit. When set to 1, the digital circuits (digital filter and LCD drivers) go into power-down mode. This also resets the values of the internal SRAM (in the digital filter) to zeros. When set to 0, the device returns to full power-up mode.

RANGE: (Default = 0) Input-Range Select Bit. When set to 0, the input voltage range is ±2V. When set to 1, the input voltage range is ±200mV. Toggle the PD_DIG and PD_ANA after changing the RANGE bit.

CLR: (Default = 0) Clear-All-Registers Bit. When set to 1, all the registers reset to their power-on reset states when $\overline{CS}$ makes a low-to-high transition.

SEG_SEL: (Default = 0) LCD Segment-Selection Bit. When set to 1, the LCD segment drivers use the LCD segment registers to display individual segments that can form letters or numbers or other information on the display. The LCD data register is NOT displayed. Send the data first to the LCD segment-display registers and then set this bit high (see Table 6).

$\overline{OFFSET}$_$\overline{CAL1}$: (Default = 0) Automatic-Offset Enable Bit. When set to 1, the MAX1492/MAX1494 disable automatic offset calibration. When this bit is set to 0, automatic offset calibration is enabled.

OFFSET_CAL2: (Default = 0) Enhanced Offset-Calibration Start Bit (MAX1494 Only and RANGE = 1). To achieve the lowest possible offset in the ±200mV input range, perform an enhanced offset calibration by setting this bit to 1. The calibration takes about 9 cycles (1800ms). After the calibration completes, set this bit to 0 to resume ADC conversions.

Note: When changing any one of the following control bits: $\overline{OFFSET}$_$\overline{CAL1}$, RANGE, PD_ANA, PD_DIG, INTREF, and EXTCLK, wait 800ms before reading the ADC results.

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Table 6. LCD Priority Table

SEG_SEL	SPI/$\overline{ADC}$	HOLD	PEAK	DISPLAYS VALUES FROM
1	X	X	X	LCD Segment Registers
0	1	X	X	LCD Display Register (User Written)
0	0	1	X	LCD Display Register
0	0	0	1	Peak Register
0	0	0	0	ADC Result Register

X = Don't care.

Overrange Register (Read/Write):

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Default values: 7CF0h (for MAX1492, +1999)

4E1Fh (for MAX1494, +19,999)

The overrange register is a 16-bit read/write register (D15 is the MSB). When the conversion result exceeds the value in the overrange register, the OVER bit in the status register latches to 1. The LCD shows a 1 followed by 4 dashes for the MAX1494 or a 1 followed by 3 dashes for the MAX1492 (see Table 4).

The data is represented in two's complement format.

Underrange Register (Read/Write):

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Default values: 8300h (for MAX1492, -2000)

B1E0h (for MAX1494, -20,000)

The underrange data register is 16-bit read/write register (D15 is the MSB). When the conversion result falls below the value in the underrange register, the UNDR bit in the status register sets to 1. The LCD shows a -1 followed by 4 dashes for the MAX1494 or a -1 followed by 3 dashes for the MAX1492 (see Table 4).

The data is represented in two's complement format.

LCD Segment-Display Register 1 (Read/Write):

MSB															LSB
$\overline{A2}$	$\overline{G2}$	$\overline{D2}$	$\overline{F2}$	$\overline{E2}$	$\overline{DP2}$	$\overline{ANN}$	$\overline{B1}$	$\overline{C1}$	$\overline{A1}$	$\overline{G1}$	$\overline{D1}$	$\overline{F1}$	$\overline{E1}$	$\overline{DP1}$	0

Default values: 0000h

The LCD segment-display register 1 is a 16-bit read/write register. When the SEG_SEL bit (in the control register) is set to 1, the MAX1492/MAX1494 provide direct access to individual LCD segments. The bits in the LCD segment-display register determine if a segment is on or off. Write a 0 to this register to turn on a segment and a 1 to turn off a segment.

$\overline{DP1}$: Segment DP Driver Bit of Digit 1. The default value turns on the LCD segment.

$\overline{E1}$: Segment e Driver Bit of Digit 1. The default value turns on the LCD segment.

$\overline{F1}$: Segment f Driver Bit of Digit 1. The default value turns on the LCD segment.

$\overline{D1}$: Segment d Driver Bit of Digit 1. The default value turns on the LCD segment.

$\overline{G1}$: Segment g Driver Bit of Digit 1. The default value turns on the LCD segment.

$\overline{A1}$: Segment a Driver Bit of Digit 1. The default value turns on the LCD segment.

$\overline{C1}$: Segment c Driver Bit of Digit 1. The default value turns on the LCD segment.

$\overline{B1}$: Segment b Driver Bit of Digit 1. The default value turns on the LCD segment.

$\overline{ANN}$: Custom Annunciator. The default value turns on the LCD segment.

$\overline{DP2}$: Segment DP Driver Bit of Digit 2. The default value turns on the LCD segment.

$\overline{E2}$: Segment e Driver Bit of Digit 2. The default value turns on the LCD segment.

$\overline{F2}$: Segment f Driver Bit of Digit 2. The default value turns on the LCD segment.

$\overline{D2}$: Segment d Driver Bit of Digit 2. The default value turns on the LCD segment.

$\overline{G2}$: Segment g Driver Bit of Digit 2. The default value turns on the LCD segment.

$\overline{A2}$: Segment a Driver Bit of Digit 2. The default value turns on the LCD segment.

LCD Segment-Display Register 2 (Read/Write):

MSB															LSB
$\overline{F4}$	$\overline{E4}$	$\overline{DP4}$	$\overline{MINUS}$	$\overline{B3}$	$\overline{C3}$	$\overline{A3}$	$\overline{G3}$	$\overline{D3}$	$\overline{F3}$	$\overline{E3}$	$\overline{DP3}$	$\overline{LOW\ BATT}$	$\overline{B2}$	$\overline{C2}$	0

Default values: 0000h

The LCD segment-display register 2 is a 16-bit read/write register. When the SEG_SEL bit (in the control register) is set to 1, the MAX1492/MAX1494 provide direct access to individual LCD segments. The bits in the LCD segment-display register determine if a segment is on or off. Write a 0 to this register to turn on a segment and a 1 to turn off a segment.

$\overline{C2}$: Segment c Driver Bit of Digit 2. The default value turns on the LCD segment.

$\overline{B2}$: Segment b Driver Bit of Digit 2. The default value turns on the LCD segment.

$\overline{LOWBATT}$: LOWBATT Driver Bit. The default value turns on the LOWBATT annunciator.

$\overline{DP3}$: Segment DP Driver Bit of Digit 3. The default value turns on the LCD segment.

$\overline{E3}$: Segment e Driver Bit of Digit 3. The default value turns on the LCD segment.

$\overline{F3}$: Segment f Driver Bit of Digit 3. The default value turns on the LCD segment.

$\overline{D3}$: Segment d Driver Bit of Digit 3. The default value turns on the LCD segment.

$\overline{G3}$: Segment g Driver Bit of Digit 3. The default value turns on the LCD segment.

$\overline{A3}$: Segment a Driver Bit of Digit 3. The default value turns on the LCD segment.

$\overline{C3}$: Segment c Driver Bit of Digit 3. The default value turns on the LCD segment.

$\overline{B3}$: Segment b Driver Bit of Digit 3. The default value turns on the LCD segment.

$\overline{MINUS}$: Minus-Sign Driver Bit. The default value turns on the LCD segment.

$\overline{DP4}$: Segment DP Driver Bit of Digit 4. The default value turns on the LCD segment (MAX1494 only).

$\overline{E4}$: Segment e Driver Bit of Digit 4. The default value turns on the LCD segment (MAX1494 only).

$\overline{F4}$: Segment f Driver Bit of Digit 4. The default value turns on the LCD segment (MAX1494 only).

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LCD Segment-Display Register 3 (Read/Write):

MSB							LSB
$\overline{PEAK}$	$\overline{HOLD}$	$\overline{BC\_}$	$\overline{B4}$	$\overline{C4}$	$\overline{A4}$	$\overline{G4}$	$\overline{D4}$

Default values: 00h

The LCD segment-display register 3 is an 8-bit read/write register. When the SEG_SEL bit (in the control register) is set to 1, the MAX1492/MAX1494 provide direct access to individual LCD segments. The bits in the LCD segment-display register determine if a segment is on or off. Write a 0 to turn on a segment and a 1 to turn off a segment.

$\overline{D4}$: Segment d Driver Bit of Digit 4. The default value turns on the LCD segment (MAX1494 only).

$\overline{G4}$: Segment g Driver Bit of Digit 4. The default value turns on the LCD segment (MAX1494 only).

$\overline{A4}$: Segment a Driver Bit of Digit 4. The default value turns on the LCD segment (MAX1494 only).

$\overline{C4}$: Segment c Driver Bit of Digit 4. The default value turns on the LCD segment (MAX1494 only).

$\overline{B4}$: Segment b Driver Bit of Digit 4. The default value turns on the LCD segment (MAX1494 only).

$\overline{BC\_}$: Segment bc_ Driver Bit. For the MAX1494, this bit enables BC5. For the MAX1492, this bit enables BC4. The default value turns on the LCD segment.

$\overline{HOLD}$: HOLD-Sign Driver Bit. The default value turns on the HOLD annunciator.

$\overline{PEAK}$: PEAK-Sign Driver Bit. The default value turns on the PEAK annunciator.

ADC Custom Offset-Calibration Register (Read/Write):

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Default values: 0000h

In addition to automatic offset calibration, the MAX1492/MAX1494 offer a user-defined custom-offset 16-bit read/write register. The final result of the ADC conversion is the input after autocalibration minus the value in the custom offset. The custom offset value is stored in this register. D15 is the MSB. The data is represented in two's complement format.

ADC Result-Register 1 (Read Only):

MSB												LSB (MAX1492)			LSB (MAX1494)
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Default values: 0000h

The ADC result-register 1 is a 16-bit read-only register. This register stores the 16 MSBs of the ADC result. The data is represented in two's complement format.

For the MAX1494, the data is 16-bit and D15 is the MSB. For the MAX1492, the data is 12-bit, D15 is the MSB, and D4 is the LSB.

LCD Data Register (Read/Write):

MSB															LSB (MAX1492) / LSB (MAX1494)
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Default values: 0000h

The LCD data register is a 16-bit read/write register. This register updates from the ADC result register 1, the PEAK register, or from the serial interface by selecting SPI/$\overline{ADC}$ bit, PEAK bit, and HOLD bit in the control register (see Table 6). The data is represented in two's complement format.

For the MAX1494, the data is 16-bit and D15 is the MSB. For the MAX1492, the data is 12-bit, D15 is the MSB, and D4 is the LSB, followed by four trailing sub-bits.

PEAK Register (Read Only):

MSB															LSB (MAX1492) / LSB (MAX1494)
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Default values: 0000h

The peak data register is a 16-bit read-only register. Set the PEAK bit to 1 to enable the PEAK function. This register stores the peak value of the ADC conversion result. First, the current ADC result is saved to the PEAK register. Then, the new ADC conversion result is compared to this value. If the new value is larger than the value in the peak register, the MAX1492/MAX1494 save the new value to the peak register. If the new value is less than the value in the peak register, the value in the peak register remains unchanged. Set the PEAK bit to 0 to clear the value in the PEAK register. The peak function is only valid for the range of -19,487 to +19,999 for the MAX1494 and -1217 to +1999 for the MAX1492.

The data is represented in two's complement format.

For the MAX1494, the data is 16-bit and D15 is the MSB. For the MAX1492, the data is 12-bit, D15 is the MSB, and D4 is the LSB followed by four trailing sub-bits.

ADC Result-Register 2 (Read Only):

MSB							LSB
D3	D2	D1	D0	0	0	0	0

Default values: 00h

The ADC result-register 2 is an 8-bit read-only register. This register stores the 4 LSBs of the ADC result. Use this result with the result in ADC result-register 1 to form a 20-bit two's complement conversion result.

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Power-On Reset

At power-up, the serial interface, LCD driver, digital filter, and modulator circuits reset. The registers return to their default values. Allow time for the reference to settle before starting calibration.

Offset Calibration

The MAX1492/MAX1494 offer on-chip offset calibration. The device offset-calibrates during every conversion when the $\overline{\text{OFFSET\_CAL1}}$ bit is 0. Enhanced offset calibration is only needed in the MAX1494 when RANGE = 1. It is performed on demand by setting the OFFSET_CAL2 bit to 1.

Power-Down Modes

The MAX1492/MAX1494 feature independent power-down control of the analog and digital circuitry. Writing a 1 to the PD_DIG and PD_ANA bits in the control register powers down the analog and digital circuitry, reducing the supply current to 400µA. PD_DIG powers down the digital filter and LCD drivers, while PD_ANA powers down the analog modulator and ADC input buffers.

V_{DISP} LCD Compensation (MAX1494 Only)

Adequate display contrast can be obtained in most applications by connecting V_{DISP} to GND. In applications where a wide temperature range is expected, the voltage levels for some triplexed LCDs may need to vary with temperature to maintain good display contrast and viewing angle. The amount of temperature compensation depends upon the type of liquid crystal used. Display manufacturers usually specify the temperature variation of the LCD thresholds voltage (RMS_{ON} - RMS_{OFF}), which is approximately 1/3 of the peak display voltage. The peak display voltage is equal to DV_{DD} - V_{DISP} (MAX1494 only). Therefore, a typical -4mV/°C temperature coefficient of an LCD threshold corresponds to a +12mV/°C temperature coefficient at V_{DISP}.

Peak

The MAX1492/MAX1494 feature peak-detection circuitry. When activated (PEAK bit = 1), the devices display only the highest voltage measured to the LCD.

Hold

The MAX1492/MAX1494 feature data-hold circuitry. When activated (HOLD bit = 1), the devices display the current reading on the LCD.

Low Battery

The MAX1492/MAX1494 feature a low-battery detection input. When the voltage at LOWBATT drops below 2.048V (typ), the LOWBATT bit of the status register goes high and the LOWBATT segment of the LCD turns on.

Strain Gauge Measurement

Connect the differential inputs of the MAX1492/MAX1494 to the bridge network of the strain gauge. In Figure 20, the analog supply voltage powers the bridge network and the MAX1492/MAX1494 along with the reference voltage. The MAX1492/MAX1494 handle an analog input-voltage range of ±200mV and ±2V full scale. The analog/reference inputs of the parts allow the analog input range to have an absolute value of anywhere between -2.2V and +2.2V.

Thermocouple Measurement

Figure 21 shows a connection from a thermocouple to the MAX1492/MAX1494. In this application, the MAX1492/MAX1494 take advantage of the on-chip input buffers that allow large source impedances on the front end. The decoupling capacitors reduce noise pickup from the thermocouple leads. To place the differential voltage from the thermocouple at a suitable common-mode voltage, the AIN- input of the MAX1492/MAX1494 is biased to GND. Use an external temperature sensor, such as the DS75, and a µC to perform cold junction-temperature compensation.

4–20mA Transmitter

Low-power, single-supply operations make the MAX1492/MAX1494 ideal for loop-powered 4–20mA transmitters. Loop-powered transmitters draw their power from the 4–20mA loop, limiting the transmitter circuitry to a current budget of 4mA. Tolerances in the loop further limit this current budget to 3.5mA. Since the MAX1492/MAX1494 only consume 950µA, a total of 2.55mA remains to power the remaining transmitter circuitry. Figure 22 shows a block diagram for a loop-powered 4–20mA transmitter.

4–20mA Measurement

To measure 4–20mA signals, connect a shunt resistor across AIN+ and AIN- to create the ±2V or ±200mV input voltage (Figure 23).

Transfer Functions

Figures 24–27 show the transfer functions of the MAX1492/MAX1494. The output data is stored in the ADC data register in two's complement.

A -1 in the ADC result register displays -0 on the LCD as shown in Figures 24–27. Negative values on the LCD are offset by 1. For example, -100 in the ADC result register appears as -99 on the LCD.

Supplies, Layout, and Bypassing

When using analog and digital supplies from the same source, isolate the digital supply from the analog supply with a low-value resistor (10Ω) or ferrite bead. For

best performance, ground the MAX1492/MAX1494 to the analog ground plane of the circuit board.

Avoid running digital lines under the device because they can couple noise onto the device. Run the analog ground plane under the MAX1492/MAX1494 to minimize coupling of digital noise. Make the power-supply lines to the MAX1492/MAX1494 as wide as possible to provide low-impedance paths and reduce the effects of glitches on the power-supply line.

Shield fast-switching signals, such as clocks, with digital ground to avoid radiating noise to other sections of the board. Avoid running clock signals near the analog inputs. Avoid crossover of digital and analog signals. Running traces that are on opposite sides of the board at right angles to each other reduces feedthrough effects.

Good decoupling is important when using high-resolution ADCs. Decouple the supplies with 0.1µF and 4.7µF ceramic capacitors to GND. Place these components as close to the device as possible to achieve the best decoupling.

See the MAX1494 evaluation kit manual for the recommended layout. The evaluation kit includes a fully assembled and tested evaluation board.

Definitions

INL

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line is either a best-straight-line fit or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. INL for the MAX1492/MAX1494 is measured using the endpoint method.

DNL

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function.

Rollover Error

Rollover error is defined as the absolute-value difference between a near positive full-scale reading and near negative full-scale reading. Rollover error is tested by applying a near full-scale positive voltage, swapping AIN+ and AIN-, and then adding the results.

Zero Input Reading

Ideally, with AIN+ connected to AIN- the MAX1492/MAX1494 LCD is 0 or -0. Zero input reading is the measured deviation from the ideal 0 and the actual measured point.

Gain Error

Gain error is the amount of deviation between the measured full-scale transition point and the ideal full-scale transition point.

Common-Mode Rejection

Common-mode rejection (CMR) is the ability of a device to reject a signal that is common to both input terminals. The common-mode signal can be either an AC or a DC signal or a combination of the two. CMR is often expressed in decibels.

Normal-Mode 50Hz and 60Hz Rejection (Simultaneously)

Normal-mode rejection is a measure of how much output changes when a 50Hz and 60Hz signal is injected into only one of the differential inputs. The MAX1492/MAX1494 sigma-delta converter uses its internal digital filter to provide normal-mode rejection to both 50Hz and 60Hz power-line frequencies simultaneously.

Power-Supply Rejection Ratio

Power-supply rejection ratio (PSRR) is the ratio of the input-supply change (in volts) to the change in the converter output (in volts). It is typically measured in decibels.

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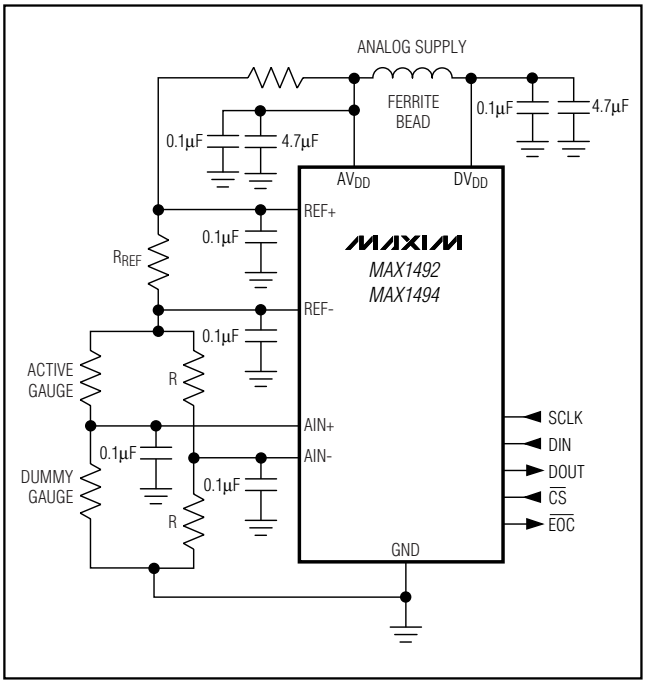

Figure 20. Strain-Gauge Application with MAX1492/MAX1494

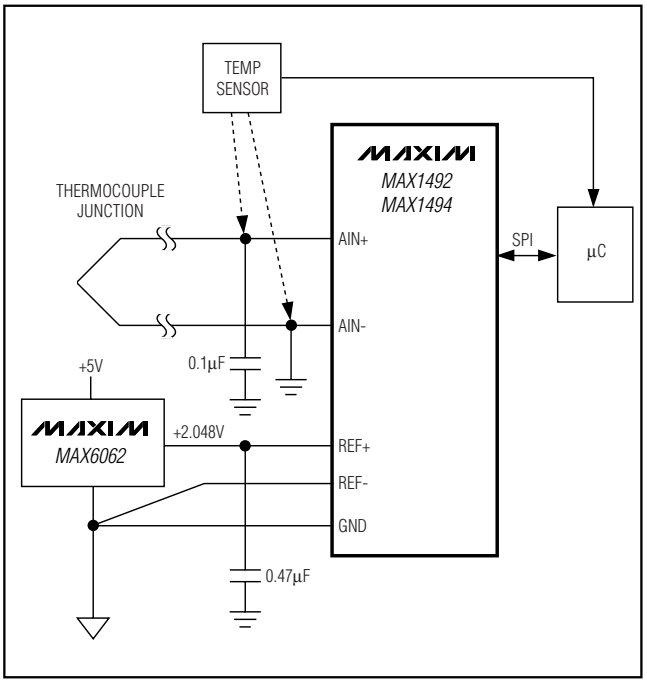

Figure 21. Thermocouple Application with MAX1492/MAX1494

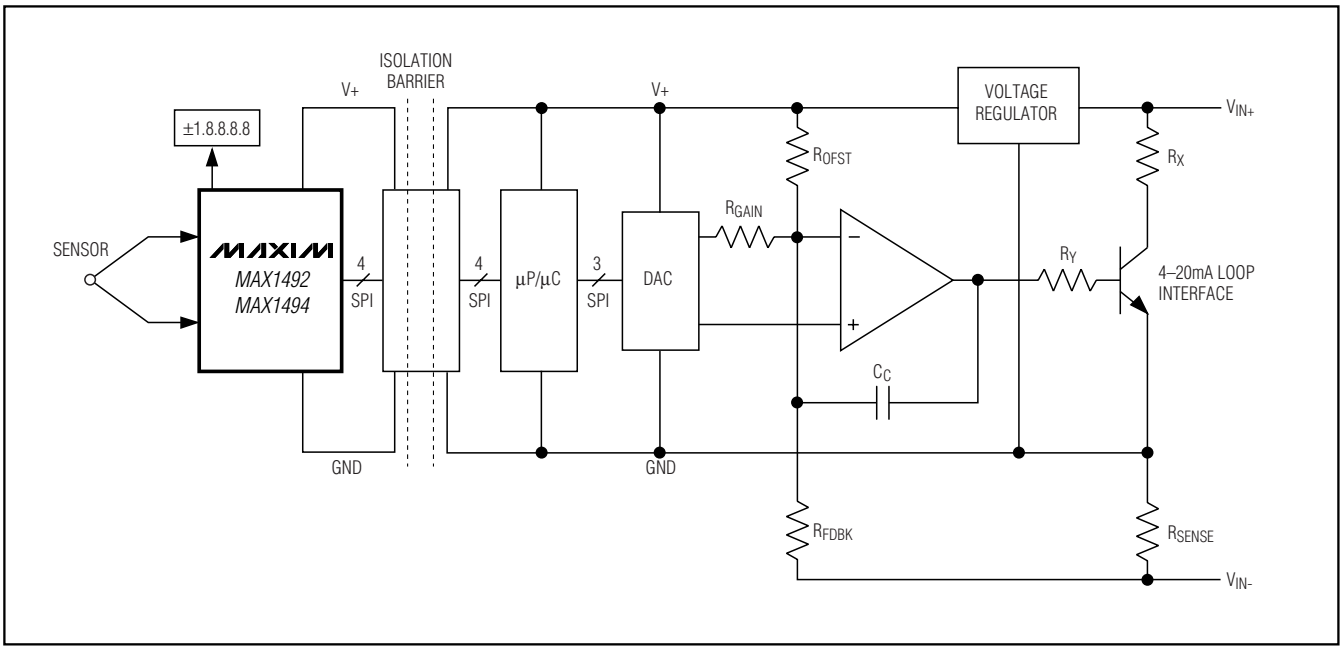

Figure 22. 4–20mA Transmitter

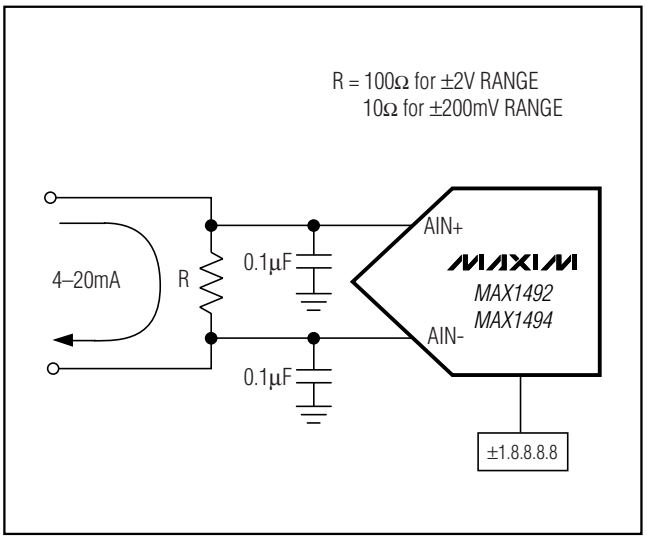

Figure 23. 4–20mA Measurement

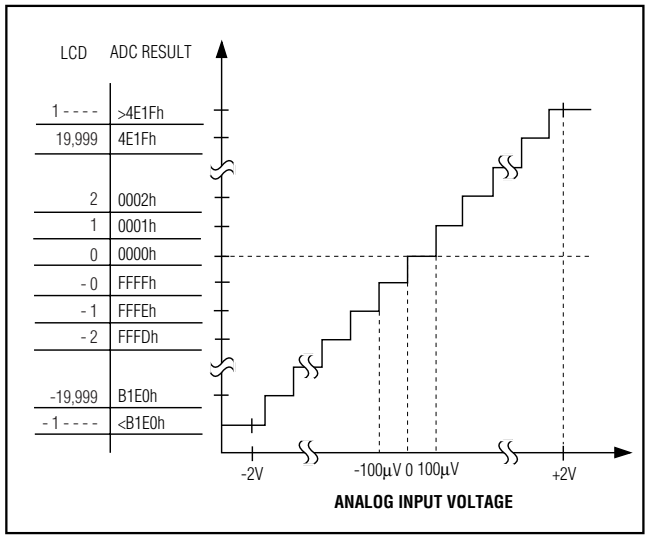

Figure 24. MAX1494 Transfer Function, ±2V Range

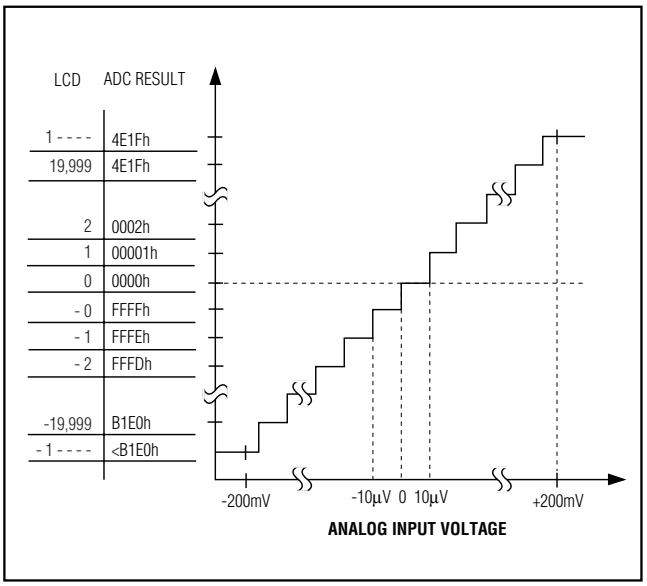

Figure 25. MAX1494 Transfer Function ±200mV Range

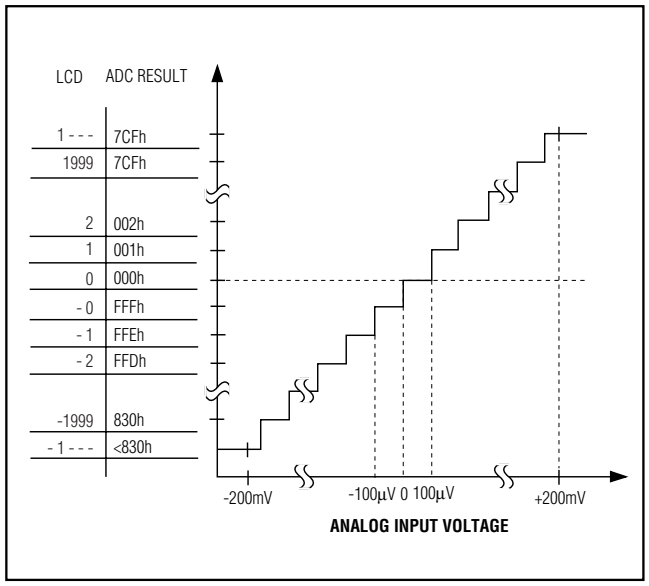

Figure 26. MAX1492 Transfer Function ±200mV Range

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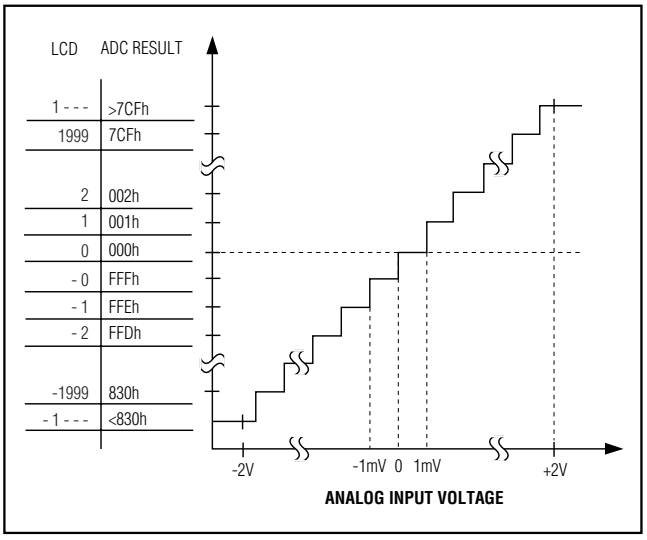
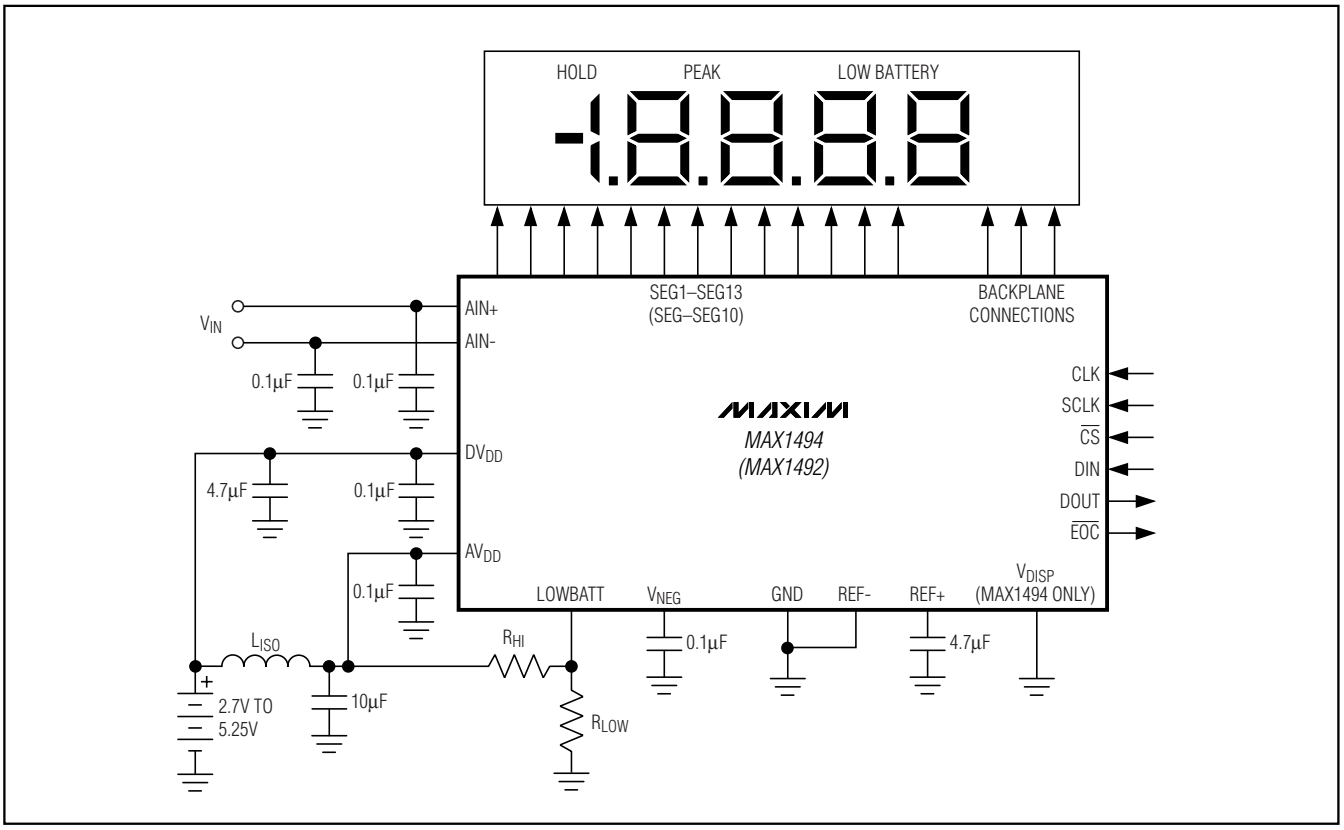


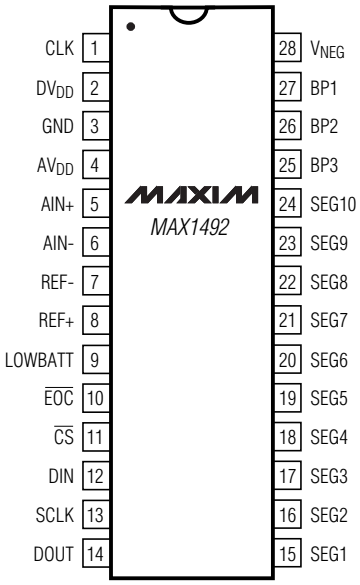
Figure 27. MAX1492 Transfer Function ±2V Range

Typical Operating Circuit

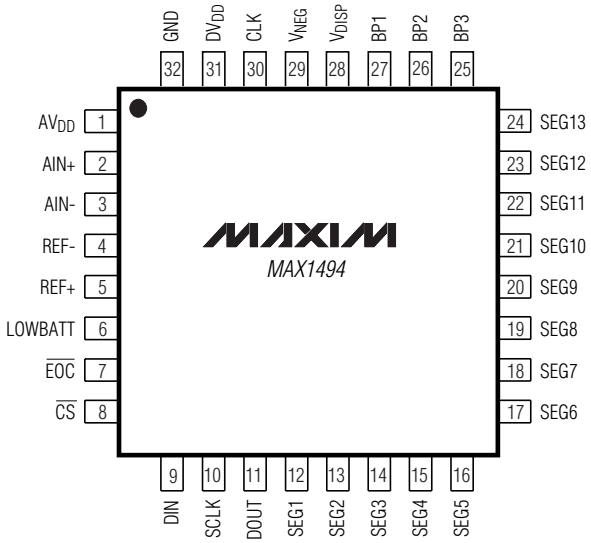


Pin Configurations

TOP VIEW



PDIP/SSOP



TQFP

Chip Information

TRANSISTOR COUNT: 79,435

PROCESS: BiCMOS

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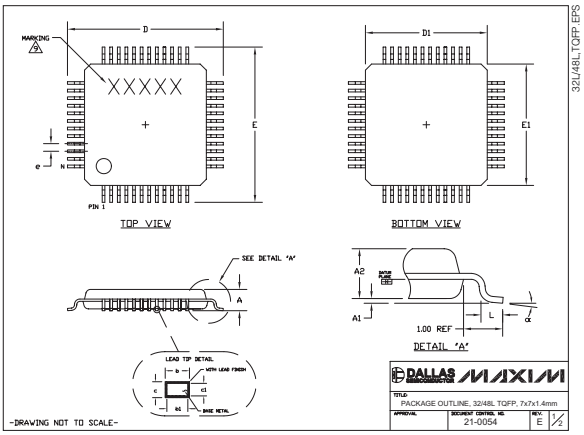
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

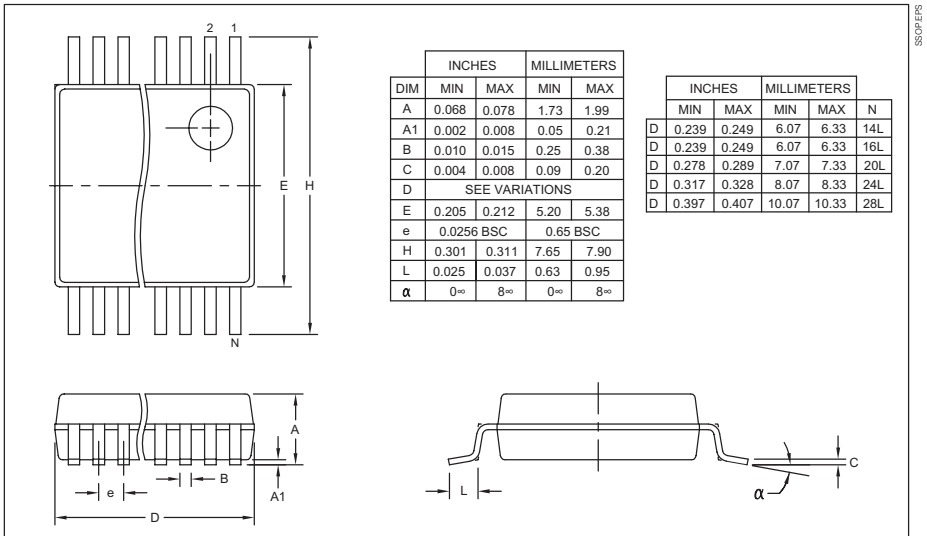
32L/48L,TQFP.EPS



NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊞ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
10. NUMBER OF LEADS ARE SHOWN FOR REFERENCE ONLY.

JEDEC VARIATION				
	BBA		BBC	
	MIN.	MAX.	MIN.	MAX.
A	---	1.60	---	1.60
A1	0.05	0.15	0.05	0.15
A2	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10
D1	6.90	7.10	6.90	7.10
E	8.90	9.10	8.90	9.10
E1	6.90	7.10	6.90	7.10
e	0.8 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27
b1	0.30	0.40	0.17	0.23
c	0.09	0.20	0.09	0.20
c1	0.09	0.16	0.09	0.16
N	32		48	
α	0°	7°	0°	7°

SSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0∞	8∞	0∞	8∞

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L

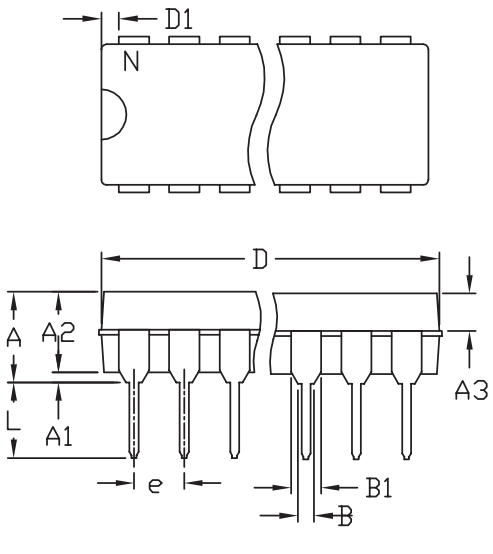
NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.
5. LEADS TO BE COPLANAR WITHIN 0.10 MM.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, SSOP, 5.3 MM
APPROVAL
DOCUMENT CONTROL NO.
21-0056
REV.
C
1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PDIPN.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.180	---	4.572
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.015	0.022	0.381	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.014	0.2	0.355
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100 BSC.		2.54 BSC.	
eA	0.300 BSC.		7.62 BSC.	
eB	0.400 BSC.		10.16 BSC.	
L	0.115	0.150	2.921	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM	PACKAGE FAMILY OUTLINE: PDIP .300"	1/1	21-0043 D
120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION	TITLE		DOCUMENT CONTROL NUMBER REV