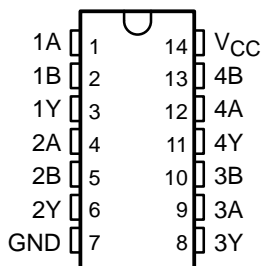


# SN54AHC00, SN74AHC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

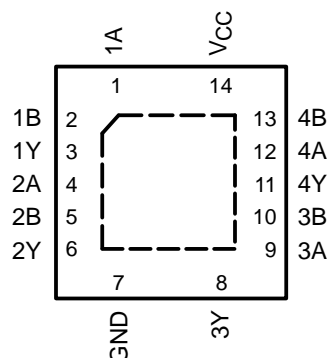
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- Operating Range 2-V to 5.5-V  $V_{CC}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

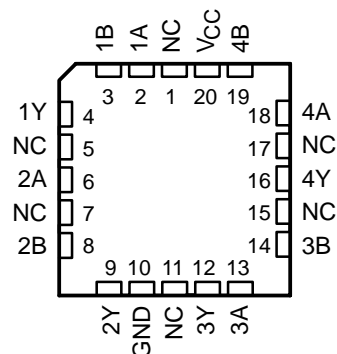
SN54AHC00 . . . J OR W PACKAGE  
SN74AHC00 . . . D, DB, DGV, N, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74AHC00 . . . RGY PACKAGE  
(TOP VIEW)



SN54AHC00 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'AHC00 devices perform the Boolean function  $Y = \overline{A} \cdot \overline{B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

## ORDERING INFORMATION

| $T_A$          | PACKAGE†    |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-------------|---------------|-----------------------|------------------|
| –40°C to 85°C  | QFN – RGY   | Tape and reel | SN74AHC00RGYR         | HA00             |
|                | PDIP – N    | Tube          | SN74AHC00N            | SN74AHC00N       |
|                | SOIC – D    | Tube          | SN74AHC00D            | AHC00            |
|                |             | Tape and reel | SN74AHC00DR           |                  |
|                | SOP – NS    | Tape and reel | SN74AHC00NSR          | AHC00            |
|                | SSOP – DB   | Tape and reel | SN74AHC00DBR          | HA00             |
|                | TSSOP – PW  | Tube          | SN74AHC00PW           | HA00             |
|                |             | Tape and reel | SN74AHC00PWR          |                  |
|                | TVSOP – DGV | Tape and reel | SN74AHC00DGVR         | HA00             |
| –55°C to 125°C | CDIP – J    | Tube          | SNJ54AHC00J           | SNJ54AHC00J      |
|                | CFP – W     | Tube          | SNJ54AHC00W           | SNJ54AHC00W      |
|                | LCCC – FK   | Tube          | SNJ54AHC00FK          | SNJ54AHC00FK     |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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INSTRUMENTS**

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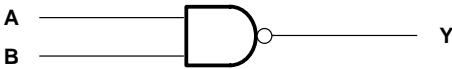
SN54AHC00, SN74AHC00  
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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FUNCTION TABLE  
(each gate)

| INPUTS |   | OUTPUT |
|--------|---|--------|
| A      | B | Y      |
| H      | H | L      |
| L      | X | H      |
| X      | L | H      |

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                  |                            |
|------------------------------------------------------------------|----------------------------|
| Supply voltage range, $V_{CC}$                                   | –0.5 V to 7 V              |
| Input voltage range, $V_I$ (see Note 1)                          | –0.5 V to 7 V              |
| Output voltage range, $V_O$ (see Note 1)                         | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                      | –20 mA                     |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )   | ±20 mA                     |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )       | ±25 mA                     |
| Continuous current through $V_{CC}$ or GND                       | ±50 mA                     |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): D package | 86°C/W                     |
| (see Note 2): DB package                                         | 96°C/W                     |
| (see Note 2): DGV package                                        | 127°C/W                    |
| (see Note 2): N package                                          | 80°C/W                     |
| (see Note 2): NS package                                         | 76°C/W                     |
| (see Note 2): PW package                                         | 113°C/W                    |
| (see Note 3): RGY package                                        | 47°C/W                     |
| Storage temperature range, $T_{stg}$                             | –65°C to 150°C             |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.  
3. The package thermal impedance is calculated in accordance with JESD 51-5.

# SN54AHC00, SN74AHC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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## recommended operating conditions (see Note 4)

|                 |                                    |                                 | SN54AHC00 |                 | SN74AHC00 |                 | UNIT |
|-----------------|------------------------------------|---------------------------------|-----------|-----------------|-----------|-----------------|------|
|                 |                                    |                                 | MIN       | MAX             | MIN       | MAX             |      |
| V <sub>CC</sub> | Supply voltage                     |                                 | 2         | 5.5             | 2         | 5.5             | V    |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 2 V           | 1.5       |                 | 1.5       |                 | V    |
|                 |                                    | V <sub>CC</sub> = 3 V           | 2.1       |                 | 2.1       |                 |      |
|                 |                                    | V <sub>CC</sub> = 5.5 V         | 3.85      |                 | 3.85      |                 |      |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 2 V           |           | 0.5             |           | 0.5             | V    |
|                 |                                    | V <sub>CC</sub> = 3 V           |           | 0.9             |           | 0.9             |      |
|                 |                                    | V <sub>CC</sub> = 5.5 V         |           | 1.65            |           | 1.65            |      |
| V <sub>I</sub>  | Input voltage                      |                                 | 0         | 5.5             | 0         | 5.5             | V    |
| V <sub>O</sub>  | Output voltage                     |                                 | 0         | V <sub>CC</sub> | 0         | V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 2 V           |           | –50             |           | –50             | μA   |
|                 |                                    | V <sub>CC</sub> = 3.3 V ± 0.3 V |           | –4              |           | –4              | mA   |
|                 |                                    | V <sub>CC</sub> = 5 V ± 0.5 V   |           | –8              |           | –8              |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 2 V           |           | 50              |           | 50              | μA   |
|                 |                                    | V <sub>CC</sub> = 3.3 V ± 0.3 V |           | 4               |           | 4               | mA   |
|                 |                                    | V <sub>CC</sub> = 5 V ± 0.5 V   |           | 8               |           | 8               |      |
| Δt/Δv           | Input transition rise or fall rate | V <sub>CC</sub> = 3.3 V ± 0.3 V |           | 100             |           | 100             | ns/V |
|                 |                                    | V <sub>CC</sub> = 5 V ± 0.5 V   |           | 20              |           | 20              |      |
| T <sub>A</sub>  | Operating free-air temperature     |                                 | –55       | 125             | –40       | 85              | °C   |

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER       | TEST CONDITIONS                                             | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |      | SN54AHC00 |     | SN74AHC00 |      | UNIT |
|-----------------|-------------------------------------------------------------|-----------------|-----------------------|-----|------|-----------|-----|-----------|------|------|
|                 |                                                             |                 | MIN                   | TYP | MAX  | MIN       | MAX | MIN       | MAX  |      |
| V <sub>OH</sub> | I <sub>OH</sub> = –50 μA                                    | 2 V             | 1.9                   | 2   |      | 1.9       |     | 1.9       |      | V    |
|                 |                                                             | 3 V             | 2.9                   | 3   |      | 2.9       |     | 2.9       |      |      |
|                 |                                                             | 4.5 V           | 4.4                   | 4.5 |      | 4.4       |     | 4.4       |      |      |
|                 | I <sub>OH</sub> = –4 mA                                     | 3 V             | 2.58                  |     |      | 2.48      |     | 2.48      |      |      |
|                 | I <sub>OH</sub> = –8 mA                                     | 4.5 V           | 3.94                  |     |      | 3.8       |     | 3.8       |      |      |
| V <sub>OL</sub> | I <sub>OL</sub> = 50 μA                                     | 2 V             |                       |     | 0.1  |           | 0.1 |           | 0.1  | V    |
|                 |                                                             | 3 V             |                       |     | 0.1  |           | 0.1 |           | 0.1  |      |
|                 |                                                             | 4.5 V           |                       |     | 0.1  |           | 0.1 |           | 0.1  |      |
|                 | I <sub>OL</sub> = 4 mA                                      | 3 V             |                       |     | 0.36 |           | 0.5 |           | 0.44 |      |
|                 | I <sub>OL</sub> = 8 mA                                      | 4.5 V           |                       |     | 0.36 |           | 0.5 |           | 0.44 |      |
| I <sub>I</sub>  | V <sub>I</sub> = 5.5 V or GND                               | 0 V to 5.5 V    |                       |     | ±0.1 |           | ±1* |           | ±1   | μA   |
| I <sub>CC</sub> | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5 V           |                       |     | 2    |           | 20  |           | 20   | μA   |
| C <sub>i</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 5 V             |                       | 2   | 10   |           |     |           | 10   | pF   |

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.



# SN54AHC00, SN74AHC00

## QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)**

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE    | T <sub>A</sub> = 25°C |      |     | SN54AHC00 |     | SN74AHC00 |     | UNIT |
|------------------|-----------------|----------------|------------------------|-----------------------|------|-----|-----------|-----|-----------|-----|------|
|                  |                 |                |                        | MIN                   | TYP  | MAX | MIN       | MAX | MIN       | MAX |      |
| t <sub>PLH</sub> | A or B          | Y              | C <sub>L</sub> = 15 pF | 5.5*                  | 7.9* | 1*  | 9.5*      | 1   | 9.5       | ns  |      |
| t <sub>PHL</sub> |                 |                |                        | 5.5*                  | 7.9* | 1*  | 9.5*      | 1   | 9.5       |     |      |
| t <sub>PLH</sub> | A or B          | Y              | C <sub>L</sub> = 50 pF | 8                     | 11.4 | 1   | 13        | 1   | 13        | ns  |      |
| t <sub>PHL</sub> |                 |                |                        | 8                     | 11.4 | 1   | 13        | 1   | 13        |     |      |

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE    | T <sub>A</sub> = 25°C |      |     | SN54AHC00 |     | SN74AHC00 |     | UNIT |
|------------------|-----------------|----------------|------------------------|-----------------------|------|-----|-----------|-----|-----------|-----|------|
|                  |                 |                |                        | MIN                   | TYP  | MAX | MIN       | MAX | MIN       | MAX |      |
| t <sub>PLH</sub> | A or B          | Y              | C <sub>L</sub> = 15 pF | 3.7*                  | 5.5* | 1*  | 6.5*      | 1   | 6.5       | ns  |      |
| t <sub>PHL</sub> |                 |                |                        | 3.7*                  | 5.5* | 1*  | 6.5*      | 1   | 6.5       |     |      |
| t <sub>PLH</sub> | A or B          | Y              | C <sub>L</sub> = 50 pF | 5.2                   | 7.5  | 1   | 8.5       | 1   | 8.5       | ns  |      |
| t <sub>PHL</sub> |                 |                |                        | 5.2                   | 7.5  | 1   | 8.5       | 1   | 8.5       |     |      |

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)**

| PARAMETER   |                                        | SN74AHC00 |      |     | UNIT |
|-------------|----------------------------------------|-----------|------|-----|------|
|             |                                        | MIN       | TYP  | MAX |      |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | 0.3       | 0.8  |     | V    |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | -0.3      | -0.8 |     | V    |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.6       |      |     | V    |
| $V_{IH(D)}$ | High-level dynamic input voltage       | 3.5       |      |     | V    |
| $V_{IL(D)}$ | Low-level dynamic input voltage        |           | 1.5  |     | V    |

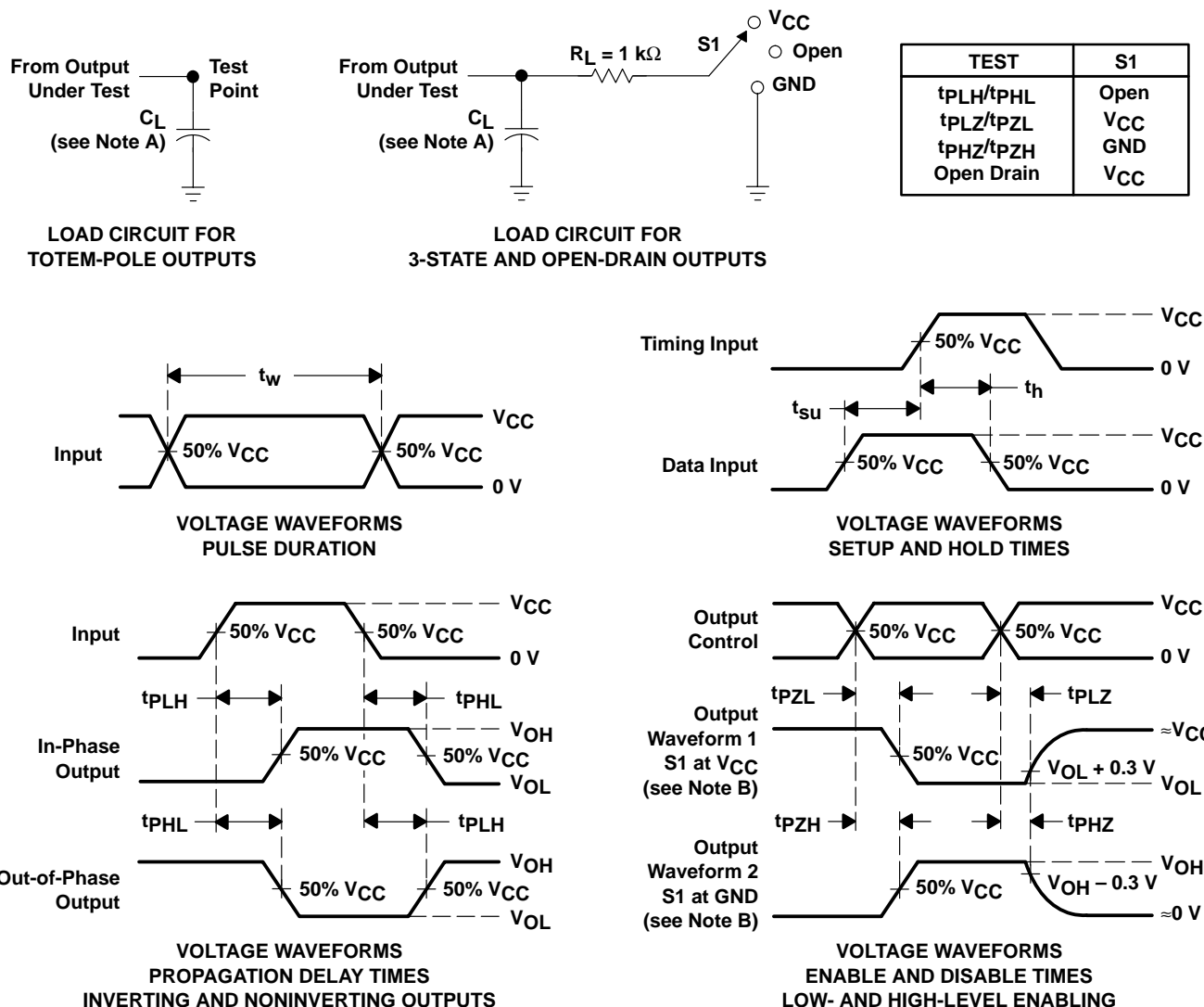
NOTE 5: Characteristics are for surface-mount packages only.

**operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

| PARAMETER |                               | TEST CONDITIONS             | TYP | UNIT |
|-----------|-------------------------------|-----------------------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance | No load, $f = 1\text{ MHz}$ | 9.5 | pF   |



# PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-9682201Q2A  | ACTIVE                | LCCC         | FK              | 20   | 1           | TBD                     | POST-PLATE       | N / A for Pkg Type           |
| 5962-9682201QCA  | ACTIVE                | CDIP         | J               | 14   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| 5962-9682201QDA  | ACTIVE                | CFP          | W               | 14   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| SN74AHC00D       | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC00DBLE    | OBSOLETE              | SSOP         | DB              | 14   |             | TBD                     | Call TI          | Call TI                      |
| SN74AHC00DBR     | ACTIVE                | SSOP         | DB              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC00DBRE4   | ACTIVE                | SSOP         | DB              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC00DBRG4   | ACTIVE                | SSOP         | DB              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC00DE4     | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC00DG4     | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC00DGVR    | ACTIVE                | TVSOP        | DGV             | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC00DGVRE4  | ACTIVE                | TVSOP        | DGV             | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC00DGVRG4  | ACTIVE                | TVSOP        | DGV             | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC00DR      | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC00DRE4    | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC00DRG4    | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC00N       | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN74AHC00NE4     | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN74AHC00NSR     | ACTIVE                | SO           | NS              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC00NSRE4   | ACTIVE                | SO           | NS              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC00NSRG4   | ACTIVE                | SO           | NS              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC00PW      | ACTIVE                | TSSOP        | PW              | 14   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC00PWE4    | ACTIVE                | TSSOP        | PW              | 14   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC00PWG4    | ACTIVE                | TSSOP        | PW              | 14   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC00PWLE    | OBSOLETE              | TSSOP        | PW              | 14   |             | TBD                     | Call TI          | Call TI                      |
| SN74AHC00PWR     | ACTIVE                | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC00PWRE4   | ACTIVE                | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74AHC00PWRG4   | ACTIVE                | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC00RGYR    | ACTIVE                | VQFN         | RGY             | 14   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| SN74AHC00RGYRG4  | ACTIVE                | VQFN         | RGY             | 14   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| SNJ54AHC00FK     | ACTIVE                | LCCC         | FK              | 20   | 1           | TBD                     | POST-PLATE       | N / A for Pkg Type           |
| SNJ54AHC00J      | ACTIVE                | CDIP         | J               | 14   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| SNJ54AHC00W      | ACTIVE                | CFP          | W               | 14   | 1           | TBD                     | A42              | N / A for Pkg Type           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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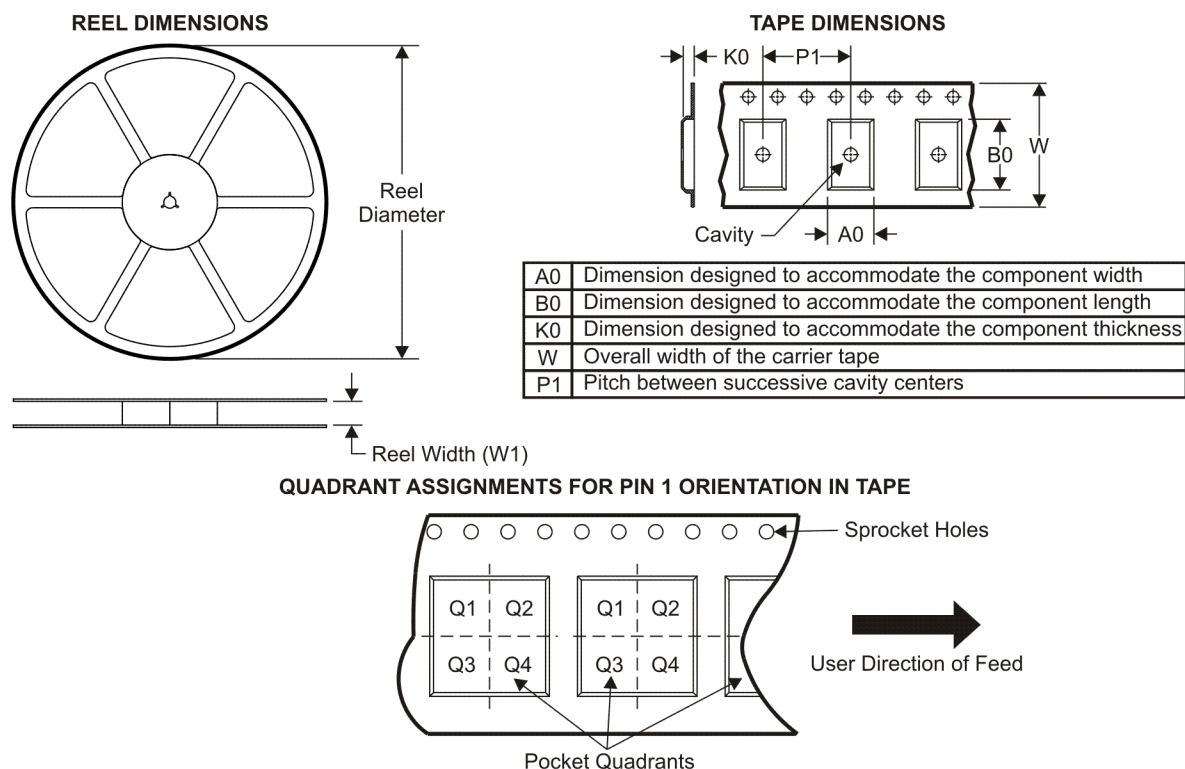
## OTHER QUALIFIED VERSIONS OF SN54AHC00, SN74AHC00 :

- Automotive: [SN74AHC00-Q1](#)
- Enhanced Product: [SN74AHC00-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications



**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHC00DBR  | SSOP         | DB              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 6.6     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74AHC00DGVR | TVSOP        | DGV             | 14   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74AHC00DR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74AHC00NSR  | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74AHC00PWR  | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 7.0     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74AHC00RGYR | VQFN         | RGY             | 14   | 3000 | 180.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHC00DBR  | SSOP         | DB              | 14   | 2000 | 346.0       | 346.0      | 33.0        |
| SN74AHC00DGVR | TVSOP        | DGV             | 14   | 2000 | 346.0       | 346.0      | 29.0        |
| SN74AHC00DR   | SOIC         | D               | 14   | 2500 | 346.0       | 346.0      | 33.0        |
| SN74AHC00NSR  | SO           | NS              | 14   | 2000 | 346.0       | 346.0      | 33.0        |
| SN74AHC00PWR  | TSSOP        | PW              | 14   | 2000 | 346.0       | 346.0      | 29.0        |
| SN74AHC00RGYR | VQFN         | RGY             | 14   | 3000 | 190.5       | 212.7      | 31.8        |

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - The terminals are gold plated.
  - Falls within JEDEC MS-004

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN

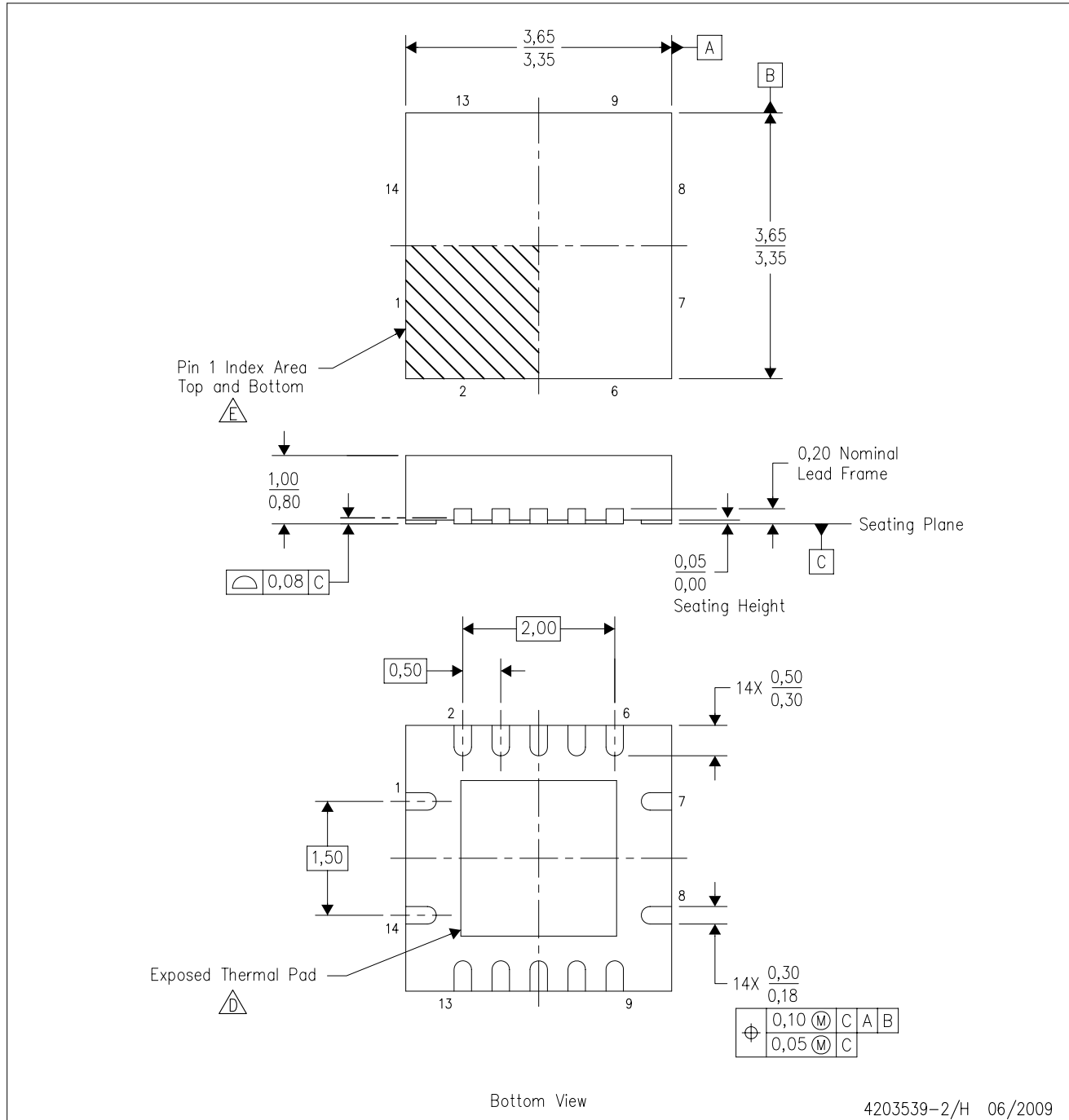


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/H 06/2009

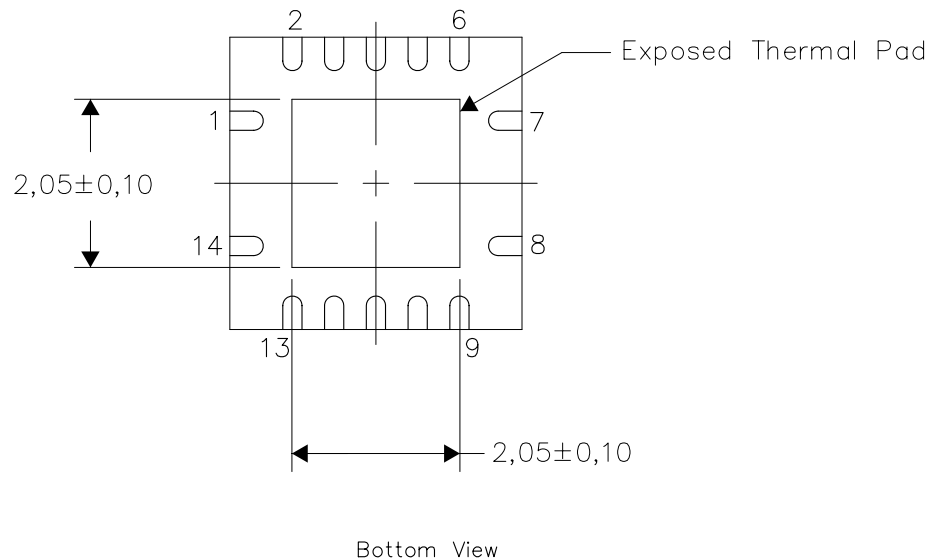
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - F. Package complies to JEDEC MO-241 variation BA.

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

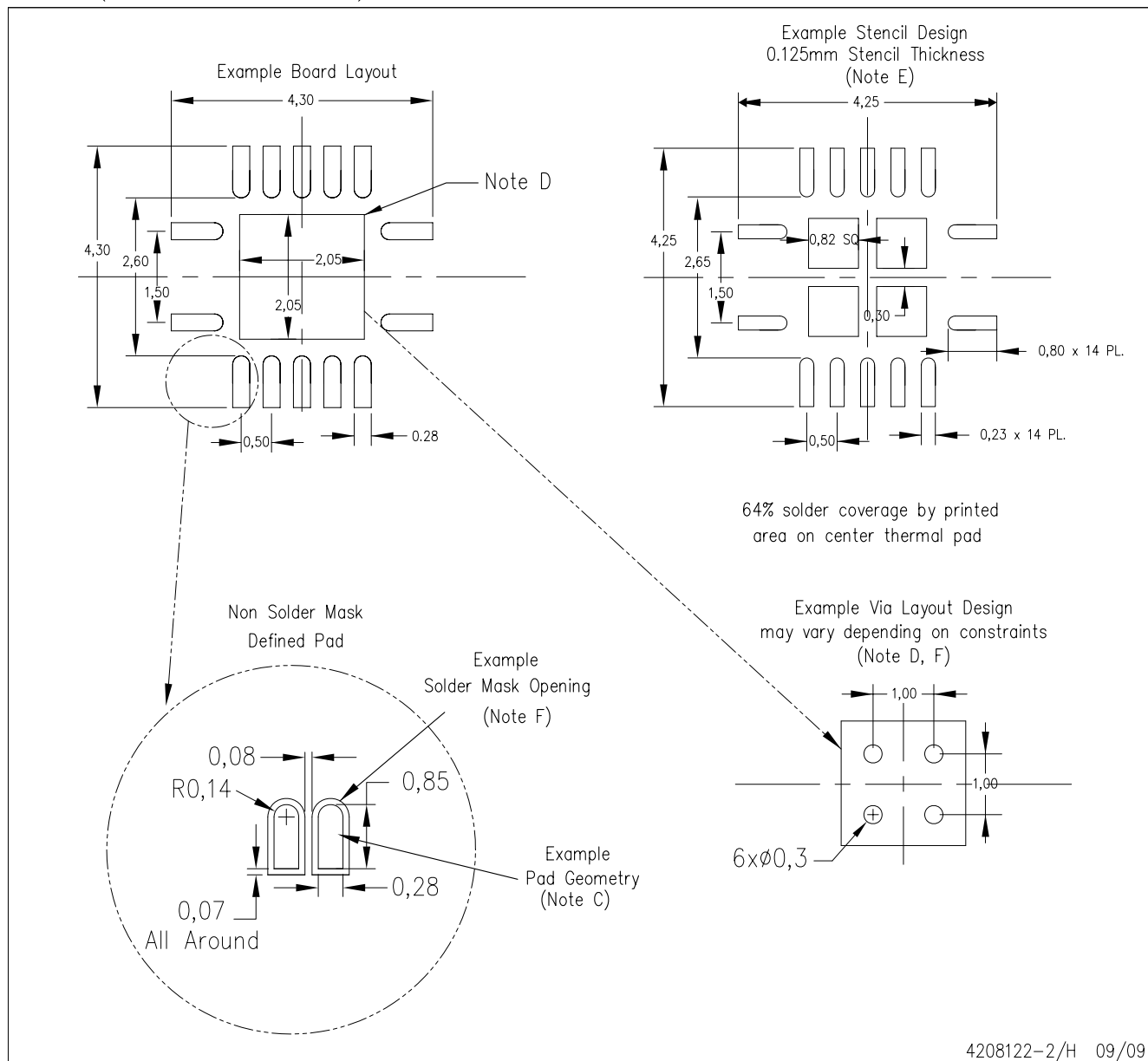
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTES: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

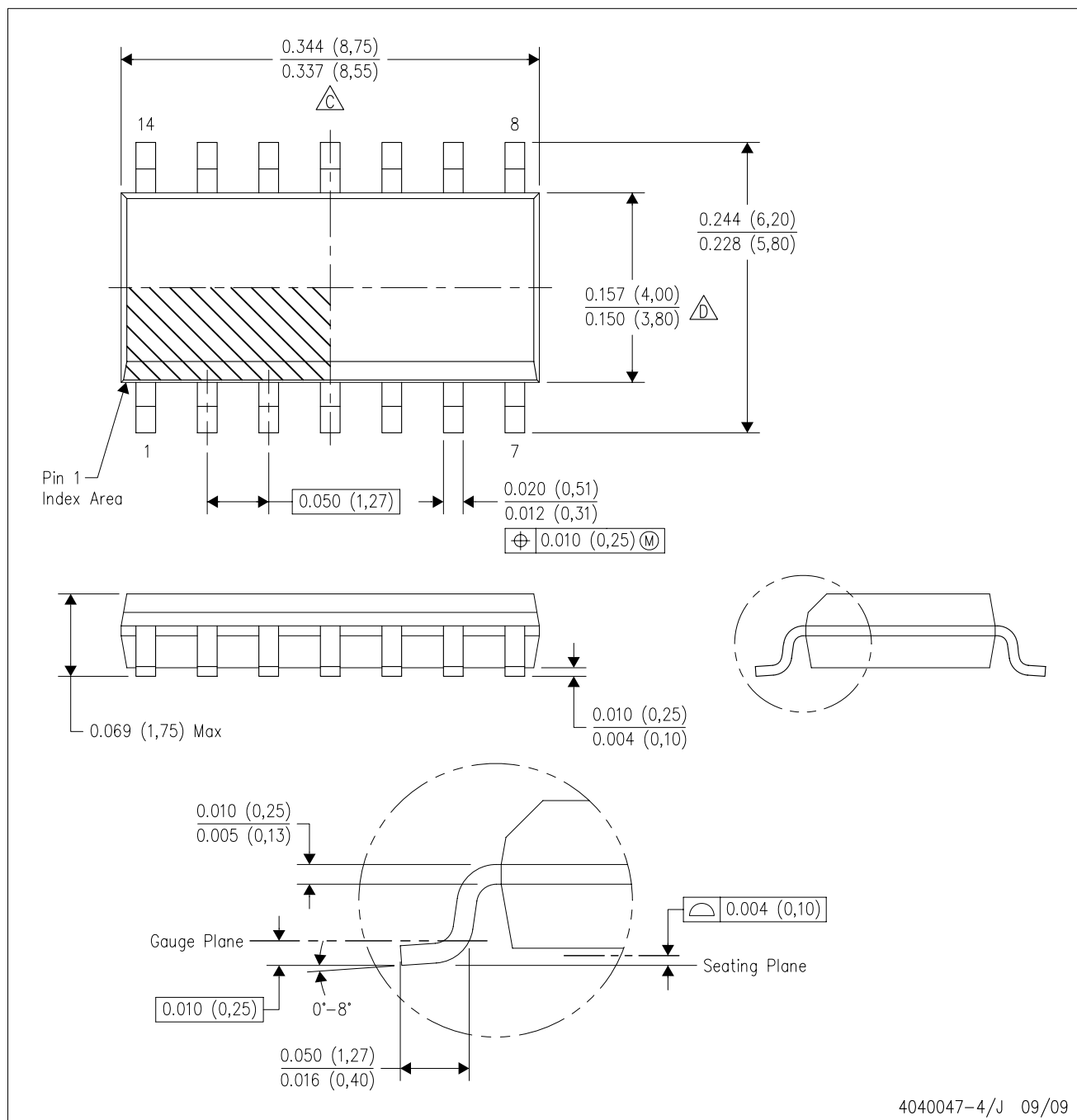
## RGY (S-PVQFN-N14)



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE

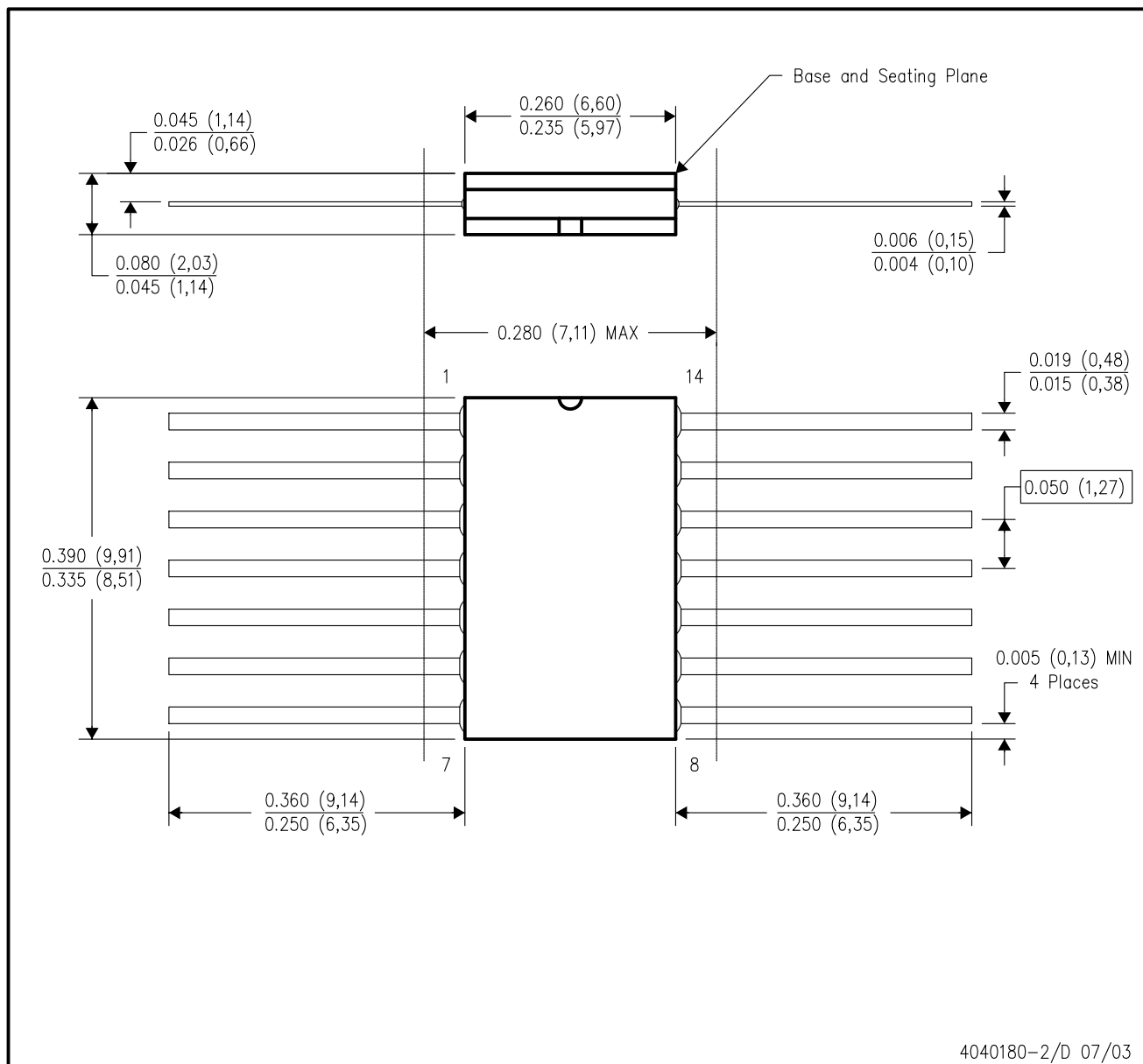


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AB.

W (R-GDFP-F14)

## CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

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| RF/IF and ZigBee® Solutions | <a href="http://www.ti.com/lprf">www.ti.com/lprf</a>               | Video and Imaging          | <a href="http://www.ti.com/video">www.ti.com/video</a>                                   |
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