

SN54LS55, SN74LS55 2-WIDE 4-INPUT AND-OR-INVERT GATES

SDLS181 – DECEMBER 1983 – REVISED MARCH 1988

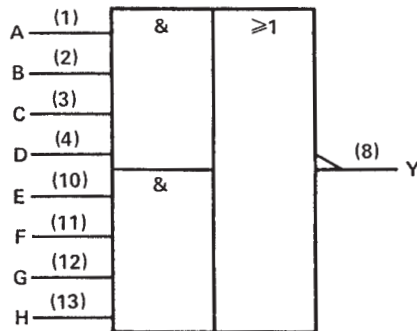
- Package Options Include "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain 2-wide 4-input AND-OR-INVERT gates. They perform the Boolean function $Y = \overline{ABCD + EFGH}$.

The SN54LS55 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS55 is characterized for operation from 0°C to 70°C .

logic symbol†

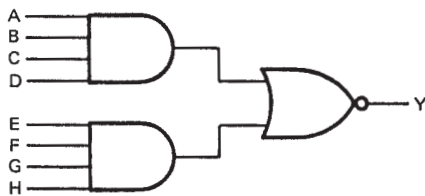


positive logic: $Y = \overline{ABCD + EFGH}$

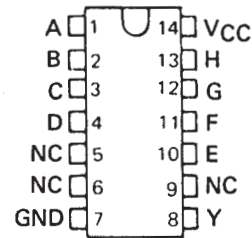
†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

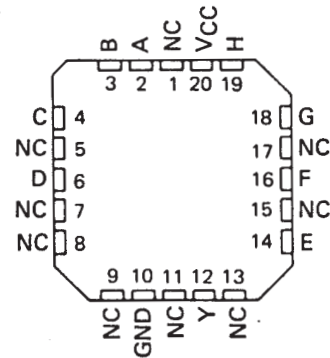
logic diagram



SN54LS55 . . . J OR W PACKAGE
SN74LS55 . . . D OR N PACKAGE
(TOP VIEW)

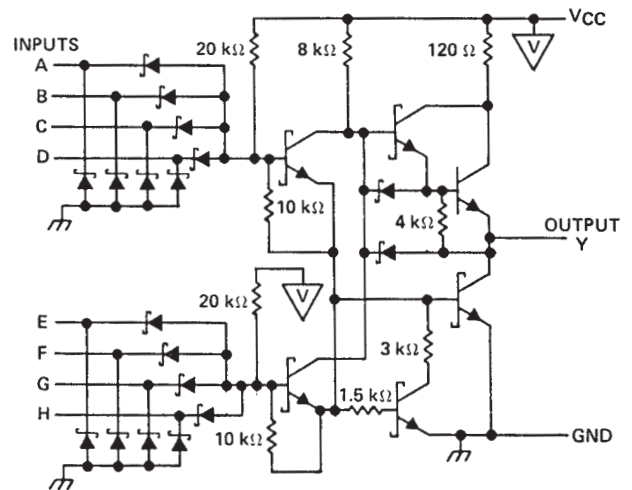


SN54LS55 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

schematic



Resistor values shown are nominal.

SN54LS55, SN74LS55

2-WIDE 4-INPUT AND-OR-INVERT GATES

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature: SN54LS55	–55°C to 125°C
SN74LS55	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS55			SN74LS55			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			–0.4			–0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS55			SN74LS55			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			–1.5			–1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$					0.35	0.5	
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			–0.4			–0.4	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$	–20		–100	–20		–100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		0.4	0.8		0.4	0.8	mA
I_{CCL}	$V_{CC} = \text{MAX}, \text{ See Note 2}$		0.7	1.3		0.7	1.3	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTE 2: All outputs of one AND gate at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		12	20	ns
t_{PHL}					12.5	20	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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