- **Members of the Texas Instruments *Widebus*™ Family**

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**

- **High-Impedance State During Power Up and Power Down**

- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**

- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**

- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**

- **Flow-Through Architecture Optimizes PCB Layout**

- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**

- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABT16823 . . . WD PACKAGE
SN74ABT16823 . . . DGG OR DL PACKAGE
(TOP VIEW)

1CLR	1	56	1CLK
1OE	2	55	1CLKEN
1Q1	3	54	1D1
GND	4	53	GND
1Q2	5	52	1D2
1Q3	6	51	1D3
V_{CC}	7	50	V_{CC}
1Q4	8	49	1D4
1Q5	9	48	1D5
1Q6	10	47	1D6
GND	11	46	GND
1Q7	12	45	1D7
1Q8	13	44	1D8
1Q9	14	43	1D9
2Q1	15	42	2D1
2Q2	16	41	2D2
2Q3	17	40	2D3
GND	18	39	GND
2Q4	19	38	2D4
2Q5	20	37	2D5
2Q6	21	36	2D6
V_{CC}	22	35	V_{CC}
2Q7	23	34	2D7
2Q8	24	33	2D8
GND	25	32	GND
2Q9	26	31	2D9
2OE	27	30	2CLKEN
2CLR	28	29	2CLK

description

These 18-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The 'ABT16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable (CLKEN) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high disables the clock buffer, latching the outputs. Taking the clear (CLR) input low causes the Q outputs to go low independently of the clock.

A buffered output-enable (OE) input can be used to place the nine outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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description (continued)

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN54ABT16823 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16823 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 9-bit flip-flop)

$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	L	L	X	Q_0
L	H	H	X	X	Q_0
H	X	X	X	X	Z

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logic symbol†

Signal	Pin	Label		Out Label	Pin	Signal
1$\overline{OE}$	2	EN1				
1$\overline{CLR}$	1	R2				
1$\overline{CLKEN}$	55	G3				
1CLK	56	3C4				
2$\overline{OE}$	27	EN5				
2$\overline{CLR}$	28	R6				
2$\overline{CLKEN}$	30	G7				
2CLK	29	7C8				
1D1	54	4D	1, 2 ▽		3	1Q1
1D2	52				5	1Q2
1D3	51				6	1Q3
1D4	49				8	1Q4
1D5	48				9	1Q5
1D6	47				10	1Q6
1D7	45				12	1Q7
1D8	44				13	1Q8
1D9	43				14	1Q9
2D1	42	8D	5, 6 ▽		15	2Q1
2D2	41				16	2Q2
2D3	40				17	2Q3
2D4	38				19	2Q4
2D5	37				20	2Q5
2D6	36				21	2Q6
2D7	34				23	2Q7
2D8	33				24	2Q8
2D9	31				26	2Q9
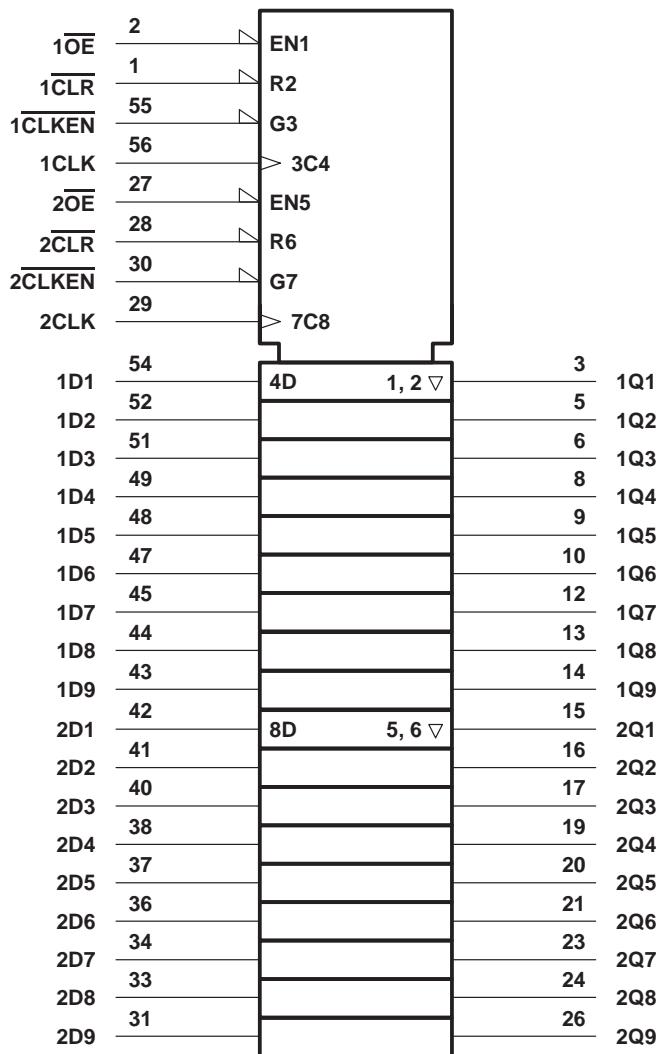
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

To Eight Other Channels

To Eight Other Channels

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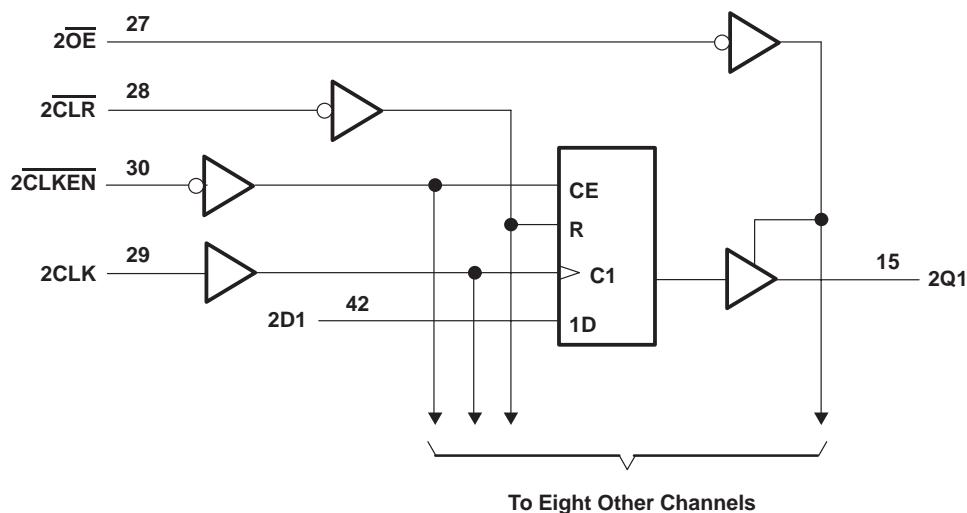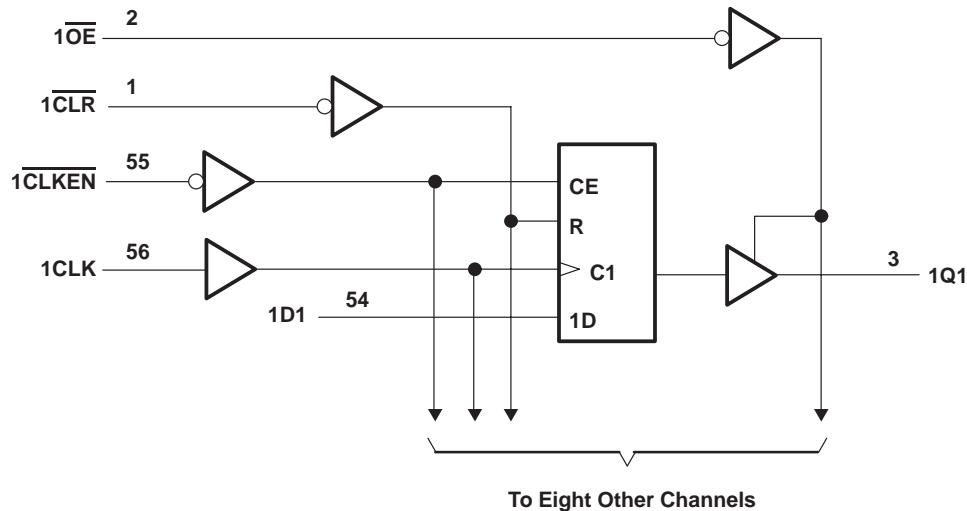
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O .... –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16823 .... 96 mA
 SN74ABT16823 .... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) .... –18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package .... 81°C/W
 DL package .... 74°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
 functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
 implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

			SN54ABT16823		SN74ABT16823		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		µs/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A = 25°C$ MIN	TYP†	MAX	SN54ABT16823 MIN	MAX	SN74ABT16823 MIN	MAX	UNIT
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			−1.2		−1.2		−1.2	V
V_{OH}		$V_{CC} = 4.5$ V,	$I_{OH} = -3$ mA	2.5			2.5		2.5		V
		$V_{CC} = 5$ V,	$I_{OH} = -3$ mA	3			3		3		
		$V_{CC} = 4.5$ V	$I_{OH} = -24$ mA	2			2				
			$I_{OH} = -32$ mA	2*					2		
V_{OL}		$V_{CC} = 4.5$ V	$I_{OL} = 48$ mA			0.55		0.55			V
			$I_{OL} = 64$ mA			0.55*				0.55	
V_{hys}					100						mV
I_I		$V_{CC} = 0$ to 5.5 V, $V_I = V_{CC}$ or GND				±1		±1		±1	µA
I_{OZPU}		$V_{CC} = 0$ to 2.1 V, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$				±50		±50		±50	µA
I_{OZPD}		$V_{CC} = 2.1$ V to 0, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$				±50		±50		±50	µA
I_{OZH}		$V_{CC} = 2.1$ V to 5.5 V, $V_O = 2.7$ V, $\overline{OE} \geq 2$ V				10**		50		10	µA
I_{OZL}		$V_{CC} = 2.1$ V to 5.5 V, $V_O = 0.5$ V, $\overline{OE} \geq 2$ V				−10**		−50		−10	µA
I_{off}		$V_{CC} = 0$, V_I or $V_O \leq 4.5$ V				±100				±100	µA
I_{CEX}	Outputs high	$V_{CC} = 5.5$ V, $V_O = 5.5$ V				50		50		50	µA
I_O‡		$V_{CC} = 5.5$ V, $V_O = 2.5$ V		−50	−100	−200	−50	−200	−50	−200	mA
I_{CC}	Outputs high	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND				0.5		0.5		0.5	mA
	Outputs low					80		80		80	
	Outputs disabled					0.5		0.5		0.5	
ΔI_{CC}§		$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i		$V_I = 2.5$ V or 0.5 V			3.5						pF
C_o		$V_O = 2.5$ V or 0.5 V			7.5						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
** These limits apply only to the SN74ABT16823.
† All typical values are at $V_{CC} = 5$ V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			$V_{CC} = 5$ V, $T_A = 25°C$		SN54ABT16823		SN74ABT16823		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	MHz
t_w	Pulse duration	$\overline{CLR}$ low	3.3		3.3		3.3		ns
		CLK high or low	3.3		3.3		3.3		
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	1.6		2		1.6		ns
		Data	1.7		1.7		1.7		
		$\overline{CLKEN}$ low	2.8		2.8		2.8		
t_h	Hold time after CLK↑	Data	1.2		1.2		1.2		ns
		$\overline{CLKEN}$ low	0.6		0.6		0.6		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT16823					UNIT
			$V_{CC} = 5$ V, $T_A = 25°C$			MIN	MAX	
			MIN	TYP	MAX			
f_{max}			150			150		MHz
t_{PLH}	CLK	Q	1.6	3.9	5.5	1.6	7.7	ns
t_{PHL}			2.1	3.9	5.4	2.1	6.4	
t_{PHL}	$\overline{CLR}$	Q	1.9	4.1	5.3	1.9	6.3	ns
t_{PZH}	$\overline{OE}$	Q	1	3.1	4.2	1	5.1	ns
t_{PZL}			1.5	3.5	4.6	1.5	5.7	
t_{PHZ}	$\overline{OE}$	Q	2.2	4.3	6	2.2	6.8	ns
t_{PLZ}			1.6	4.3	6.4	1.6	9.9	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT16823					UNIT
			$V_{CC} = 5$ V, $T_A = 25°C$			MIN	MAX	
			MIN	TYP	MAX			
f_{max}			150			150		MHz
t_{PLH}	CLK	Q	1.6	3.9	5.5	1.6	6.8	ns
t_{PHL}			2.1	3.9	5.4	2.1	6	
t_{PHL}	$\overline{CLR}$	Q	1.9	4.1	5.3	1.9	6.1	ns
t_{PZH}	$\overline{OE}$	Q	1	3.1	4.2	1	4.9	ns
t_{PZL}			1.5	3.5	4.6	1.5	5.5	
t_{PHZ}	$\overline{OE}$	Q	2.2	4.3	5.6	2.2	6.1	ns
t_{PLZ}			1.6	4.3	6.4	1.6	8.7	

PARAMETER MEASUREMENT INFORMATION
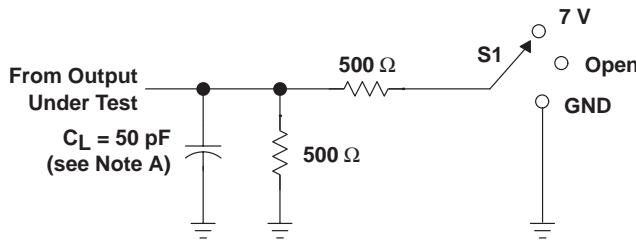
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT
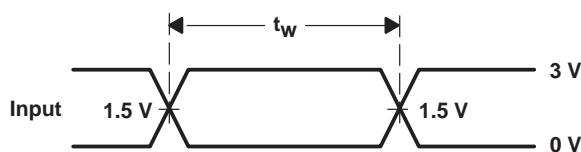
VOLTAGE WAVEFORMS
PULSE DURATION
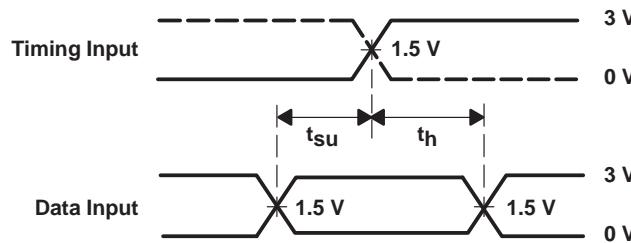
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
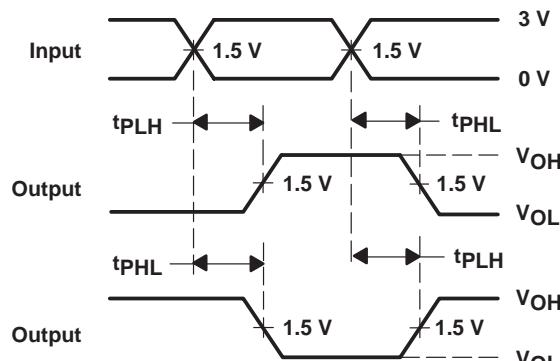
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS
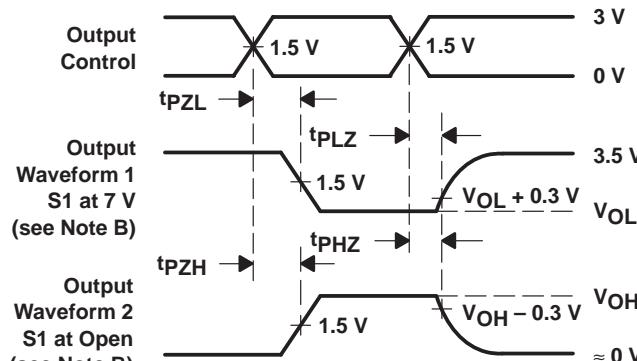
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
        B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
           Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
        C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
        D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-9584201QXA	ACTIVE	CFP	WD	56	1	TBD	Call TI	N / A for Pkg Type
74ABT16823DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16823DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16823DGVR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16823DGVRE4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16823DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16823DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16823DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16823DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ABT16823WD	ACTIVE	CFP	WD	56	1	TBD	Call TI	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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WD (R-GDFP-F**)   **CERAMIC DUAL FLATPACK**

48 LEADS SHOWN
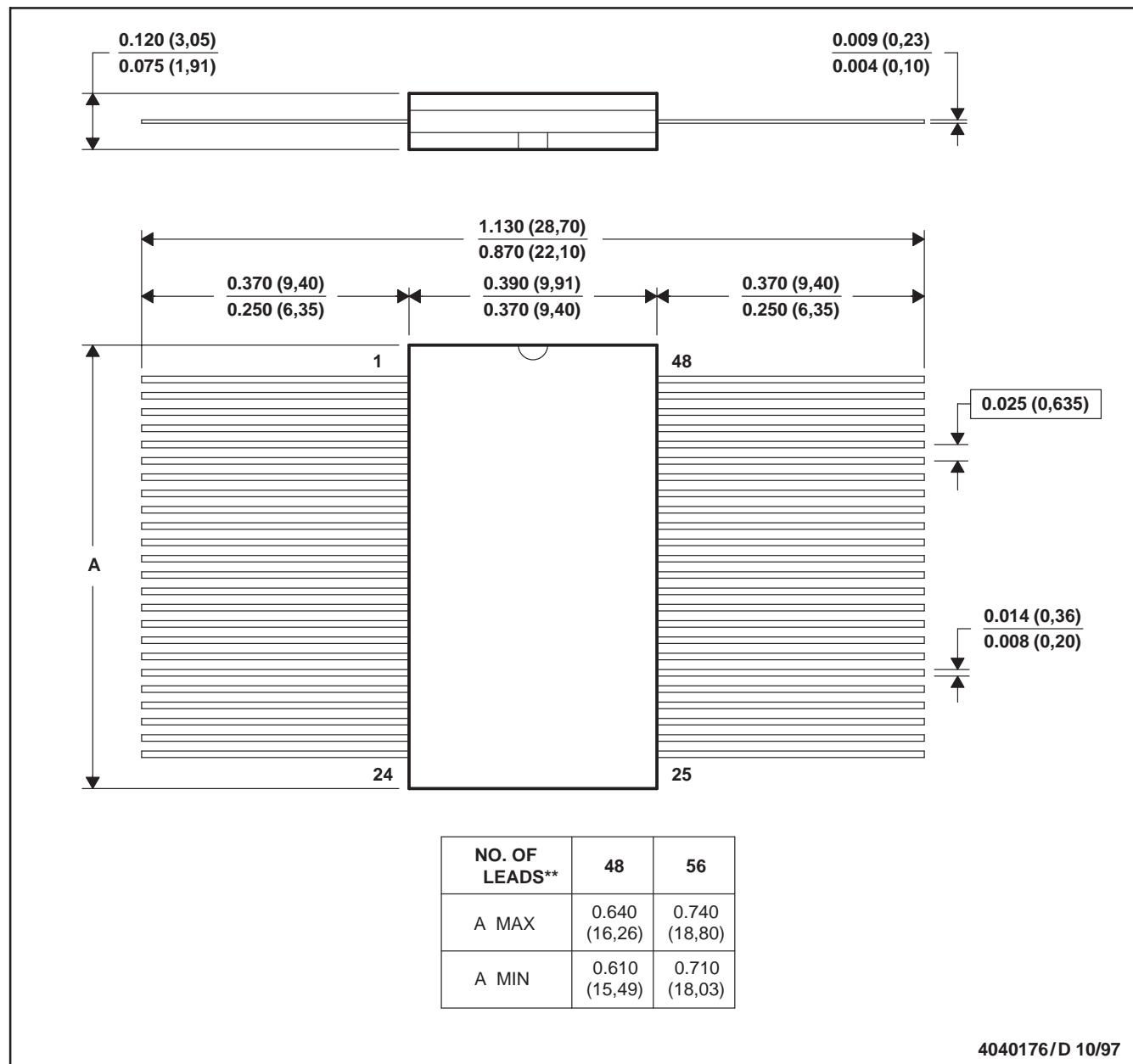
NO. OF LEADS**	48	56
A MAX	0.640 (16,26)	0.740 (18,80)
A MIN	0.610 (15,49)	0.710 (18,03)

4040176 / D 10/97

NOTES: A. All linear dimensions are in inches (millimeters).
             B. This drawing is subject to change without notice.
             C. This package can be hermetically sealed with a ceramic lid using glass frit.
             D. Index point is provided on cap for terminal identification only
             E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
                                           GDFP1-F56 and JEDEC MO-146AB

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN
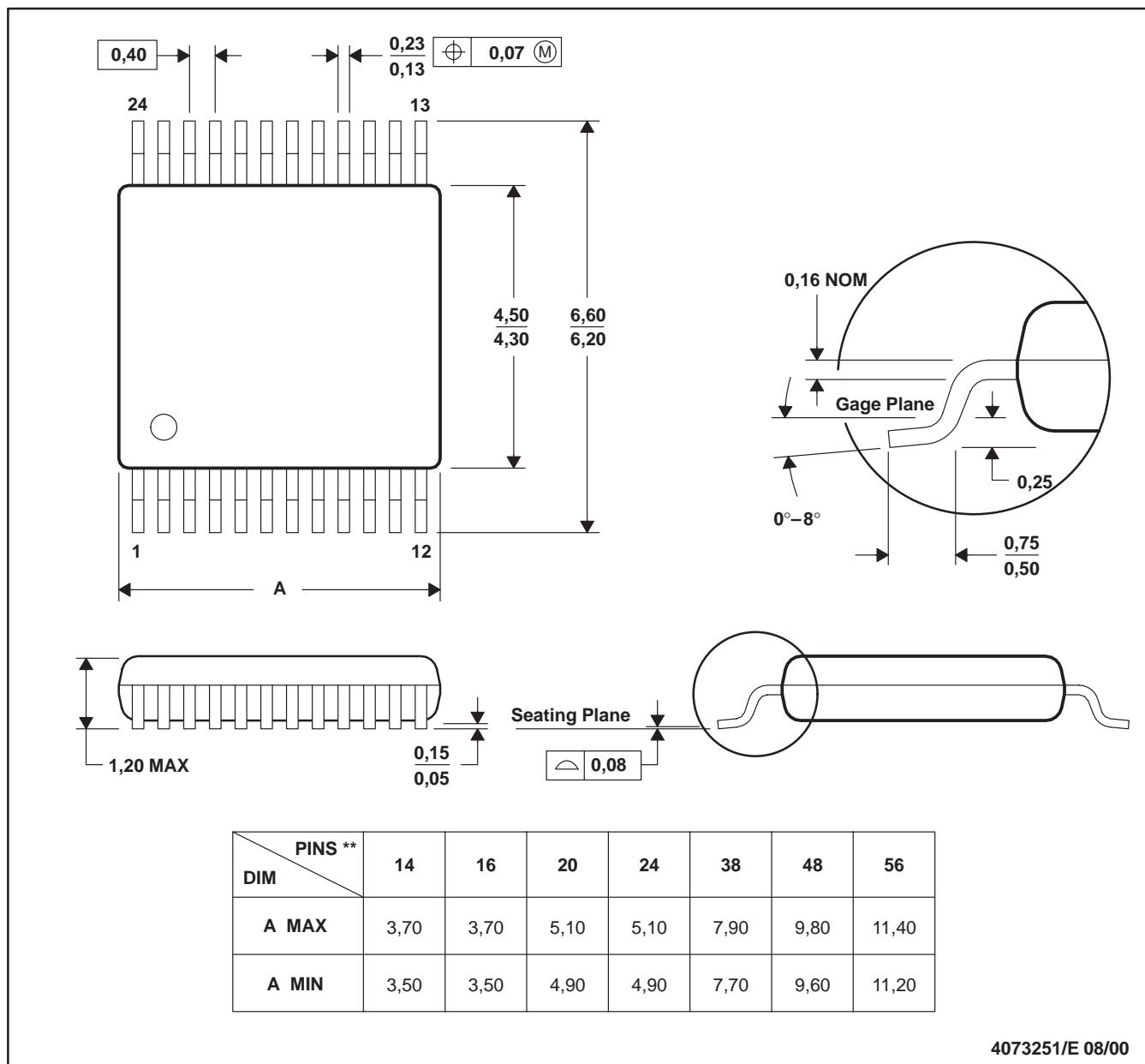
PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
          D. Falls within JEDEC: 24/48 Pins – MO-153
                                  14/16/20/56 Pins – MO-194

DL (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**
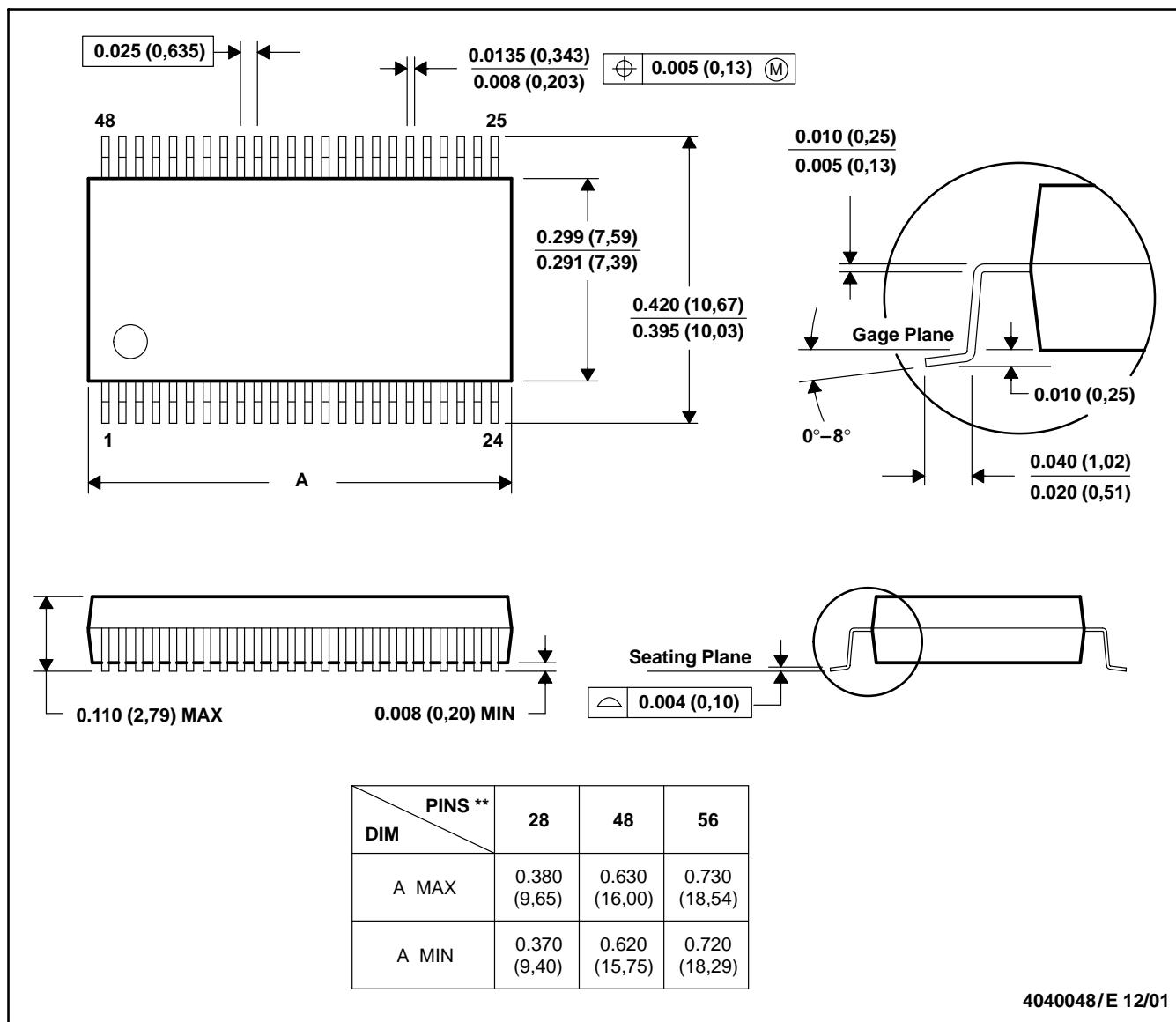
48 PINS SHOWN

0.025 (0,635)

0.0135 (0,343)
0.008 (0,203)

0.005 (0,13) (M)

48   25

0.010 (0,25)
0.005 (0,13)

0.299 (7,59)
0.291 (7,39)

0.420 (10,67)
0.395 (10,03)

Gage Plane

0.010 (0,25)

1   24

0°–8°

0.040 (1,02)
0.020 (0,51)

A

0.110 (2,79) MAX   0.008 (0,20) MIN

Seating Plane

0.004 (0,10)

PINS ** DIM	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048 / E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118
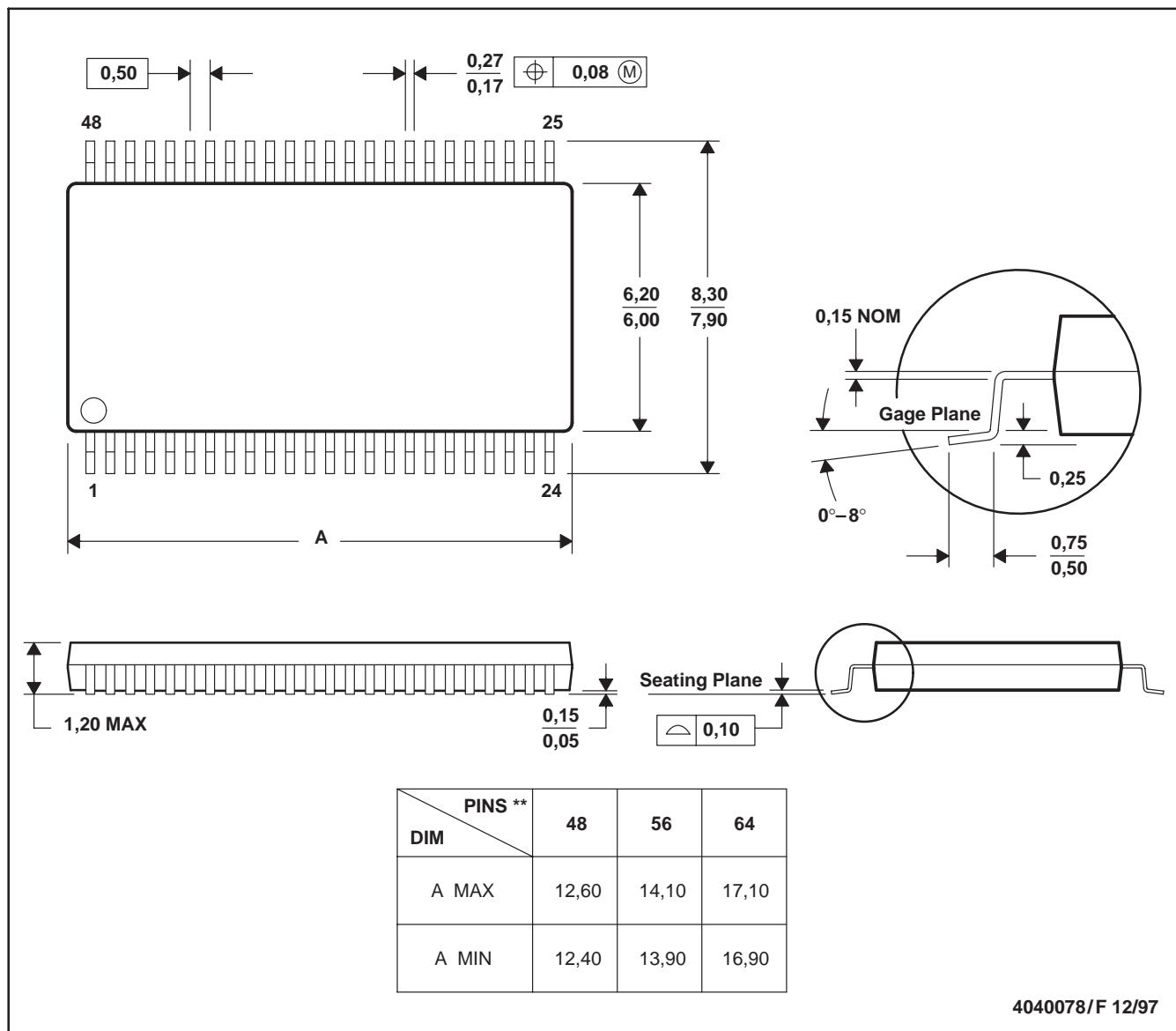
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MECHANICAL DATA

DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

PINS **	48	56	64
DIM			
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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