Features

Fast Read Access Time - 70ns

Low Power CMOS Operation

- 100µa max. Standby
- 30mA max. Active at 5 MHz

JEDEC Standard Package

- 32 lead LCC, Windowed

5V ±10% Supply

High Reliability CMOS Technology

- 2000V ESD Protection
- 200mA Latchup Immunity

Rapid™ Programming Algorithm - 100µs/byte (typical)

CMOS and TTL Compatible Inputs and Outputs

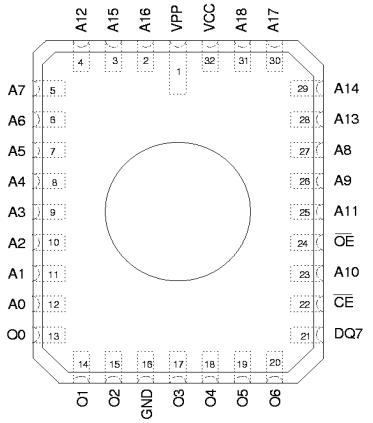
Integrated Product Identification Code

Military and Industrial Temperature Ranges

4 Megabit (512Kx8) UV Erasable CMOS EEPROM

The EDI68512C chip is a low-power, high performance, 4,194,304-bit ultraviolet erasable programmable read only memory (EPROM) organized as 512Kx8 bits. The EDI68612C requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 70ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems. Atmel's scaled CMOS technology provides low active power consumption and fast programming. Power consumption is typically 8mA in active mode and less than 10µa in standby mode.

Pin Configurations



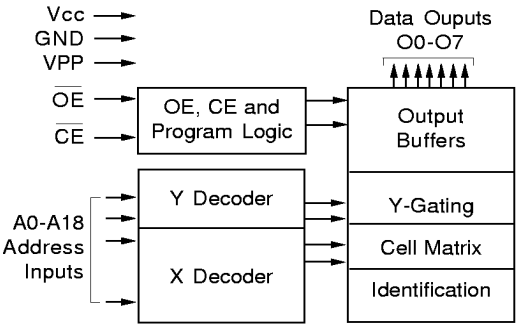
Pin Names

AØ-A18	Addresses
OØ-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable

Switching Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1uF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the Vcc and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7uF bulk electrolytic capacitor should be utilized, again connected between the Vcc and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Operating Modes

Mode/Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	Ai	X(1)	D_{OUT}
Output Disable	X	V_{IH}	X	X	High Z
Standby	V_{IH}	X	X	X	High Z
Rapid Program (2)	V_{IL}	V_{IH}	Ai	V_{PP}	D_{IN}
PGM Verify	X	V_{IL}	Ai	V_{PP}	D_{OUT}
PGM Inhibit	V_{IH}	V_{IH}	X	V_{PP}	High Z
Product Identification(4)	V_{IL}	V_{IL}	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1-A18 = V_{IL}	X	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming Characteristics.
3. V_H=12.0±0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

Absolute Maximum Ratings*

Temperature Under Bias	-55 ℃ to +125 ℃
Storage Temperature	-65 ℃ to +150 ℃
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)

*Note: 1. Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Conditions for Read Operation

		-70	-90	-12	-15
Operating	**Military**	- -	-55 ℃ to +125 ℃	-55 ℃ to +125 ℃	-55 ℃ to +125 ℃
Temperature (Case)	**Industrial**	-40 ℃ to +85 ℃	-40 ℃ to +85 ℃	-40 ℃ to +85 ℃	-40 ℃ to +85 ℃
Vcc Power Supply		5V±10%	5V±10%	5V±10%	5V±10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1}[2]	V_{PP}[1] Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC}[1] Standby Current	I_{SB1} (CMOS), CE = V_{CC}±0.3V		100	µA
		I_{SB2} (TTL), CE = 2.0 to V_{CC}±0.5V		1	mA
I_{CC}	V_{CC} Active Current	f= 5MHz, I_{OUT} = 0mA, CE = V_{IN}		30	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400µA	2.4		V

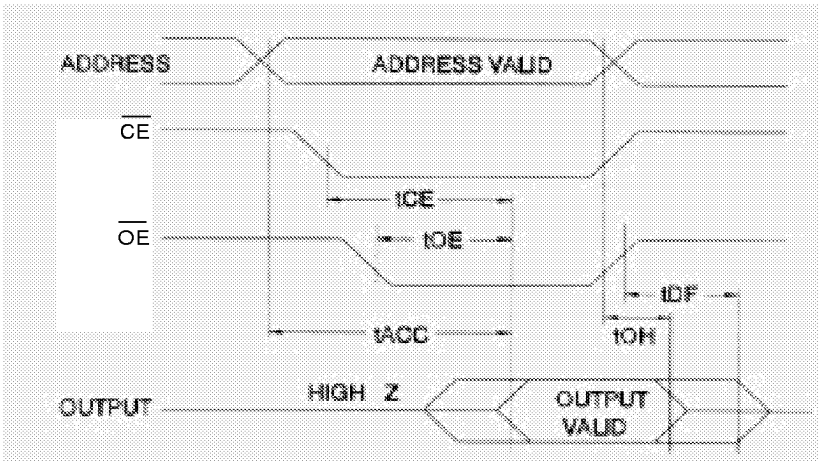
Notes: 1. Vcc must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.
2. Vpp may be connected directly to Vcc, except during programming. The supply current would then be the sum of Icc and Ipp.

AC Characteristics for Read Operation

			-70		-90		-12		-15		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC}[3]	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		70		90		120		150	ns
t_{CE}[2]	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		70		90		120		150	ns
t_{OE}[2][3]	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		30		35		35		40	ns
t_{DF}[4][5]	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occured first			20		20		30		30	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occured first			0		0		0		0	ns

Note: 2, 3, 4, 5: see AC Waveforms for Read Operation.

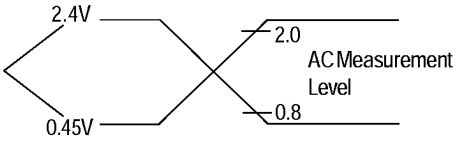
AC Waveforms for Read Operation[1]



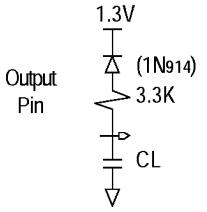
Notes: 1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4 V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurment Levels

AC Driving Levels



Output Test Load



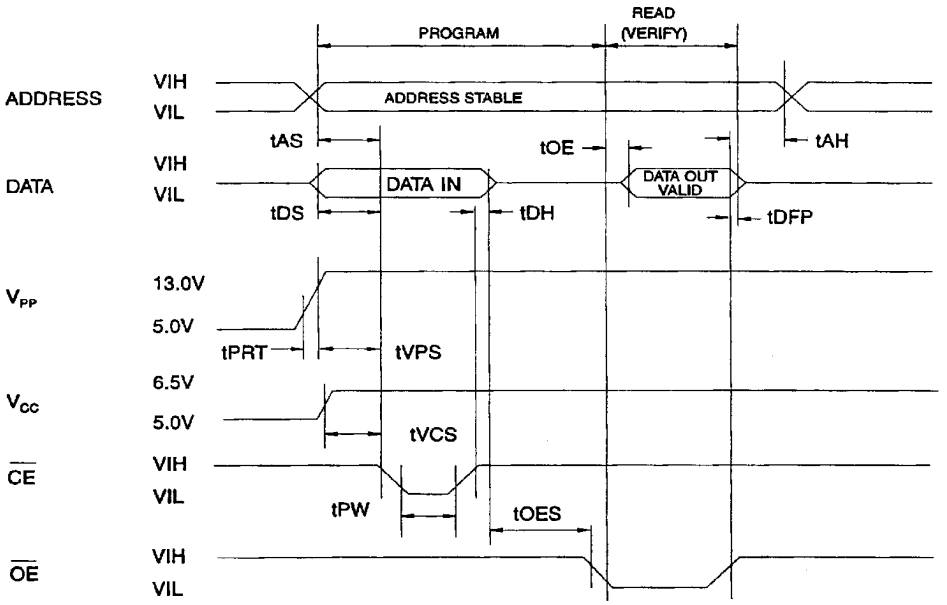
Pin Capacitance

(f=1 MHz, T=25 ℃)[1]

	Typ	Max	Unit	Conditions
C_{IN}	4	8	pF	V_{IN} =0V
C_{OUT}	8	12	pF	V_{OUT} =0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and not 100% tested.

Programming Waveforms[1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} 2.0V for V_{IH}.
2. t_{DF} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the EDI68512C a 0.1 uF capacitor is required accross Vpp ground to supress spurious voltage transients.

DC Programming Characteristics

T_A=25±5 ℃, Vcc=6.5±0.25V, Vpp=13.0±0.25V

			Limits		
Symbol	**Parameter**	**Test Conditions**	**Min**	**Max**	**Units**
I_{LI}	Input Load Current	$V_{IN}=V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	Vcc+0.7	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	0.4	V
V_{OH}	Output High Voltage	I_{OH}= -400µA	2.4		V
V_{CC2}	Vcc Supply Current (Program and Verify)			40	mA
I_{PP2}	Vpp Supply Current	$\overline{CE}$= V_{IL}		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

T_A=25±5 ℃, Vcc=6.5±0.25V, Vpp=13.0±0.25V

Symbol	Parameter	Test Conditions[1]	Limits Min	Max	Units
t_{AS}	Address Setup Time	Input Rise and Fall Times (10% to 90%) 20ns Input Pulse Levels 0.45 to 2.4V Input Timing Reference Level 0.8V to 2.0V Output Timing Reference Level 0.8V to 2.0V	2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay[2]		0	130	µs
t_{VPS}	Vpp Setup Time		2		µs
t_{VCS}	Vcc Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width[3]		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$[2]			150	µs
t_{PRT}	Vpp Pulse Rise Time During Programming		50		µs

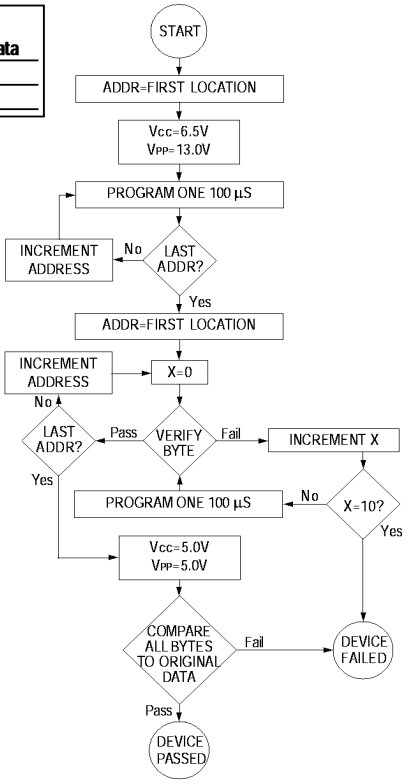
Notes: 1. Vcc must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven - see timing diagram.
3. Program Pulse width tolerance is 100 µsec ±5%.

Product Identification Code

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	0	1	1	1E

Rapid Programming Algorith

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. Vcc is raised to 6.5V and Vpp is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/ reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. Vpp is then lowered to 5.0V and Vcc to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

Industrial Temperature -40°C +85°C

Part No.	Speed (ns)	Package No.
EDI68512C70LI	70	426
EDI68512C90LI	90	426
EDI68512C120LI	120	426
EDI68512C150LI	150	426

MilitaryTemperature -55°C +125°C

Part No.	Speed (ns)	Package No.
EDI68512C90LM	90	426
EDI68512C120LM	120	426
EDI68512C150LM	150	426

Package Description

Package No. 426

32 Pad Windowed
Leadless Chip Carrier