

PowerMOS transistor

Logic level FET

BUK555-100A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

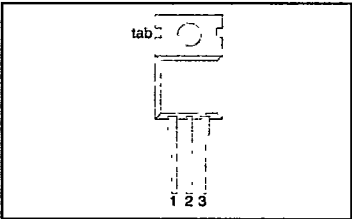
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK555	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	25	22	A
P_{tot}	Total power dissipation	125	125	W
T_j	Junction temperature	175	175	°C
$R_{DS,ON}$	Drain-source on-state resistance; $V_{GS} = 5\text{ V}$	0.085	0.11	Ω

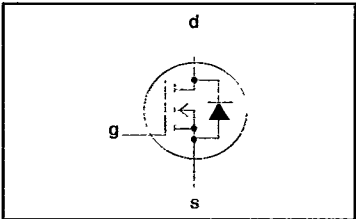
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50\text{ }\mu\text{s}$	-	20		V
I_D	Drain current (DC)	$T_{rb} = 25\text{ }^\circ\text{C}$	-	-100A	-100B	A
I_D	Drain current (DC)	$T_{rb} = 100\text{ }^\circ\text{C}$	-	25	22	A
I_{DM}	Drain current (pulse peak value)	$T_{rb} = 25\text{ }^\circ\text{C}$	-	18	15	A
				100	88	A
P_{tot}	Total power dissipation	$T_{rb} = 25\text{ }^\circ\text{C}$	-	125		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th,mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th,ja}$	Thermal resistance junction to ambient		-	60	-	K/W

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STATIC CHARACTERISTICS $T_{mb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}$	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1\text{ mA}$	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 100\text{ V}; V_{GS} = 0\text{ V}; T_J = 25\text{ }^{\circ}\text{C}$	-	1	10	μA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 100\text{ V}; V_{GS} = 0\text{ V}; T_J = 125\text{ }^{\circ}\text{C}$	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 10\text{ V}; V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 13\text{ A}$	-	0.075	0.085	Ω
		BUK555-100A	-	0.09	0.11	Ω
		BUK555-100B	-			

DYNAMIC CHARACTERISTICS $T_{mb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 25\text{ V}; I_D = 13\text{ A}$	10	13.5	-	S
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	1450	1750	pF
C_{oss}	Output capacitance		-	280	350	pF
C_{rss}	Feedback capacitance		-	100	150	pF
t_{don}	Turn-on delay time	$V_{DD} = 30\text{ V}; I_D = 3\text{ A}; V_{GS} = 5\text{ V}; R_{GS} = 50\text{ }\Omega;$	-	25	40	ns
t_r	Turn-on rise time	$R_{gen} = 50\text{ }\Omega$	-	65	85	ns
t_{doff}	Turn-off delay time		-	135	180	ns
t_f	Turn-off fall time		-	80	110	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS $T_{mb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{OR}	Continuous reverse drain current	-	-	-	25	A
I_{ORM}	Pulsed reverse drain current	-	-	-	100	A
V_{SD}	Diode forward voltage	$I_F = 25\text{ A}; V_{GS} = 0\text{ V}$	-	1.3	1.7	V
t_{rr}	Reverse recovery time	$I_F = 25\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_R = 30\text{ V}$	-	90	-	ns
Q_{rr}	Reverse recovery charge		-	0.8	-	μC

AVALANCHE LIMITING VALUE $T_{mb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 25\text{ A}; V_{PD} \leq 50\text{ V}; V_{GS} = 5\text{ V}; R_{GS} = 50\text{ }\Omega$	-	-	140	mJ

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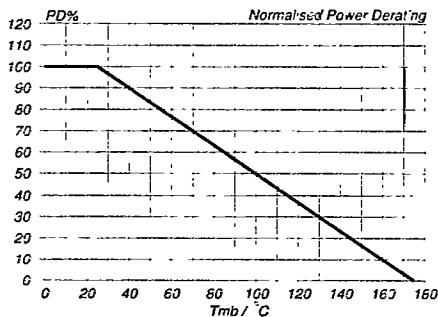


Fig. 1. Normalised power dissipation.
 $PD\% = 100 \cdot P_D / P_{D 25^\circ\text{C}} = f(T_{mb})$

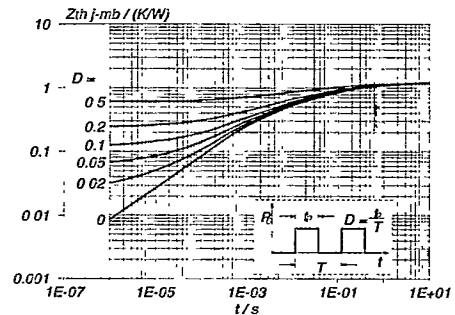


Fig. 4. Transient thermal impedance.
 $Z_{th j-mb} = f(t)$; parameter $D = t_p / T$

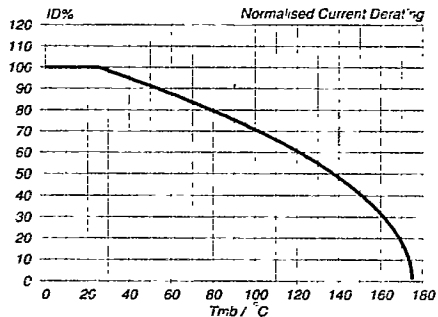


Fig. 2. Normalised continuous drain current.
 $ID\% = 100 \cdot I_D / I_{D 25^\circ\text{C}} = f(T_{mb})$; conditions: $V_{GS} \geq 5 \text{ V}$

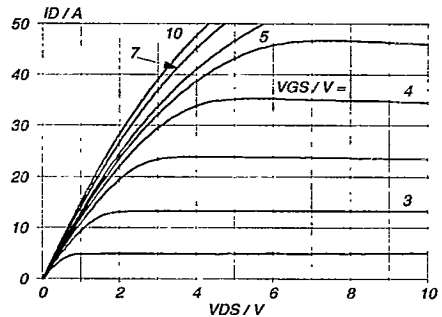


Fig. 5. Typical output characteristics, $T_j = 25^\circ\text{C}$.
 $I_D = f(V_{DS})$; parameter V_{GS}

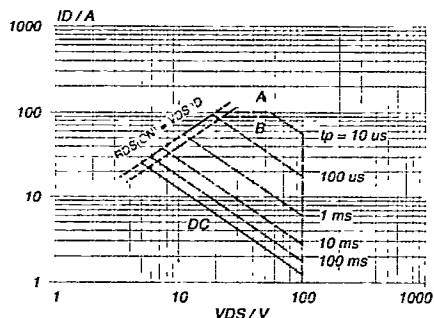


Fig. 3. Safe operating area. $T_{mb} = 25^\circ\text{C}$
 $I_D \& I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

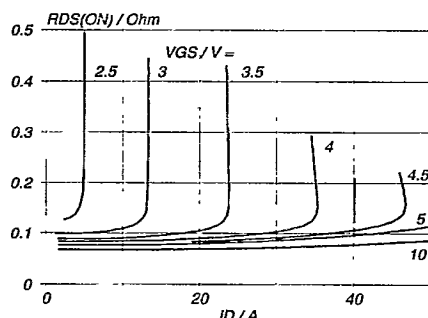
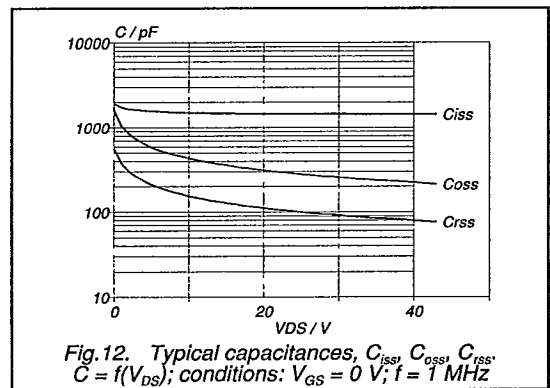
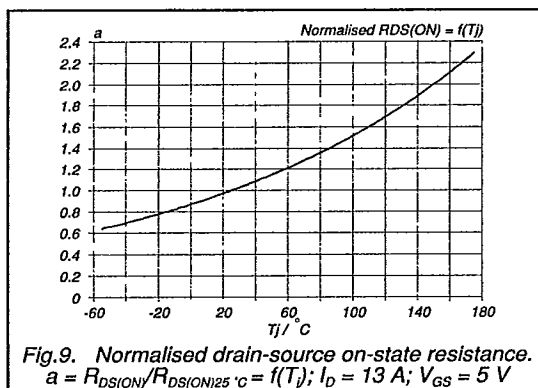
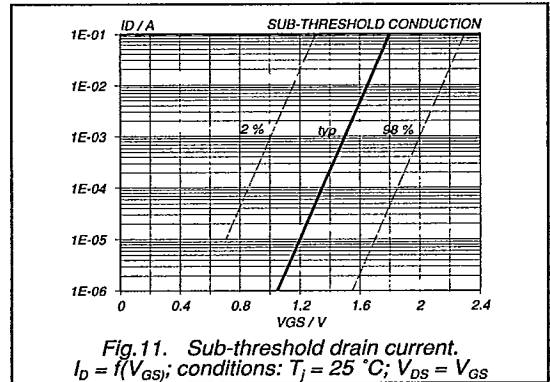
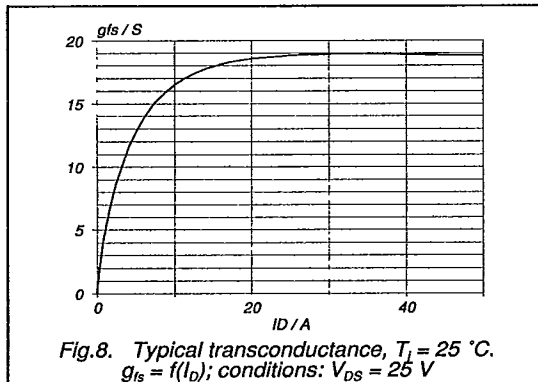
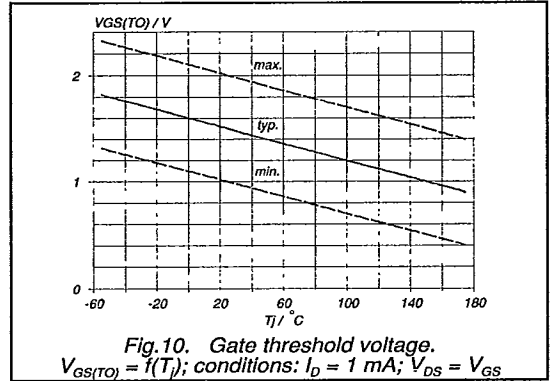
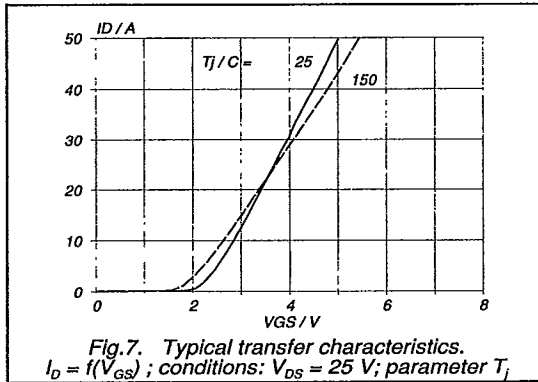


Fig. 6. Typical on-state resistance, $T_j = 25^\circ\text{C}$.
 $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

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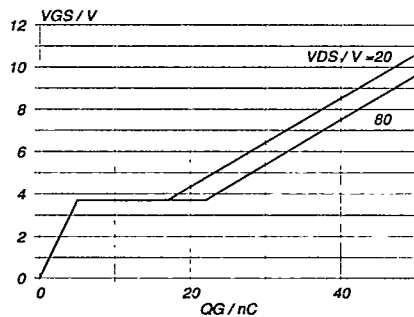


Fig. 13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; conditions: $I_D = 25\text{ A}$; parameter V_{DS}

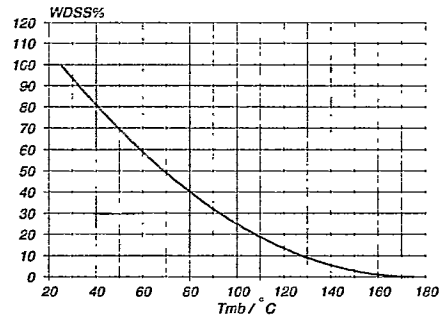


Fig. 15. Normalised avalanche energy rating.
 $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 25\text{ A}$

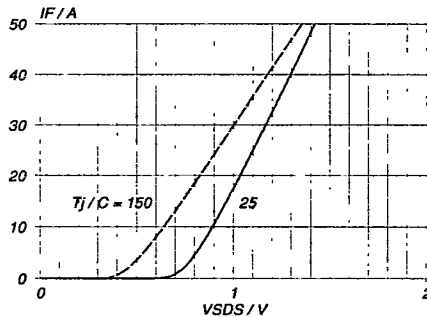


Fig. 14. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0\text{ V}$; parameter T_j

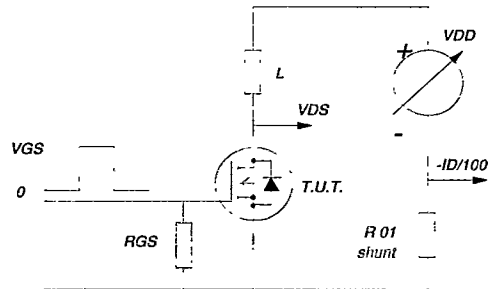


Fig. 16. Avalanche energy test circuit.
 $W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$