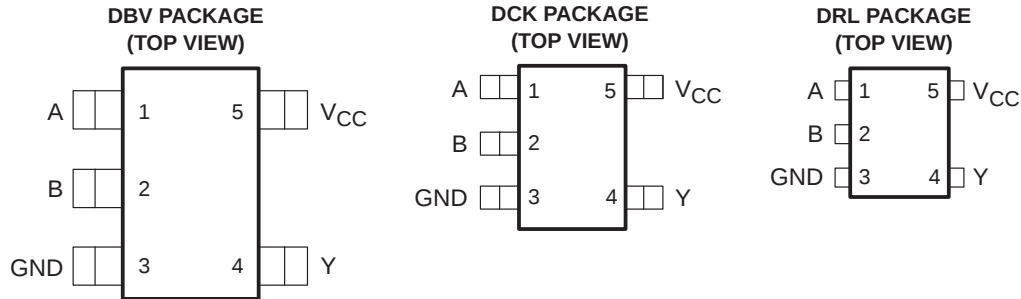


# SN74AHC1G86

## SINGLE 2-INPUT EXCLUSIVE-OR GATE

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- Operating Range of 2 V to 5.5 V
- Max  $t_{pd}$  of 8 ns at 5 V
- Low Power Consumption, 10- $\mu$ A Max  $I_{CC}$
- $\pm 8$ -mA Output Drive at 5 V
- Schmitt Trigger Action at All Inputs Makes the Circuit Tolerant for Slower Input Rise and Fall Time
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

### description/ordering information

The SN74AHC1G86 is a single 2-input exclusive-OR gate. The device performs the Boolean function  $Y = A \oplus B$  or  $Y = \bar{A}B + A\bar{B}$  in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

### ORDERING INFORMATION

| $T_A$         | PACKAGE <sup>†</sup> |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING <sup>‡</sup> |
|---------------|----------------------|--------------|-----------------------|-------------------------------|
| –40°C to 85°C | SOT (SOT-23) – DBV   | Reel of 3000 | SN74AHC1G86DBVR       | A86_                          |
|               |                      | Reel of 250  | SN74AHC1G86DBVT       |                               |
|               | SOT (SC-70) – DCK    | Reel of 3000 | SN74AHC1G86DCKR       | AH_                           |
|               |                      | Reel of 250  | SN74AHC1G86DCKT       |                               |
|               | SOT (SOT-553) – DRL  | Reel of 4000 | SN74AHC1G86DRLR       | AH_                           |
|               |                      |              |                       |                               |

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

<sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

### FUNCTION TABLE

| INPUTS |   | OUTPUT |
|--------|---|--------|
| A      | B | Y      |
| L      | L | L      |
| L      | H | H      |
| H      | L | H      |
| H      | H | L      |



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**TEXAS  
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SN74AHC1G86  
SINGLE 2-INPUT EXCLUSIVE-OR GATE

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exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These are five equivalent exclusive-OR symbols valid for an SN74AHC1G86 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



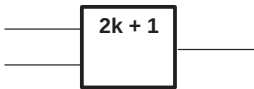
The output is active (low) if all inputs stand at the same logic level (i.e.,  $A = B$ ).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                    |                            |
|--------------------------------------------------------------------|----------------------------|
| Supply voltage range, $V_{CC}$                                     | –0.5 V to 7 V              |
| Input voltage range, $V_I$ (see Note 1)                            | –0.5 V to 7 V              |
| Output voltage range, $V_O$ (see Note 1)                           | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                        | –20 mA                     |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )     | ±20 mA                     |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )         | ±25 mA                     |
| Continuous current through $V_{CC}$ or GND                         | ±50 mA                     |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package | 206°C/W                    |
| DCK package                                                        | 252°C/W                    |
| DRL package                                                        | 142°C/W                    |
| Storage temperature range, $T_{Stg}$                               | –65°C to 150°C             |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

# SN74AHC1G86

## SINGLE 2-INPUT EXCLUSIVE-OR GATE

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### recommended operating conditions (see Note 3)

|                     |                                    |                                          | MIN  | MAX      | UNIT               |
|---------------------|------------------------------------|------------------------------------------|------|----------|--------------------|
| $V_{CC}$            | Supply voltage                     |                                          | 2    | 5.5      | V                  |
| $V_{IH}$            | High-level input voltage           | $V_{CC} = 2\text{ V}$                    | 1.5  |          | V                  |
|                     |                                    | $V_{CC} = 3\text{ V}$                    | 2.1  |          |                    |
|                     |                                    | $V_{CC} = 5.5\text{ V}$                  | 3.85 |          |                    |
| $V_{IL}$            | Low-level input voltage            | $V_{CC} = 2\text{ V}$                    |      | 0.5      | V                  |
|                     |                                    | $V_{CC} = 3\text{ V}$                    |      | 0.9      |                    |
|                     |                                    | $V_{CC} = 5.5\text{ V}$                  |      | 1.65     |                    |
| $V_I$               | Input voltage                      |                                          | 0    | 5.5      | V                  |
| $V_O$               | Output voltage                     |                                          | 0    | $V_{CC}$ | V                  |
| $I_{OH}$            | High-level output current          | $V_{CC} = 2\text{ V}$                    |      | -50      | $\mu\text{A}$      |
|                     |                                    | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |      | -4       | mA                 |
|                     |                                    | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$   |      | -8       |                    |
| $I_{OL}$            | Low-level output current           | $V_{CC} = 2\text{ V}$                    |      | 50       | $\mu\text{A}$      |
|                     |                                    | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |      | 4        | mA                 |
|                     |                                    | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$   |      | 8        |                    |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |      | 100      | ns/V               |
|                     |                                    | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$   |      | 20       |                    |
| $T_A$               | Operating free-air temperature     |                                          | -40  | 85       | $^{\circ}\text{C}$ |

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS                   | $V_{CC}$     | $T_A = 25^{\circ}\text{C}$ |     |           | MIN  | MAX     | UNIT          |
|-----------|-----------------------------------|--------------|----------------------------|-----|-----------|------|---------|---------------|
|           |                                   |              | MIN                        | TYP | MAX       |      |         |               |
| $V_{OH}$  | $I_{OH} = -50\text{ }\mu\text{A}$ | 2 V          | 1.9                        | 2   |           | 1.9  |         | V             |
|           |                                   | 3 V          | 2.9                        | 3   |           | 2.9  |         |               |
|           |                                   | 4.5 V        | 4.4                        | 4.5 |           | 4.4  |         |               |
|           | $I_{OH} = -4\text{ mA}$           | 3 V          | 2.58                       |     |           | 2.48 |         |               |
|           | $I_{OH} = -8\text{ mA}$           | 4.5 V        | 3.94                       |     |           | 3.8  |         |               |
| $V_{OL}$  | $I_{OL} = 50\text{ }\mu\text{A}$  | 2 V          |                            |     | 0.1       |      | 0.1     | V             |
|           |                                   | 3 V          |                            |     | 0.1       |      | 0.1     |               |
|           |                                   | 4.5 V        |                            |     | 0.1       |      | 0.1     |               |
|           | $I_{OL} = 4\text{ mA}$            | 3 V          |                            |     | 0.36      |      | 0.44    |               |
|           | $I_{OL} = 8\text{ mA}$            | 4.5 V        |                            |     | 0.36      |      | 0.44    |               |
| $I_I$     | $V_I = 5.5\text{ V}$ or GND       | 0 V to 5.5 V |                            |     | $\pm 0.1$ |      | $\pm 1$ | $\mu\text{A}$ |
| $I_{CC}$  | $V_I = V_{CC}$ or GND, $I_O = 0$  | 5.5 V        |                            |     | 1         |      | 10      | $\mu\text{A}$ |
| $C_i$     | $V_I = V_{CC}$ or GND             | 5 V          |                            | 4   | 10        |      | 10      | pF            |



# SN74AHC1G86

## SINGLE 2-INPUT EXCLUSIVE-OR GATE

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE  | $T_A = 25^\circ\text{C}$ |      |     | MIN | MAX  | UNIT |
|-----------|-----------------|----------------|----------------------|--------------------------|------|-----|-----|------|------|
|           |                 |                |                      | MIN                      | TYP  | MAX |     |      |      |
| $t_{PLH}$ | A or B          | Y              | $C_L = 15\text{ pF}$ | 7                        | 11   |     | 1   | 13   | ns   |
| $t_{PHL}$ |                 |                |                      | 7                        | 11   |     | 1   | 13   |      |
| $t_{PLH}$ | A or B          | Y              | $C_L = 50\text{ pF}$ | 9.5                      | 14.5 |     | 1   | 16.5 | ns   |
| $t_{PHL}$ |                 |                |                      | 9.5                      | 14.5 |     | 1   | 16.5 |      |

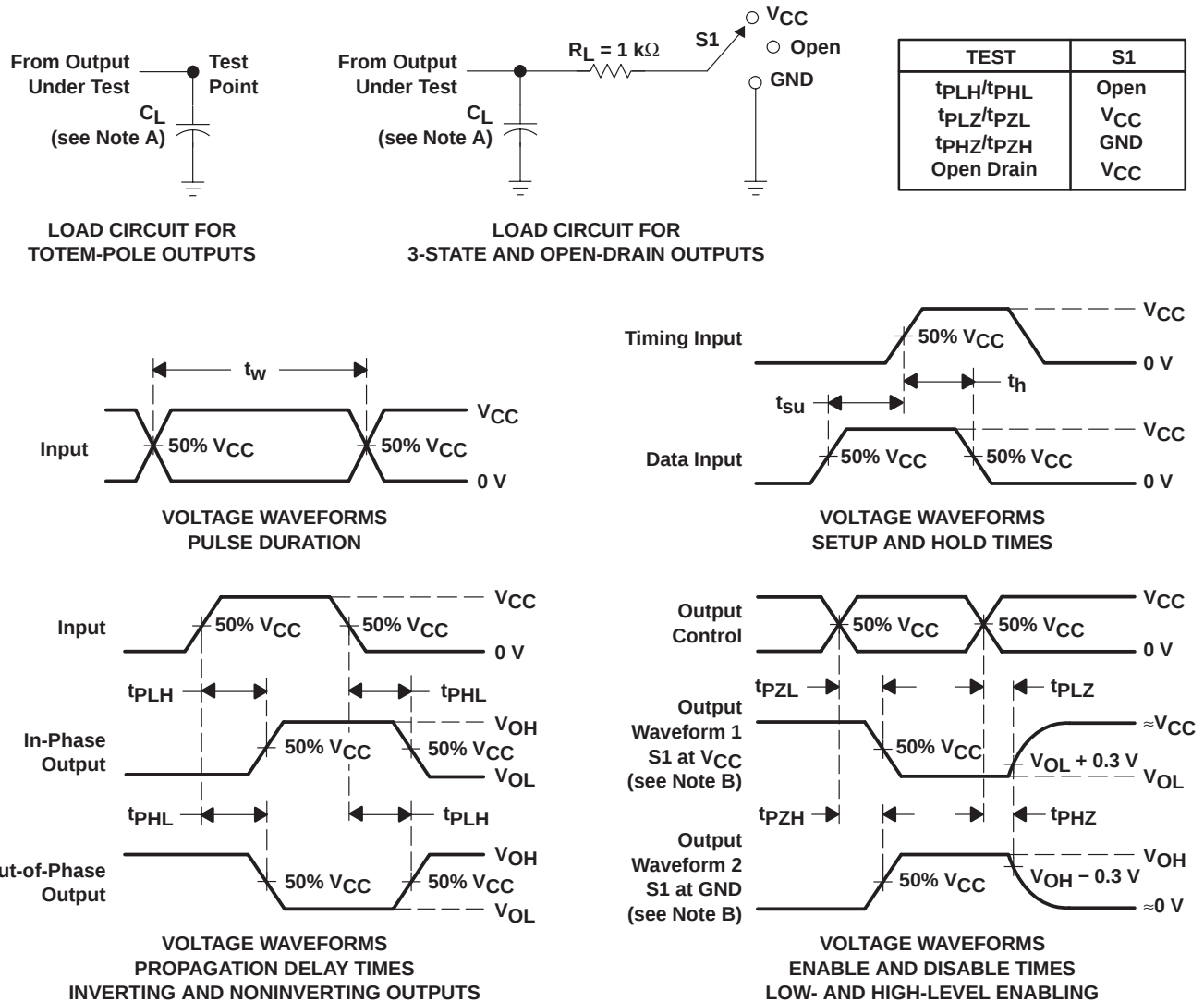
switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE  | $T_A = 25^\circ\text{C}$ |     |     | MIN | MAX | UNIT |
|-----------|-----------------|----------------|----------------------|--------------------------|-----|-----|-----|-----|------|
|           |                 |                |                      | MIN                      | TYP | MAX |     |     |      |
| $t_{PLH}$ | A or B          | Y              | $C_L = 15\text{ pF}$ | 4.8                      | 6.8 |     | 1   | 8   | ns   |
| $t_{PHL}$ |                 |                |                      | 4.8                      | 6.8 |     | 1   | 8   |      |
| $t_{PLH}$ | A or B          | Y              | $C_L = 50\text{ pF}$ | 6.3                      | 8.8 |     | 1   | 10  | ns   |
| $t_{PHL}$ |                 |                |                      | 6.3                      | 8.8 |     | 1   | 10  |      |

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER |                               | TEST CONDITIONS             | TYP | UNIT |
|-----------|-------------------------------|-----------------------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance | No load, $f = 1\text{ MHz}$ | 18  | pF   |

### PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - D. The outputs are measured one at a time, with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

| Orderable Device  | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4)                 | Samples                 |
|-------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|------------------------------------------|-------------------------|
| SN74AHC1G86DBVG4  | ACTIVE        | SOT-23       | DBV                | 5    |                | TBD                        | Call TI          | Call TI              | -40 to 85    |                                          | <a href="#">Samples</a> |
| SN74AHC1G86DBVR   | ACTIVE        | SOT-23       | DBV                | 5    | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | (A862 ~ A863 ~<br>A86G ~ A86J ~<br>A86S) | <a href="#">Samples</a> |
| SN74AHC1G86DBVRE4 | ACTIVE        | SOT-23       | DBV                | 5    | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | (A862 ~ A863 ~<br>A86G ~ A86J ~<br>A86S) | <a href="#">Samples</a> |
| SN74AHC1G86DBVRG4 | ACTIVE        | SOT-23       | DBV                | 5    | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | (A862 ~ A863 ~<br>A86G ~ A86J ~<br>A86S) | <a href="#">Samples</a> |
| SN74AHC1G86DBVT   | ACTIVE        | SOT-23       | DBV                | 5    | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | (A862 ~ A863 ~<br>A86G ~ A86S)           | <a href="#">Samples</a> |
| SN74AHC1G86DBVTE4 | ACTIVE        | SOT-23       | DBV                | 5    | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | (A862 ~ A863 ~<br>A86G ~ A86S)           | <a href="#">Samples</a> |
| SN74AHC1G86DBVTG4 | ACTIVE        | SOT-23       | DBV                | 5    | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | (A862 ~ A863 ~<br>A86G ~ A86S)           | <a href="#">Samples</a> |
| SN74AHC1G86DCKR   | ACTIVE        | SC70         | DCK                | 5    | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | (AH3 ~ AHG ~ AHJ ~<br>AHS)               | <a href="#">Samples</a> |
| SN74AHC1G86DCKRE4 | ACTIVE        | SC70         | DCK                | 5    | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | (AH3 ~ AHG ~ AHJ ~<br>AHS)               | <a href="#">Samples</a> |
| SN74AHC1G86DCKRG4 | ACTIVE        | SC70         | DCK                | 5    | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | (AH3 ~ AHG ~ AHJ ~<br>AHS)               | <a href="#">Samples</a> |
| SN74AHC1G86DCKT   | ACTIVE        | SC70         | DCK                | 5    | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | (AH3 ~ AHG ~ AHS)                        | <a href="#">Samples</a> |
| SN74AHC1G86DCKTE4 | ACTIVE        | SC70         | DCK                | 5    | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | (AH3 ~ AHG ~ AHS)                        | <a href="#">Samples</a> |
| SN74AHC1G86DCKTG4 | ACTIVE        | SC70         | DCK                | 5    | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | (AH3 ~ AHG ~ AHS)                        | <a href="#">Samples</a> |
| SN74AHC1G86DRLR   | ACTIVE        | SOT          | DRL                | 5    | 4000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | AHS                                      | <a href="#">Samples</a> |
| SN74AHC1G86DRLRG4 | ACTIVE        | SOT          | DRL                | 5    | 4000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | AHS                                      | <a href="#">Samples</a> |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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#### **OTHER QUALIFIED VERSIONS OF SN74AHC1G86 :**

- Automotive: [SN74AHC1G86-Q1](#)
- Enhanced Product: [SN74AHC1G86-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHC1G86DBVR | SOT-23       | DBV             | 5    | 3000 | 178.0              | 9.2                | 3.3     | 3.2     | 1.55    | 4.0     | 8.0    | Q3            |
| SN74AHC1G86DBVT | SOT-23       | DBV             | 5    | 250  | 178.0              | 9.0                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| SN74AHC1G86DBVT | SOT-23       | DBV             | 5    | 250  | 178.0              | 9.2                | 3.3     | 3.2     | 1.55    | 4.0     | 8.0    | Q3            |
| SN74AHC1G86DCKR | SC70         | DCK             | 5    | 3000 | 178.0              | 9.2                | 2.4     | 2.4     | 1.22    | 4.0     | 8.0    | Q3            |
| SN74AHC1G86DCKR | SC70         | DCK             | 5    | 3000 | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| SN74AHC1G86DCKT | SC70         | DCK             | 5    | 250  | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| SN74AHC1G86DCKT | SC70         | DCK             | 5    | 250  | 178.0              | 9.2                | 2.4     | 2.4     | 1.22    | 4.0     | 8.0    | Q3            |
| SN74AHC1G86DRLR | SOT          | DRL             | 5    | 4000 | 180.0              | 8.4                | 1.98    | 1.78    | 0.69    | 4.0     | 8.0    | Q3            |

## TAPE AND REEL BOX DIMENSIONS

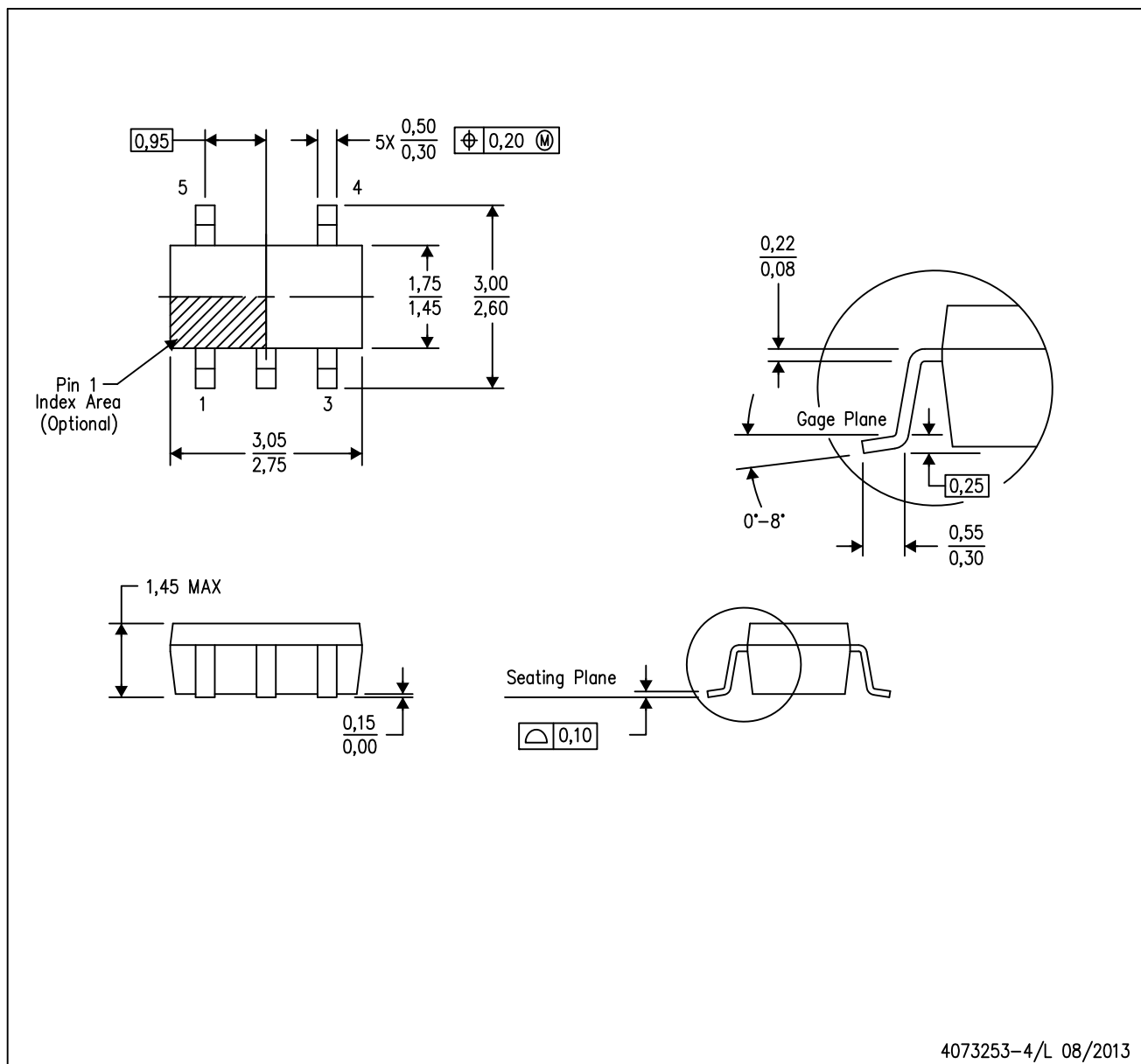


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHC1G86DBVR | SOT-23       | DBV             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74AHC1G86DBVT | SOT-23       | DBV             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| SN74AHC1G86DBVT | SOT-23       | DBV             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| SN74AHC1G86DCKR | SC70         | DCK             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74AHC1G86DCKR | SC70         | DCK             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74AHC1G86DCKT | SC70         | DCK             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| SN74AHC1G86DCKT | SC70         | DCK             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| SN74AHC1G86DRLR | SOT          | DRL             | 5    | 4000 | 202.0       | 201.0      | 28.0        |

DBV (R-PDSO-G5)

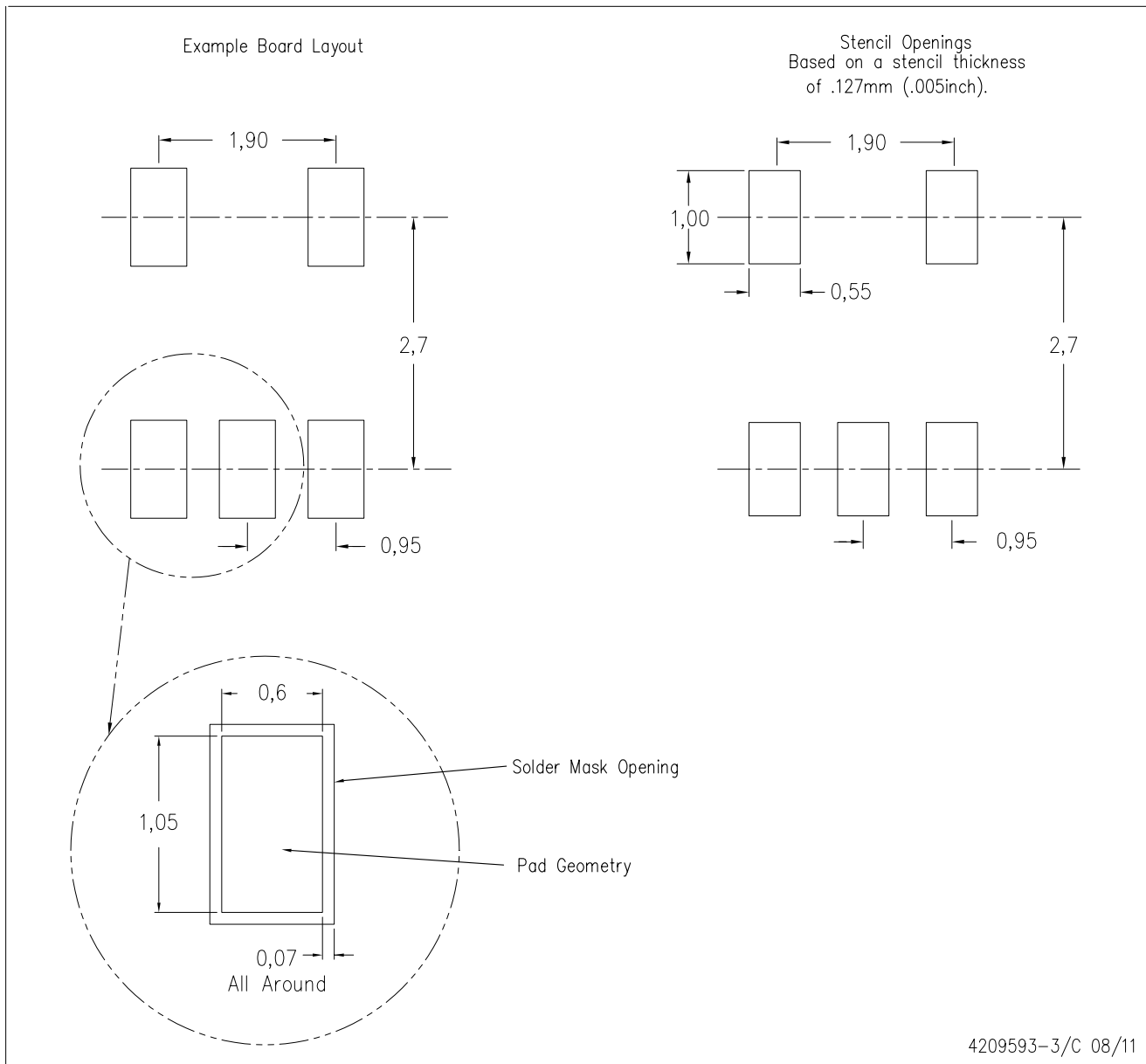
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

## DCK (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

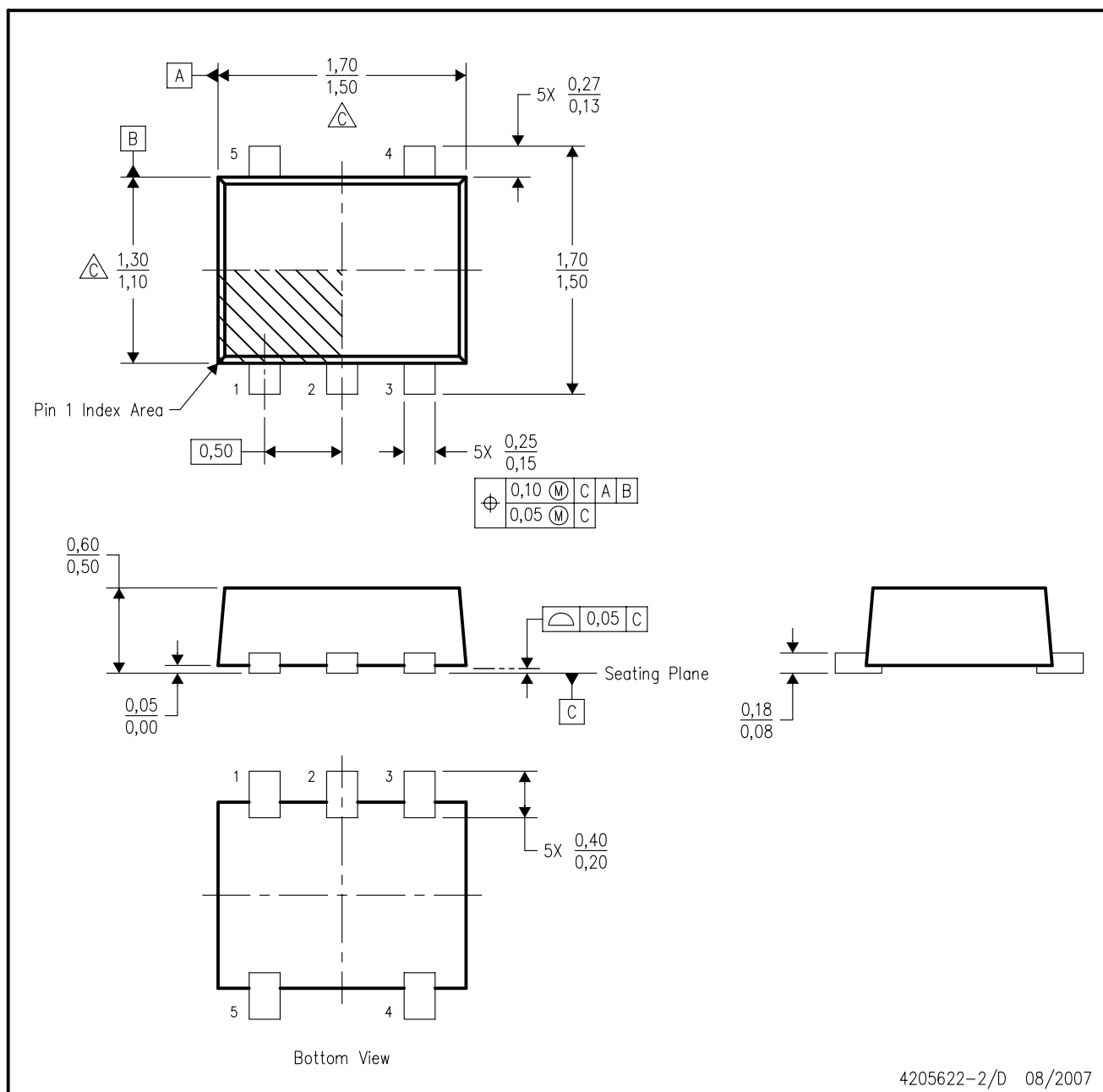
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



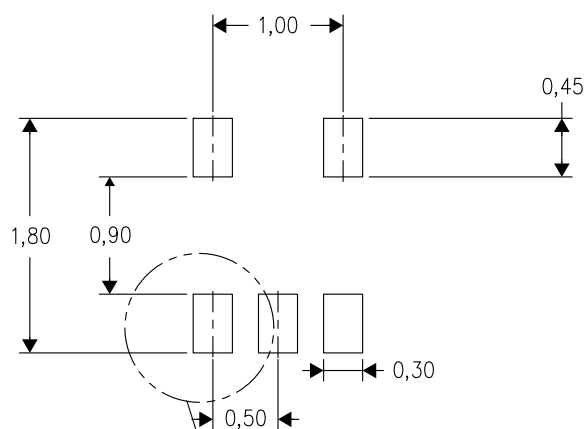
4205622-2/D 08/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
  - D. JEDEC package registration is pending.

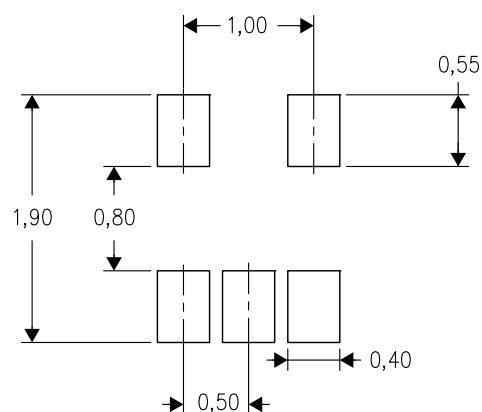
DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE

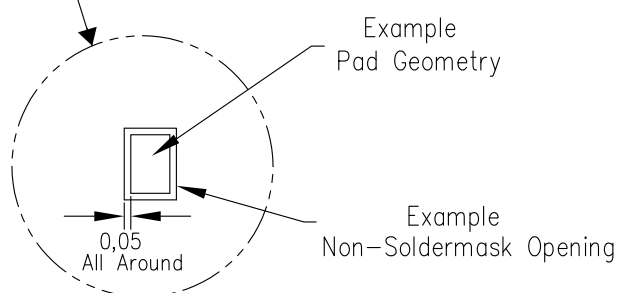
Example Board Layout



Example Stencil Design  
(Note E)



Example  
Non-Soldermask Defined Pad



4208207-2/E 06/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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