

HD74HCT373, HD74HCT533

Octal D-type Transparent Latches (with 3-state outputs)

Octal D-type Transparent Latches (with inverted 3-state outputs)

REJ03D0666-0200
(Previous ADE-205-555)
Rev.2.00
Mar 30, 2006

Description

When the latch enable input is high, the Q outputs of HD74HCT373 will follow the D inputs and the Q outputs of HD74HCT533 will follow the inversion of the D inputs. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals present at the other inputs and the state of the storage elements.

Features

- LSTTL Output Logic Level Compatibility as well as CMOS Output Compatibility
- High Speed Operation: t_{pd} (Data to Q) = 14 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 4.5$ to 5.5 V
- Low Input Current: $1 \mu A$ max
- Low Quiescent Supply Current: I_{CC} (static) = $4 \mu A$ max ($T_a = 25^\circ C$)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HCT373P	DILP-20 pin	PRDP0020AC-B (DP-20NEV)	P	—
HD74HCT373FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)
HD74HCT373RPEL HD74HCT533RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)
HD74HCT373TELL	TSSOP-20 pin	PTSP0020JB-A (TTP-20DAV)	T	ELL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

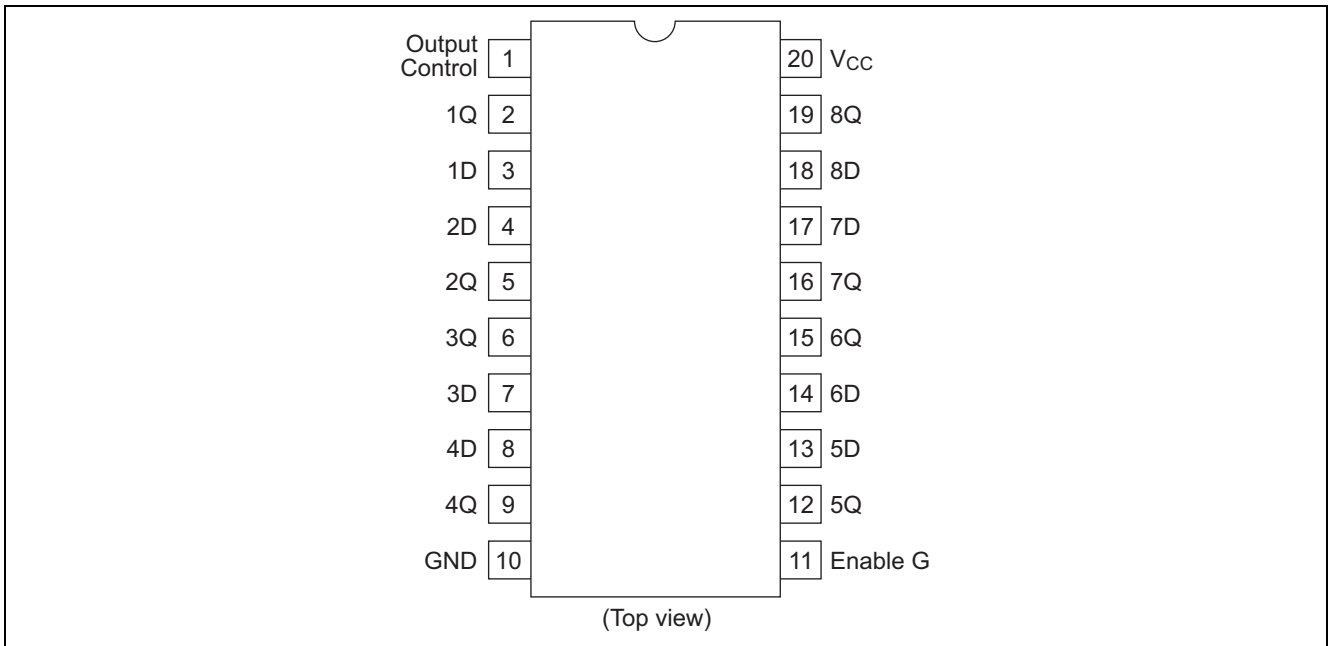
Function Table

Output Control	Enable G	D	HD74HCT373 Q	HD74HCT533 $\bar{Q}$
L	H	H	H	L
L	H	L	L	H
L	L	X	No change	No change
H	X	X	Z	Z

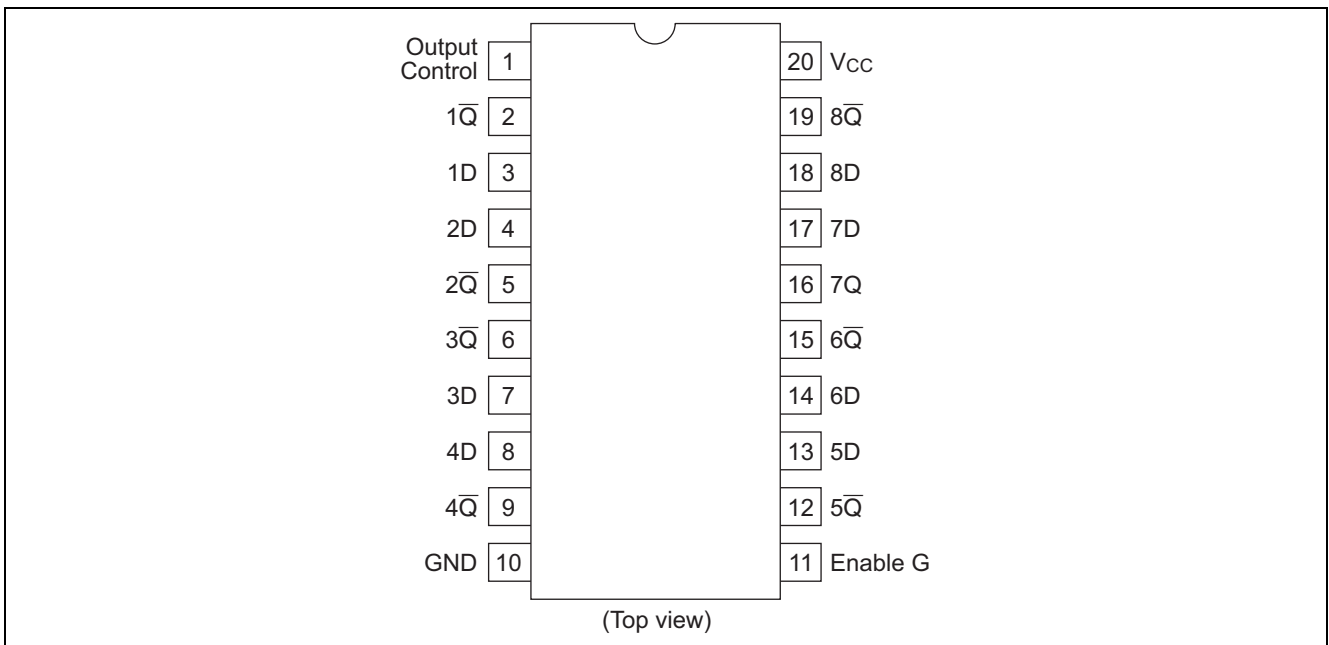
Notes: 1. H; High level, L; Low level, X; Irrelevant, Z; High impedance

Pin Arrangement

HD74HCT373

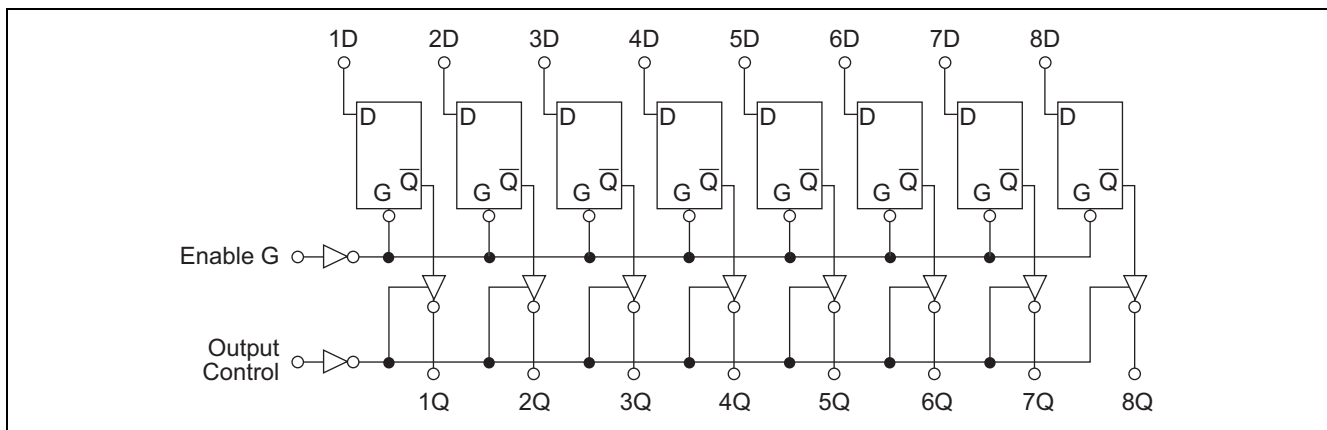


HD74HCT533

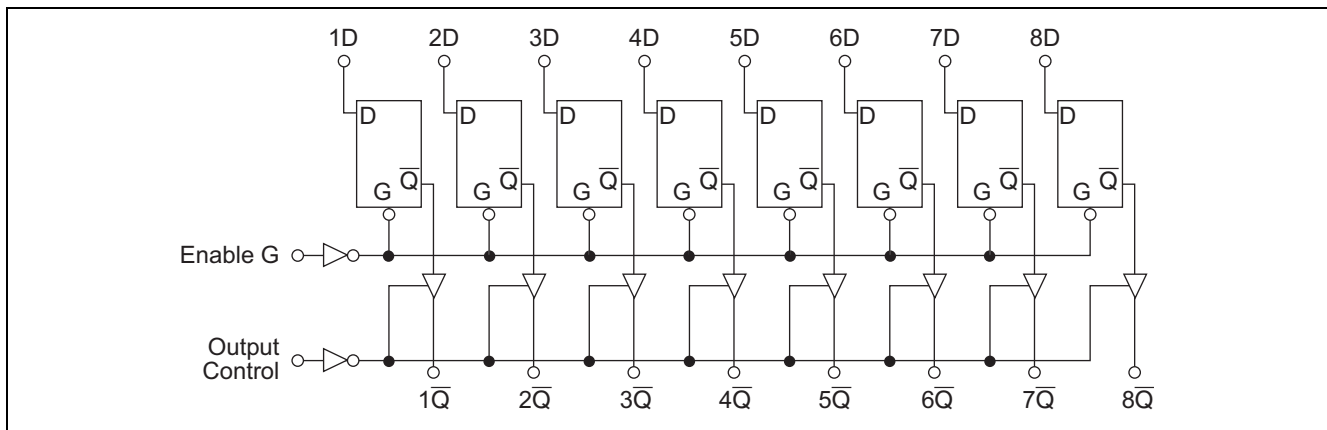


Logic Diagram

HD74HCT373



HD74HCT533



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{IN}, V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	I_{IK}, I_{OK}	± 20	mA
Output current	I_{OUT}	± 35	mA
V_{CC} , GND current	I_{CC} or I_{GND}	± 75	mA
Power dissipation	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	4.5 to 5.5	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	T_a	-40 to 85	°C	
Input rise / fall time ^{*1}	t_r, t_f	0 to 500	ns	$V_{CC} = 4.5$ V

Notes: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

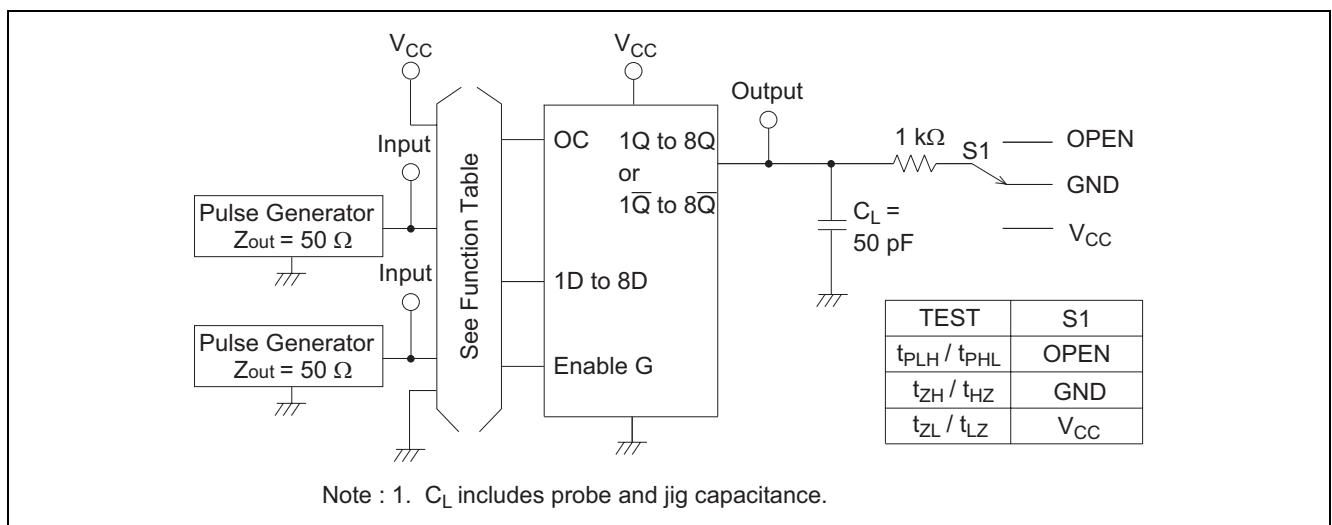
Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	4.5 to 5.5	2.0	—	—	2.0	—	V		
	V _{IL}	4.5 to 5.5	—	—	0.8	—	0.8	V		
Output voltage	V _{OH}	4.5	4.4	—	—	4.4	—	V	Vin = V _{IH} or V _{IL}	I _{OH} = -20 μA
		4.5	4.18	—	—	4.13	—			I _{OH} = -6 mA
	V _{OL}	4.5	—	—	0.1	—	0.1	V	Vin = V _{IH} or V _{IL}	I _{OL} = 20 μA
		4.5	—	—	0.26	—	0.33			I _{OL} = 6 mA
Off-state output current	I _{OZ}	5.5	—	—	±0.5	—	±5.0	μA	Vin = V _{IH} or V _{IL} , Vout = V _{CC} or GND	
Input current	I _{in}	5.5	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent current	I _{CC}	5.5	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, Iout = 0 μA	

Switching Characteristics

(C_L = 50 pF, Input t_r = t_f = 6 ns)

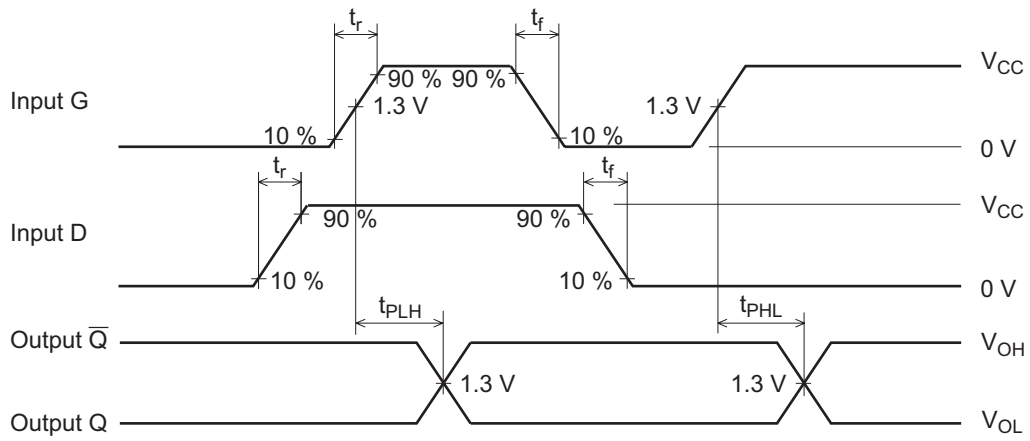
Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Propagation delay time	t _{PLH}	4.5	—	13	30	—	38	ns	Latch control to Q	
	t _{PHL}	4.5	—	16	30	—	38			
	t _{PLH}	4.5	—	14	25	—	31	ns	Data to Q	
	t _{PHL}	4.5	—	12	25	—	31			
Output enable time	t _{ZL}	4.5	—	16	30	—	38	ns		
	t _{ZH}	4.5	—	15	30	—	38			
Output disable time	t _{LZ}	4.5	—	14	30	—	38	ns		
	t _{HZ}	4.5	—	16	30	—	38			
Setup time	t _{SU}	4.5	20	—	—	25	—	ns	Data to latch control	
Hold time	t _H	4.5	10	—	—	13	—	ns	Latch control to data	
Pulse width	t _w	4.5	16	—	—	20	—	ns	Latch control, output control	
Output rise/fall time	t _{TLH}	4.5	—	4	12	—	15	ns		
	t _{THL}	4.5	—	—	—	—	—			
Input capacitance	C _{in}	—	—	5	10	—	10	pF		

Test Circuit

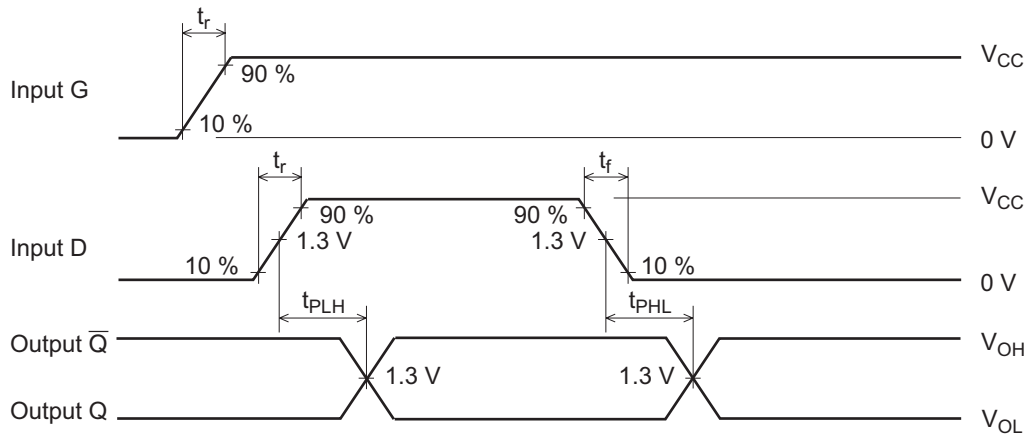


Waveforms

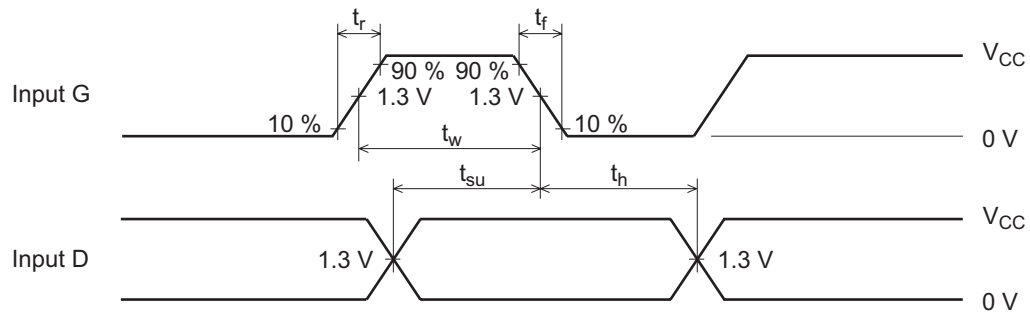
• Waveform – 1



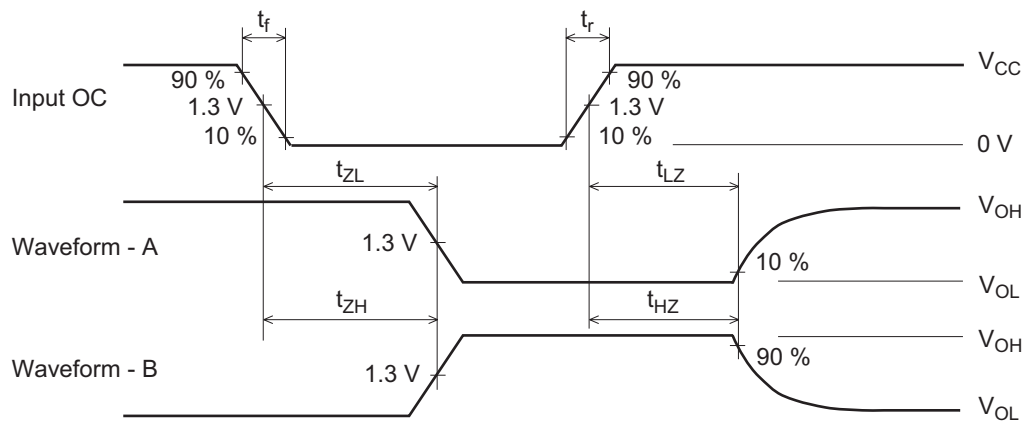
• Waveform – 2



• Waveform – 3

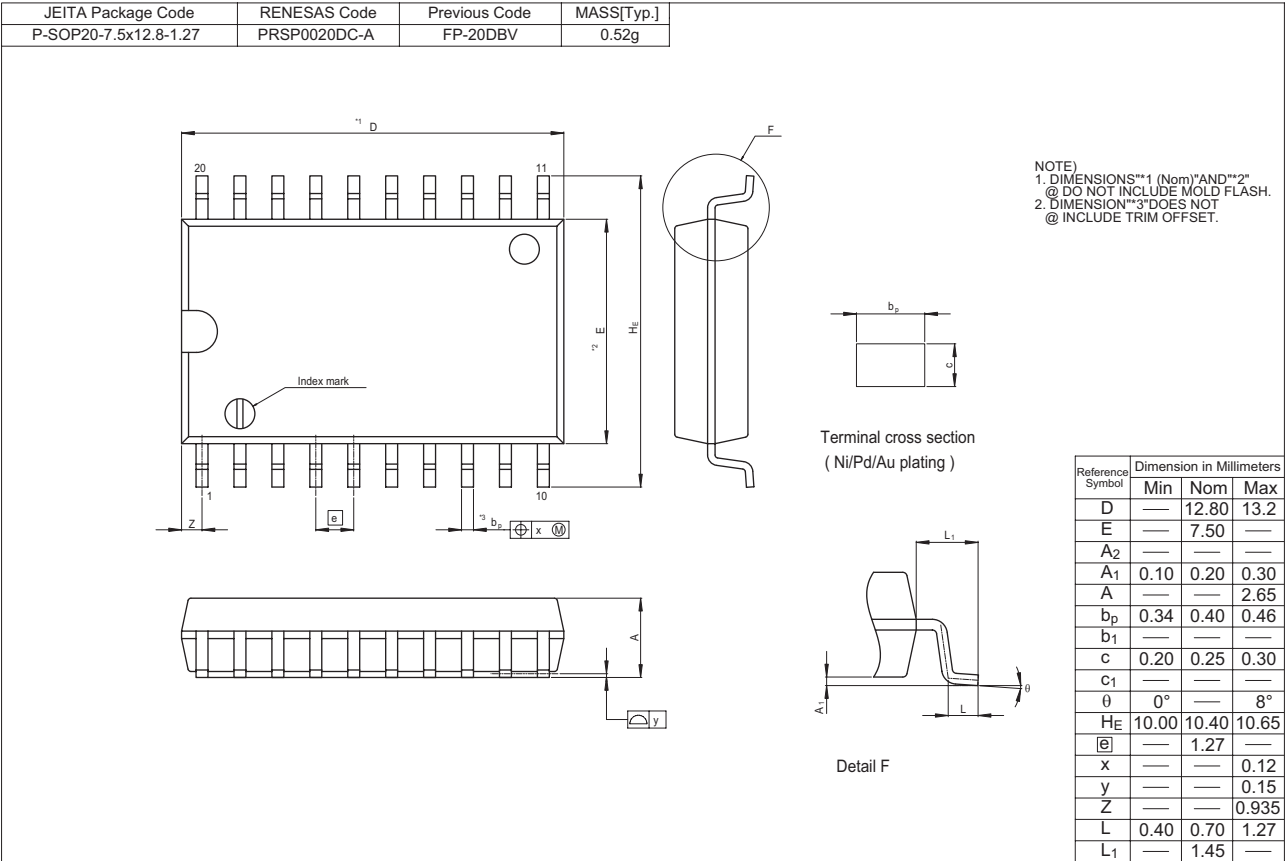
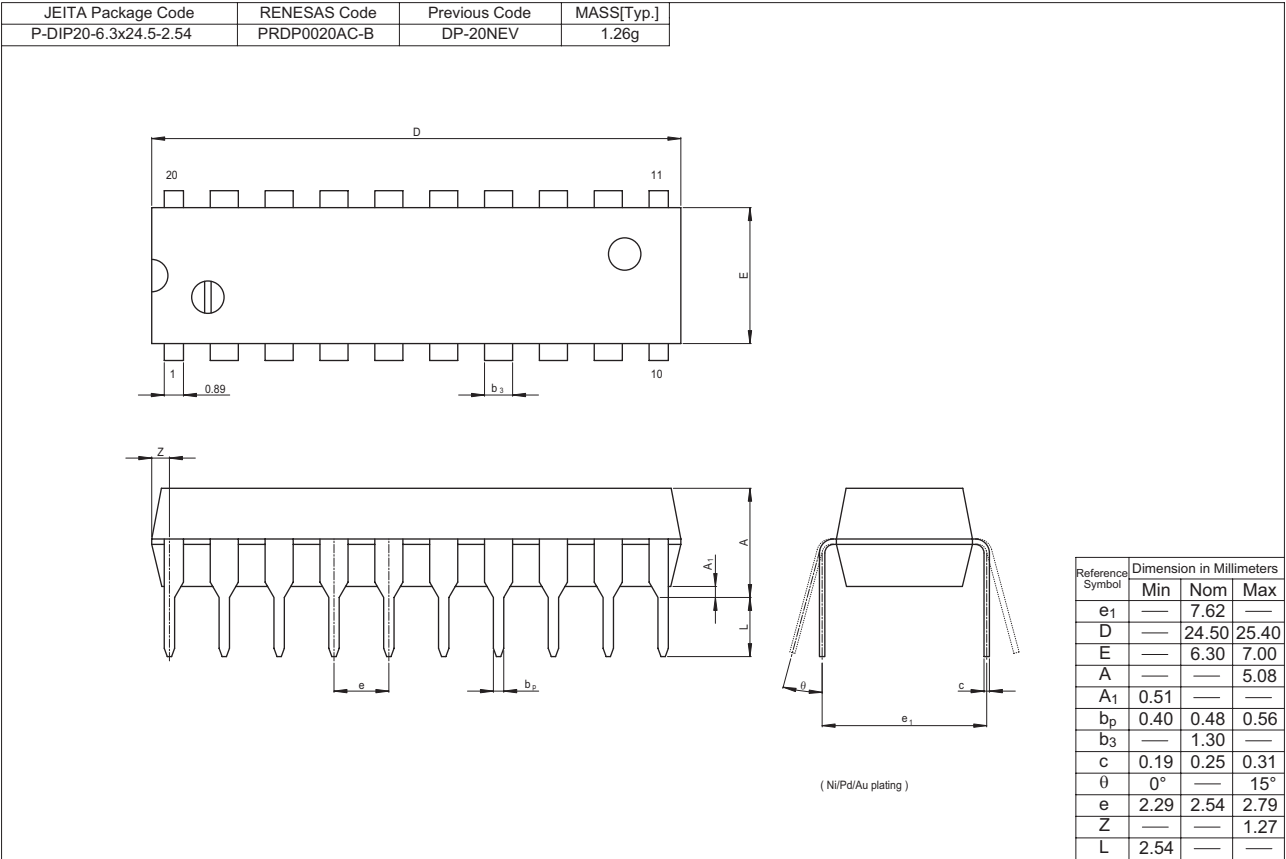


• Waveform – 4

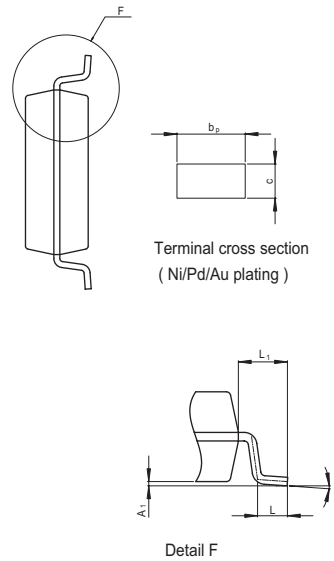
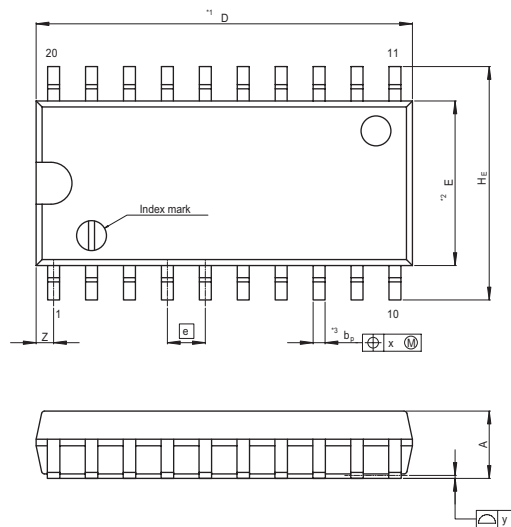


- Notes :
1. Input waveform : $PRR \leq 1 \text{ MHz}$, duty cycle 50%, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$
 2. Waveform– A is for an output with internal conditions such that the output is low except when disabled by the output control.
 3. Waveform– B is for an output with internal conditions such that the output is high except when disabled by the output control.
 4. The output are measured one at a time with one transition per measurement.

Package Dimensions



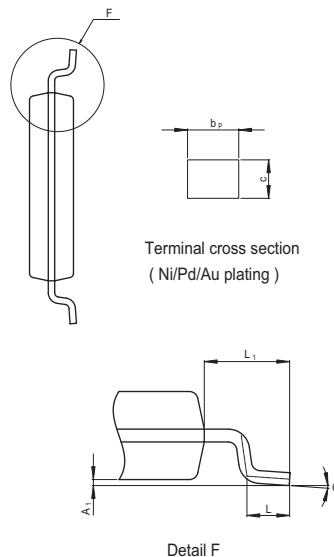
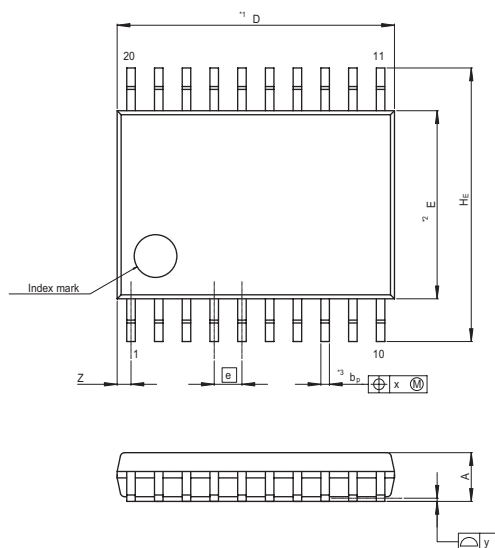
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-5.5x12.6-1.27	PRSP0020DD-B	FP-20DAV	0.31g



NOTE)
1. DIMENSIONS**1 (Nom)"AND**2"
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION**3"DOES NOT
INCLUDE TRIM OFFSET.

Reference Symbol	Min	Nom	Max
D	—	12.60	13.0
E	—	5.50	—
A ₂	—	—	—
A ₁	0.00	0.10	0.20
A	—	—	2.20
b _p	0.34	0.40	0.46
b ₁	—	—	—
c	0.15	0.20	0.25
c ₁	—	—	—
θ	0°	—	8°
H _E	7.50	7.80	8.00
⓪	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.80
L	0.50	0.70	0.90
L ₁	—	1.15	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP20-4.4x6.5-0.65	PTSP0020JB-A	TTP-20DAV	0.07g



NOTE)
1. DIMENSIONS**1 (Nom)"AND**2"
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION**3"DOES NOT
INCLUDE TRIM OFFSET.

Reference Symbol	Min	Nom	Max
D	—	6.50	6.80
E	—	4.40	—
A ₂	—	—	—
A ₁	0.03	0.07	0.10
A	—	—	1.10
b _p	0.15	0.20	0.25
b ₁	—	—	—
c	0.10	0.15	0.20
c ₁	—	—	—
θ	0°	—	8°
H _E	6.20	6.40	6.60
⓪	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.65
L	0.4	0.5	0.6
L ₁	—	1.0	—

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Renesas Technology America, Inc.

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Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.

Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
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Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

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Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510