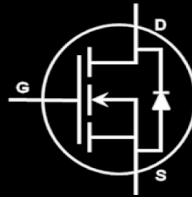


# EPC2016 – Enhancement Mode Power Transistor

 $V_{DSS}, 100\text{ V}$ 

NEW PRODUCT

 $R_{DS(ON)}, 16\text{ m}\Omega$ 
 $I_D, 11\text{ A}$ 


Gallium Nitride is grown on Silicon Wafers and processed using standard CMOS equipment leveraging the infrastructure that has been developed over the last 55 years. GaN's exceptionally high electron mobility and low temperature coefficient allows very low  $R_{DS(ON)}$ , while its lateral device structure and majority carrier diode provide exceptionally low  $Q_G$  and zero  $Q_{RR}$ . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.



EPC2016 eGaN® FETs are supplied only in passivated die form with solder bars

### Applications

- High Speed DC-DC conversion
- Class D Audio
- Hard Switched and High Frequency Circuits

### Benefits

- Ultra High Efficiency
- Ultra Low  $R_{DS(on)}$
- Ultra low  $Q_G$
- Ultra small footprint

Maximum Ratings			
$V_{DS}$	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5ms pulses at 125° C)	120	V
$I_D$	Continuous ( $T_A = 25^\circ\text{C}, \theta_{JA} = 32$ )	11	A
	Pulsed (25° C, $T_{pulse} = 300\ \mu\text{s}$ )	50	
$V_{GS}$	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-5	
$T_J$	Operating Temperature	-40 to 125	°C
$T_{STG}$	Storage Temperature	-40 to 150	

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>Static Characteristics</b> ( $T_J = 25^\circ\text{C}$ unless otherwise stated)						
$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 200\ \mu\text{A}$	100		V	
$I_{DSS}$	Drain Source Leakage	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$		25	150	$\mu\text{A}$
$I_{GSS}$	Gate-Source Forward Leakage	$V_{GS} = 5\text{ V}$		0.5	3	mA
	Gate-Source Reverse Leakage	$V_{GS} = -5\text{ V}$		0.1	0.5	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 3\text{ mA}$	0.7	1.4	2.5	V
$R_{DS(ON)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}, I_D = 11\text{ A}$		12	16	$\text{m}\Omega$
<b>Source-Drain Characteristics</b> ( $T_J = 25^\circ\text{C}$ unless otherwise stated)						
$V_{SD}$	Source-Drain Forward Voltage	$I_S = 0.5\text{ A}, V_{GS} = 0\text{ V}, T = 25^\circ\text{C}$		1.68		V
		$I_S = 0.5\text{ A}, V_{GS} = 0\text{ V}, T = 125^\circ\text{C}$		1.73		

All measurements were done with substrate shorted to source.

Thermal Characteristics				
			TYP	
$R_{\theta JC}$	Thermal Resistance, Junction to Case		3.6	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board		19	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)		69	°C/W

Note 1:  $R_{\theta JA}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See [http://epc-co.com/epc/documents/product-training/Appnote\\_Thermal\\_Performance\\_of\\_eGaN\\_FETs.pdf](http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf) for details.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Dynamic Characteristics</b> ( $T_J = 25^\circ\text{C}$ unless otherwise stated)						
$C_{ISS}$	Input Capacitance	$V_{DS} = 50\text{V}, V_{GS} = 0\text{V}$		433	520	pF
$C_{OSS}$	Output Capacitance			225	280	
$C_{RSS}$	Reverse Transfer Capacitance			4.3	6	
$Q_G$	Total Gate Charge ( $V_{GS} = 5\text{V}$ )	$V_{DS} = 50\text{V}, I_D = 11\text{A}$		3.8	5.2	nC
$Q_{GD}$	Gate to Drain Charge			0.70	1.4	
$Q_{GS}$	Gate to Source Charge			0.99	1.5	
$Q_{OSS}$	Output Charge			20	30	
$Q_{RR}$	Source-Drain Recovery Charge			0	0	

All measurements were done with substrate shorted to source.

Figure 1: Typical Output Characteristics

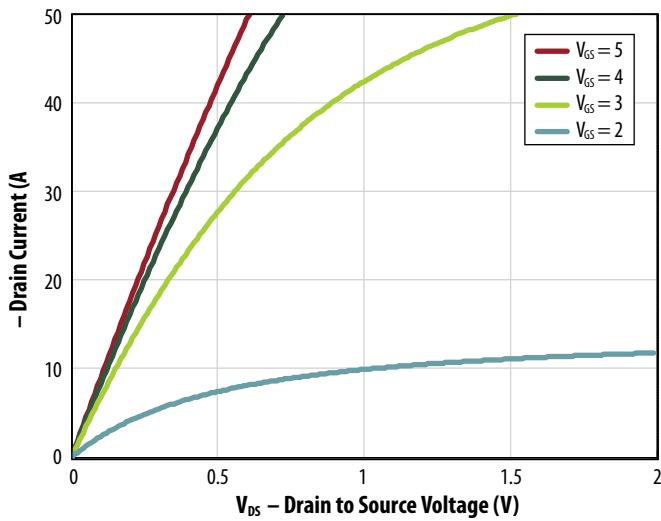


Figure 2: Transfer Characteristics

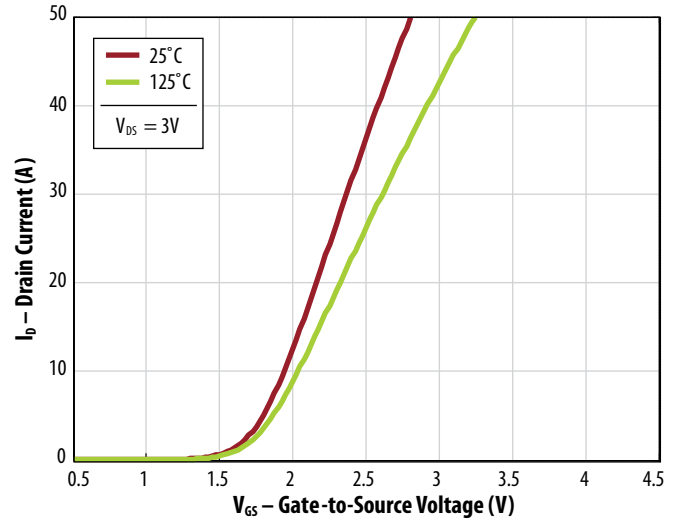


Figure 3:  $R_{DS(on)}$  vs  $V_{GS}$  for Various Drain Currents

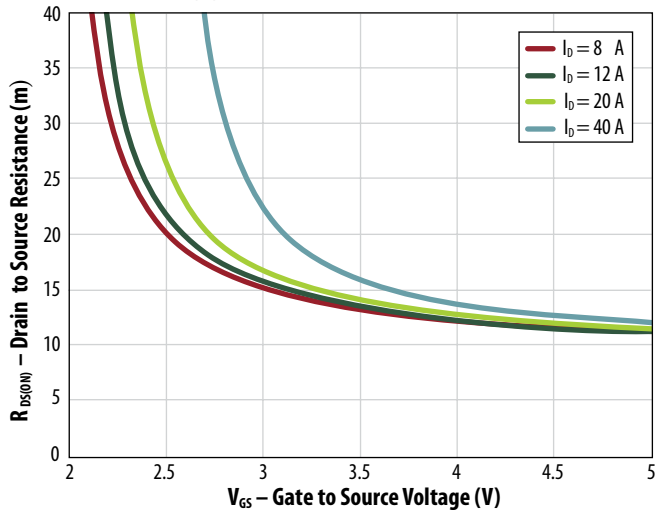


Figure 4:  $R_{DS(on)}$  vs  $V_{GS}$  for Various Temperatures

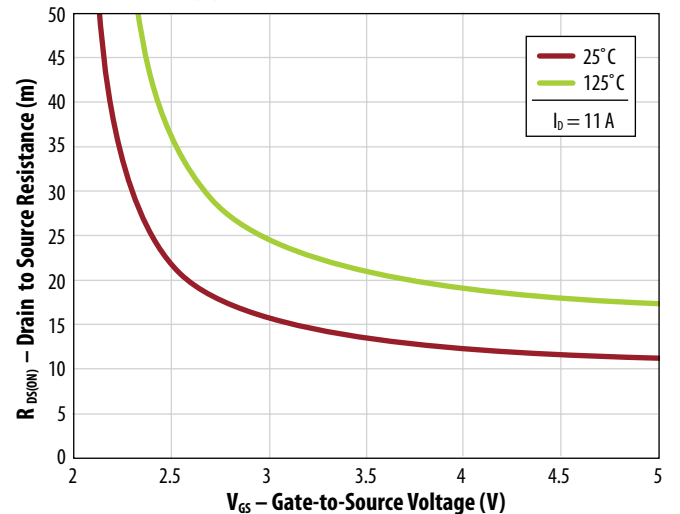


Figure 5: Capacitance

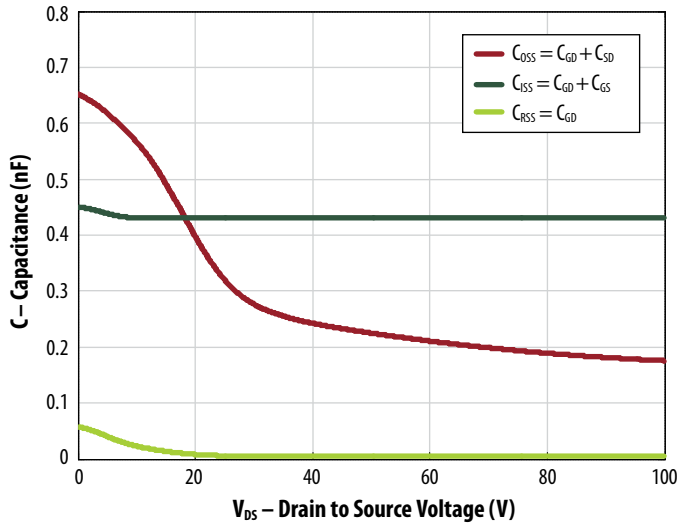


Figure 6: Gate Charge

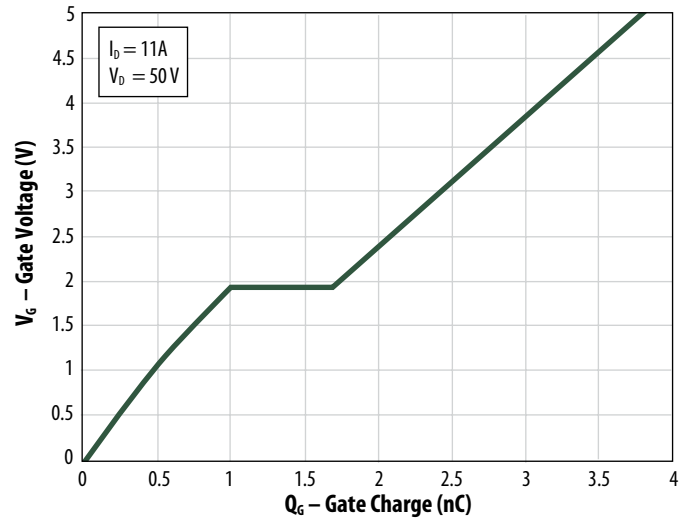


Figure 7: Reverse Drain-Source Characteristics

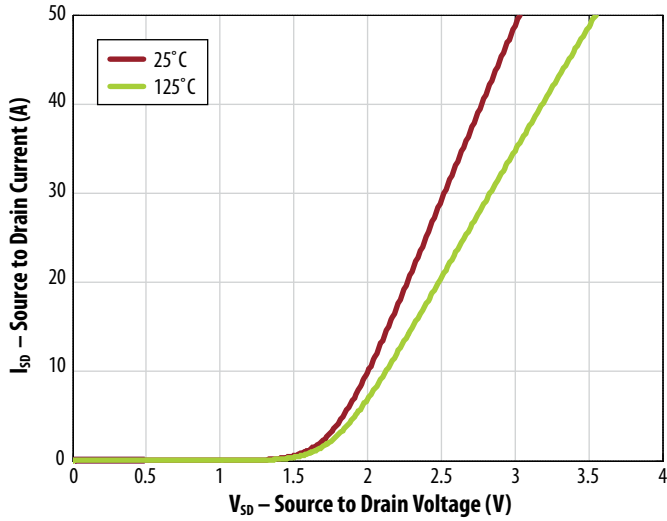


Figure 8: Normalized On Resistance vs. Temperature

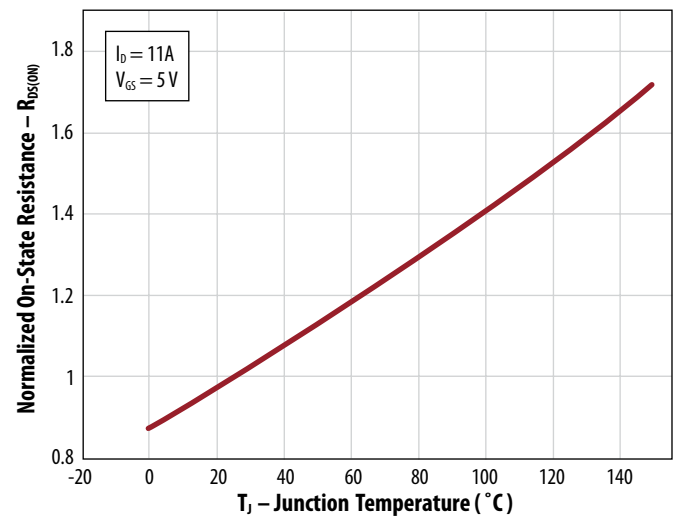


Figure 9: Normalized Threshold Voltage vs. Temperature

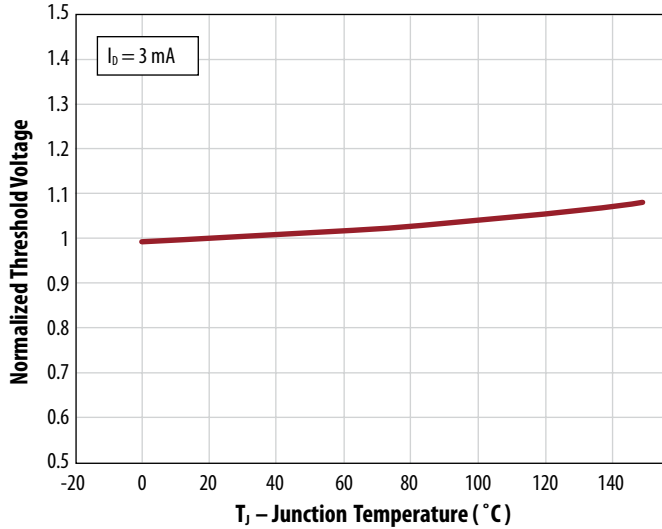
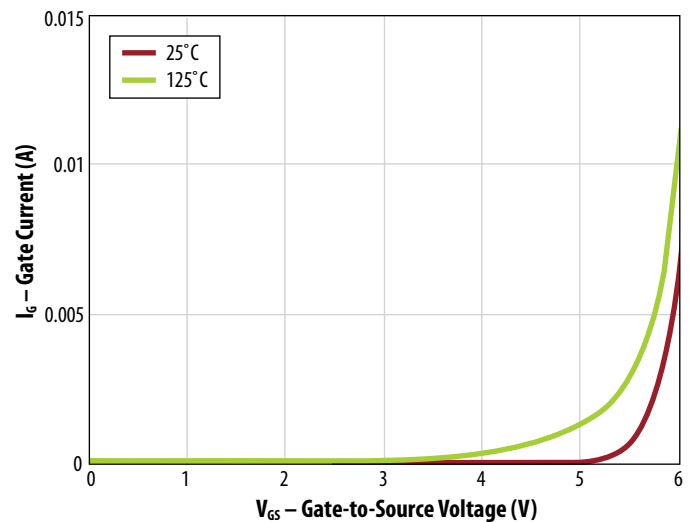


Figure 10: Gate Current



All measurements were done with substrate shorted to source.

Figure 11: Transient Thermal Response Curves

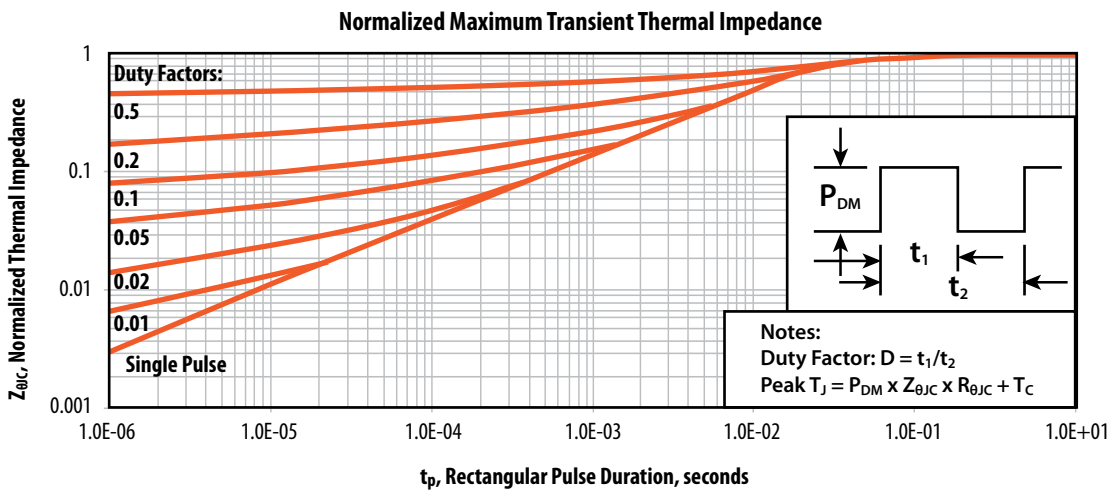
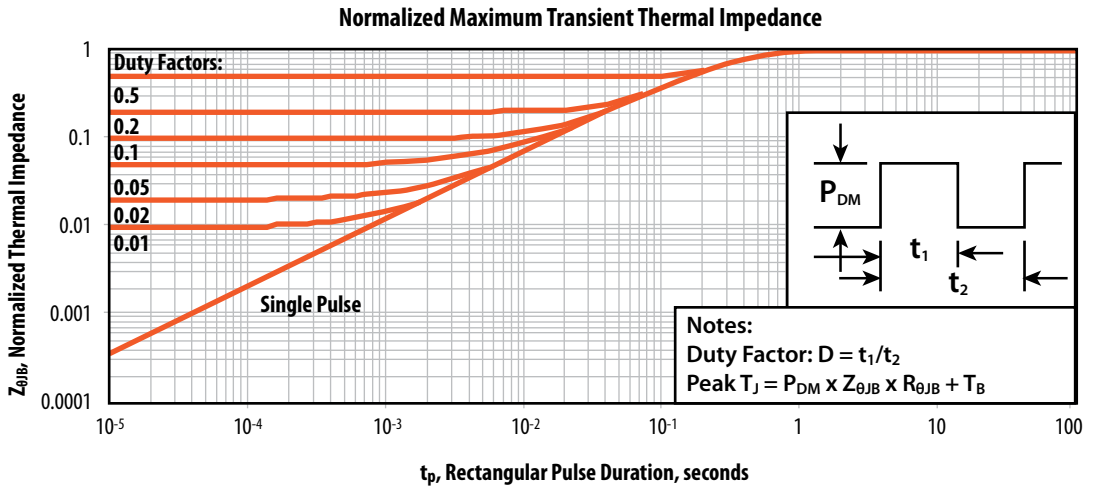
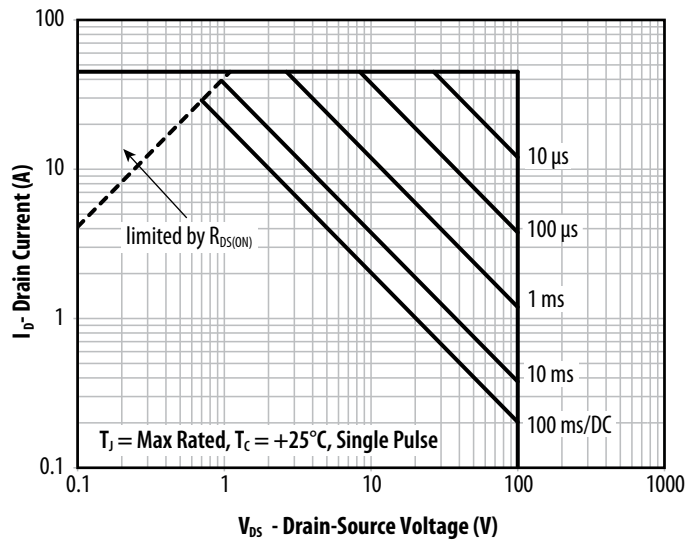
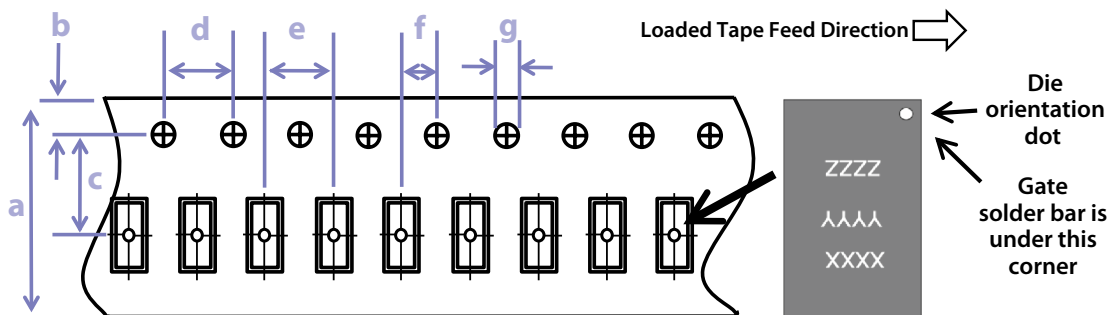
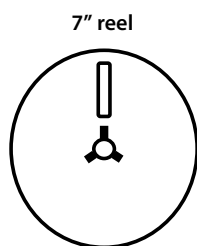


Figure 12: Safe Operating Area



**TAPE AND REEL CONFIGURATION**

4mm pitch, 8mm wide tape on 7" reel

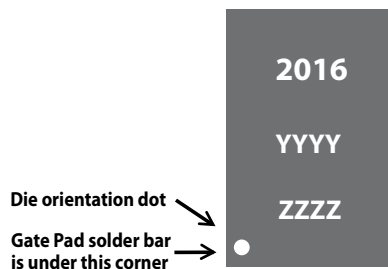


Dimension (mm)	EPC2016 (note 1)		
	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Die is placed into pocket solder bar side down (face side down)

Note 1: MSL1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.  
 Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

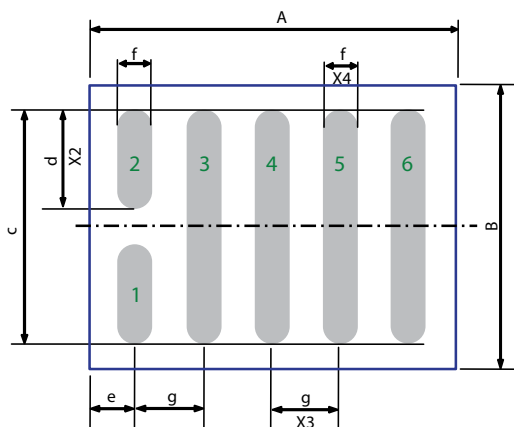
**DIE MARKINGS**



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC2016	2016	YYYY	ZZZZ

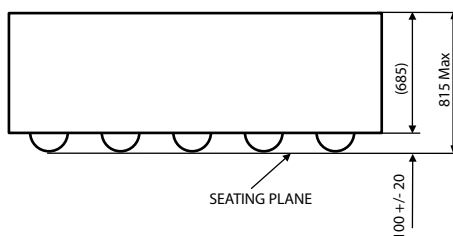
**DIE OUTLINE**

Solder Bar View



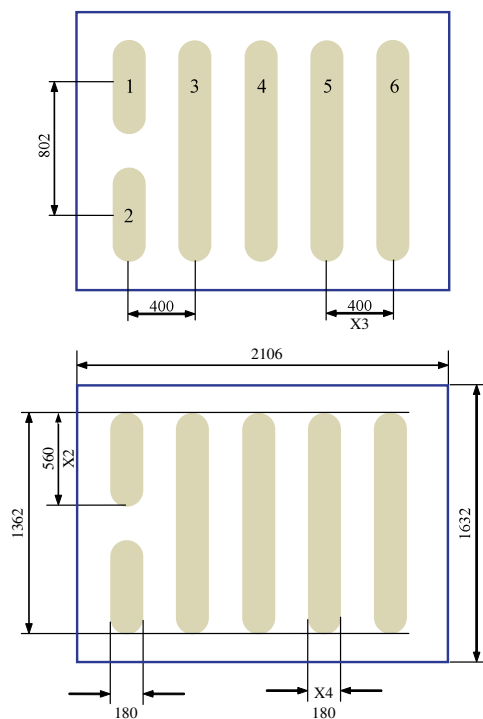
DIM	MICROMETERS		
	MIN	Nominal	MAX
A	2076	2106	2136
B	1602	1632	1662
c	1379	1382	1385
d	577	580	583
e	235	250	265
f	195	200	205
g	400	400	400

Side View



**RECOMMENDED  
LAND PATTERN**  
(units in  $\mu\text{m}$ )

The land pattern is solder mask defined.



Pad no. 1 is Gate;

Pads no. 3, 5 are Drain;

Pads no. 4, 6 are Source;

Pad no. 2 is Substrate.

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U.S. Patents 8,350,294; 8,404,508; 8,431,960; 8,436,398

Information subject to  
change without notice.  
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