

75A, 55V, 0.007 Ohm, N-Channel UltraFET Power MOSFETs



These N-Channel power MOSFETs are manufactured using the innovative UltraFET® process. This advanced process technology

achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA75345.

Ordering Information

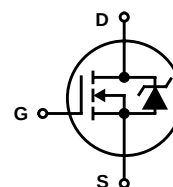
PART NUMBER	PACKAGE	BRAND
HUF75345G3	TO-247	75345G
HUF75345P3	TO-220AB	75345P
HUF75345S3S	TO-263AB	75345S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUF75345S3ST.

Features

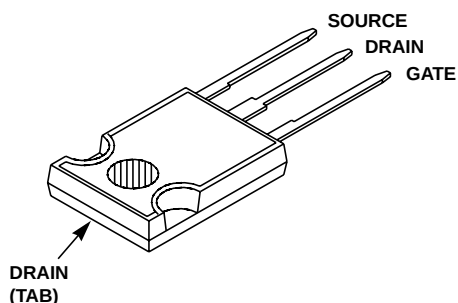
- 75A, 55V
- Simulation Models
 - Temperature Compensated PSPICE® and SABER™ Models
 - Thermal Impedance SPICE and SABER Models Available on the WEB at: www.intersil.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
 - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

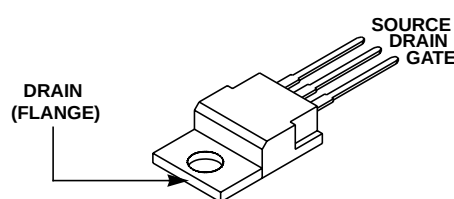


Packaging

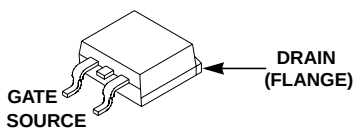
JEDEC STYLE TO-247



JEDEC TO-220AB



JEDEC TO-263AB



HUF75345G3, HUF75345P3, HUF75345S3S

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

			UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	55	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	V_{DGR}	55	V
Gate to Source Voltage	V_{GS}	± 20	V
Drain Current			
Continuous (Figure 2)	I_D	75	A
Pulsed Drain Current	I_{DM}	Figure 4	
Pulsed Avalanche Rating	E_{AS}	Figure 6	
Power Dissipation	P_D	325	W
Derate Above 25°C		2.17	W/ $^{\circ}\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	$^{\circ}\text{C}$
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	300	$^{\circ}\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	260	$^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 11)	55	-	-	V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 50V, V _{GS} = 0V	-	-	1	μA	
		V _{DS} = 45V, V _{GS} = 0V, T _C = 150 ⁰ C	-	-	250	μA	
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V	-	-	±100	nA	
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 10)	2	-	4	V	
Drain to Source On Resistance	r _{DS(ON)}	I _D = 75A, V _{GS} = 10V (Figure 9)	-	0.006	0.007	W	
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	R _{θJC}	(Figure 3)	-	-	0.46	⁰ C/W	
Thermal Resistance Junction to Ambient	R _{θJA}	TO-247	-	-	30	⁰ C/W	
		TO-220, TO-263	-	-	62	⁰ C/W	
SWITCHING SPECIFICATIONS (V _{GS} = 10V)							
Turn-On Time	t _{ON}	V _{DD} = 30V, I _D ≅ 75A, R _L = 0.4Ω, V _{GS} = 10V, R _{GS} = 2.5Ω	-	-	145	ns	
Turn-On Delay Time	t _{d(ON)}		-	20	-	ns	
Rise Time	t _r		-	75	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	45	-	ns	
Fall Time	t _f		-	30	-	ns	
Turn-Off Time	t _{OFF}		-	-	115	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 20V	V _{DD} = 30V, I _D ≅ 75A, R _L = 0.4Ω I _{g(REF)} = 1.0mA (Figure 13)	-	220	275	nC
Gate Charge at 10V	Q _{g(10)}	V _{GS} = 0V to 10V		-	125	165	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 2V		-	6.8	10	nC
Gate to Source Gate Charge	Q _{gs}			-	14	-	nC
Gate to Drain “Miller” Charge	Q _{ad}			-	58	-	nC

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CAPACITANCE SPECIFICATIONS						
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$ (Figure 12)	-	4000	-	pF
Output Capacitance	C_{OSS}		-	1450	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	450	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 75\text{A}$	-	-	1.25	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 75\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	110	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 75\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	225	nC

Typical Performance Curves

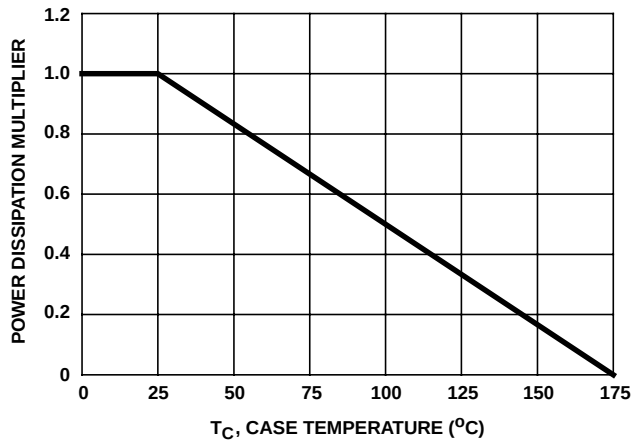


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

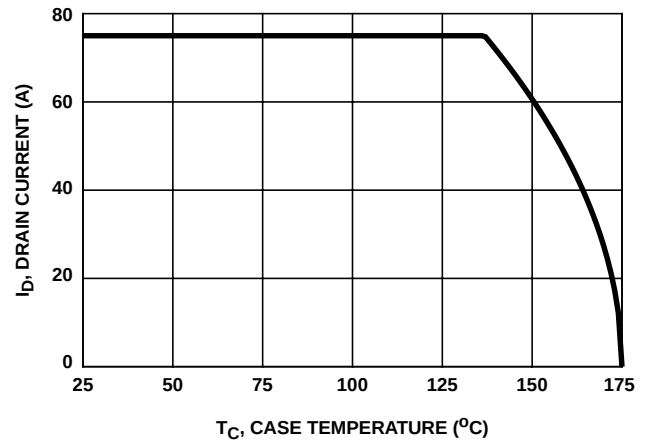


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

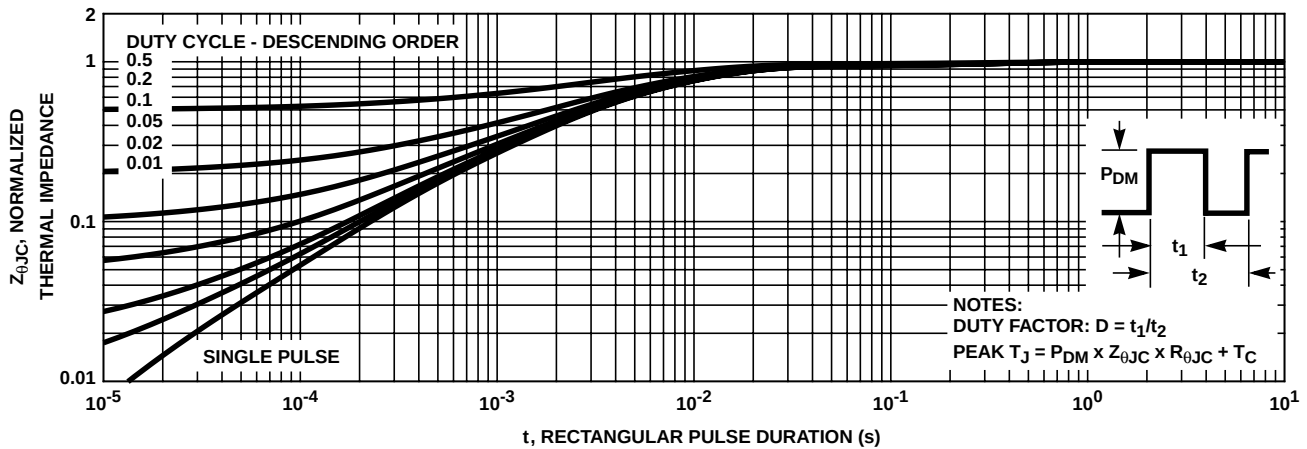


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves (Continued)

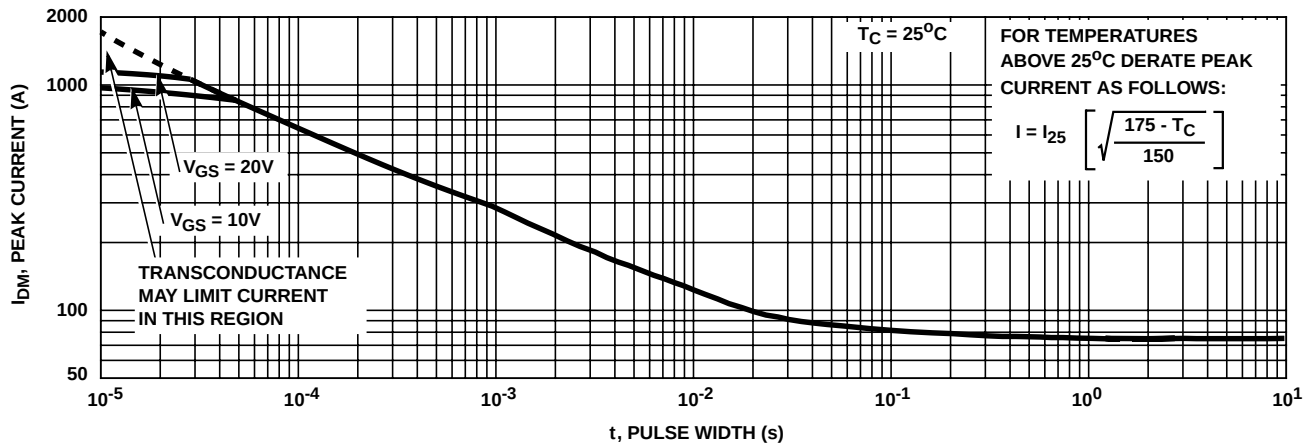


FIGURE 4. PEAK CURRENT CAPABILITY

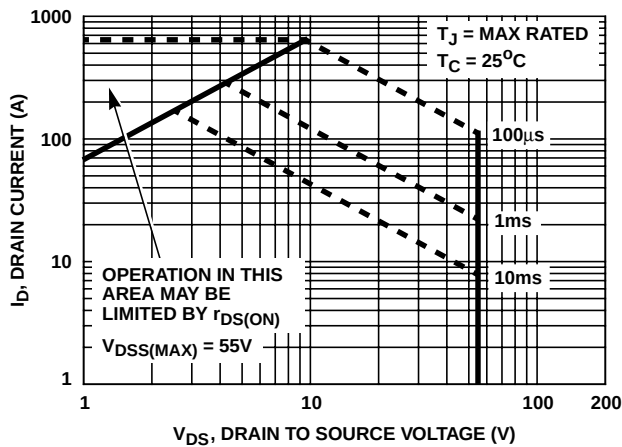
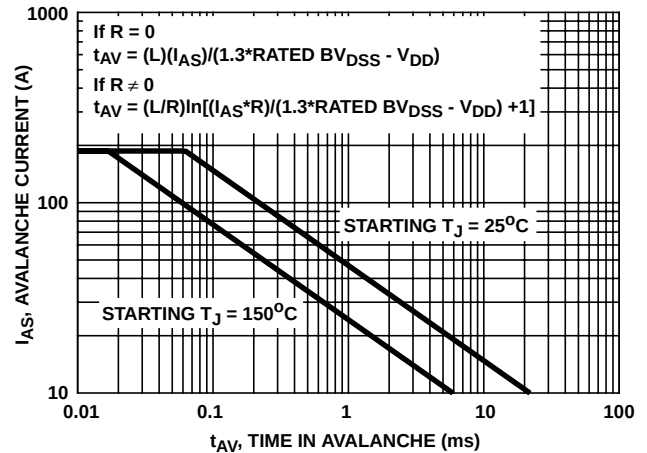


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

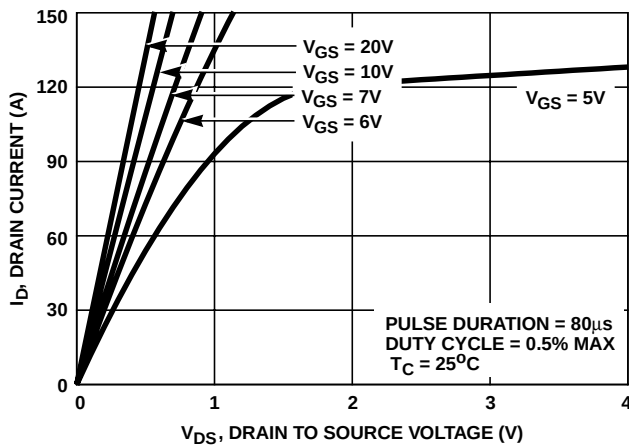


FIGURE 7. SATURATION CHARACTERISTICS

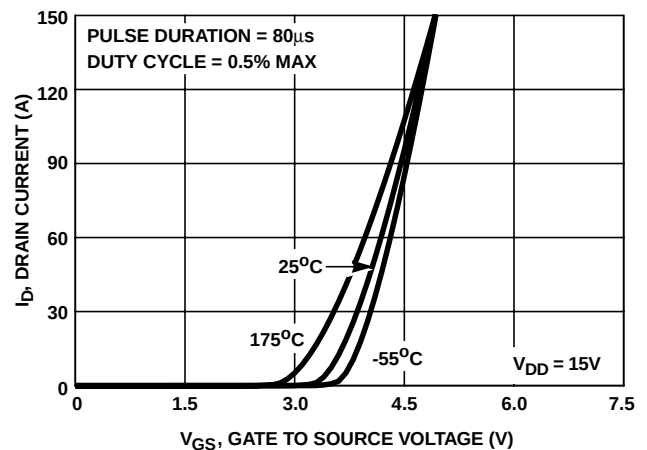


FIGURE 8. TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

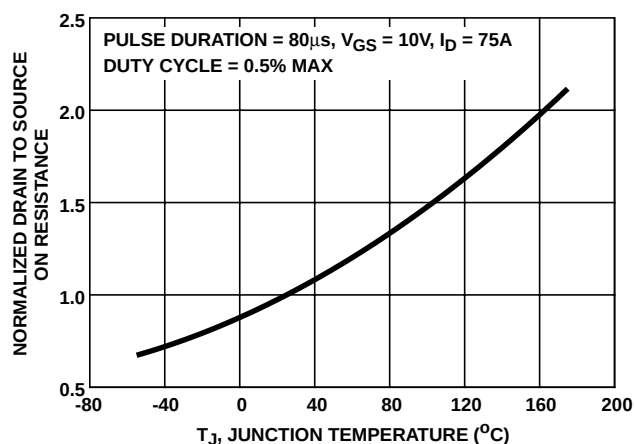


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

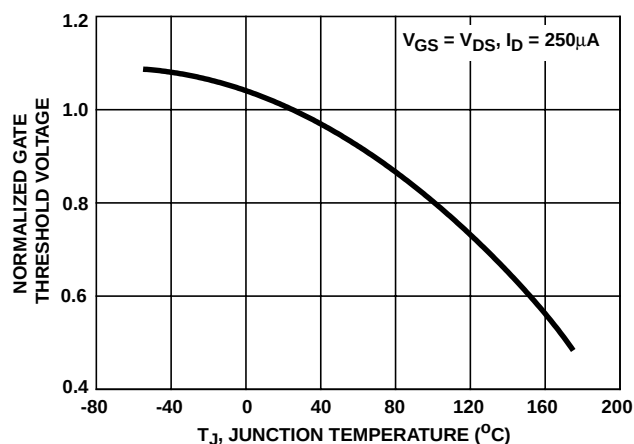


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

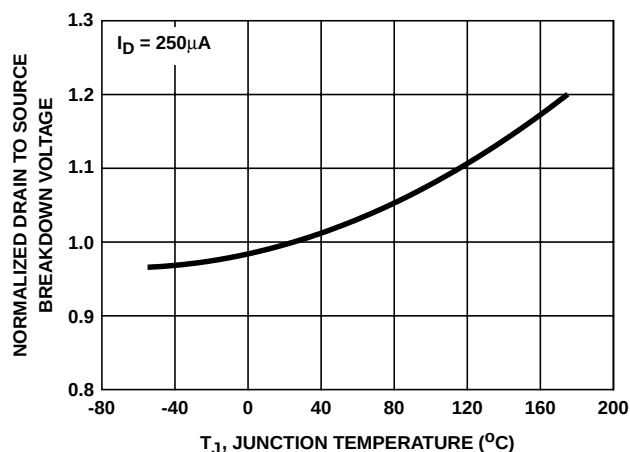


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

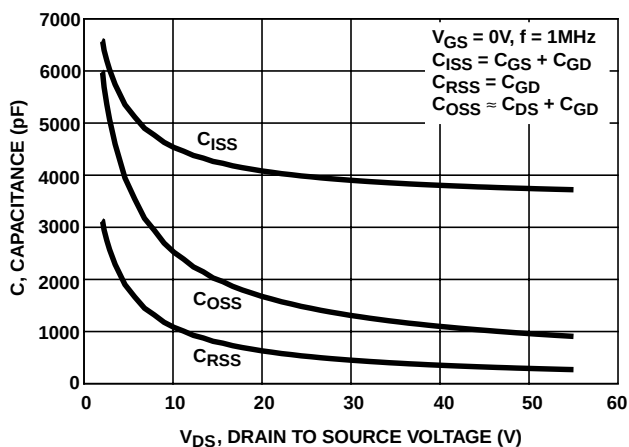
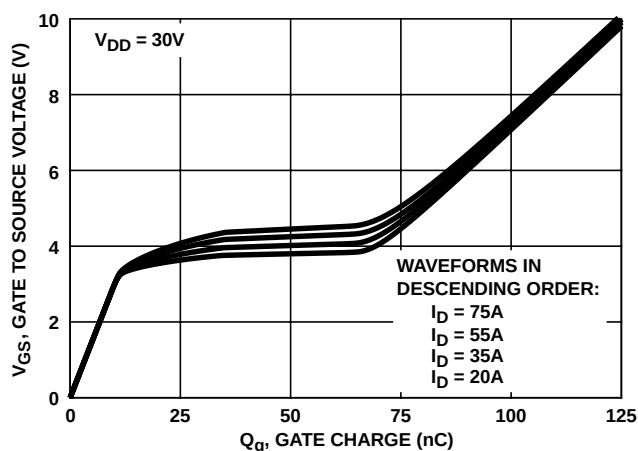


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

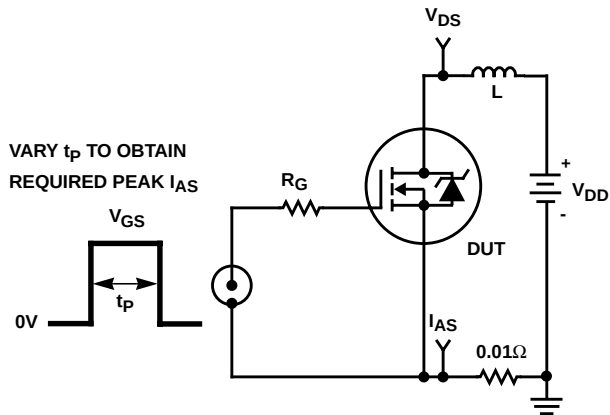


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

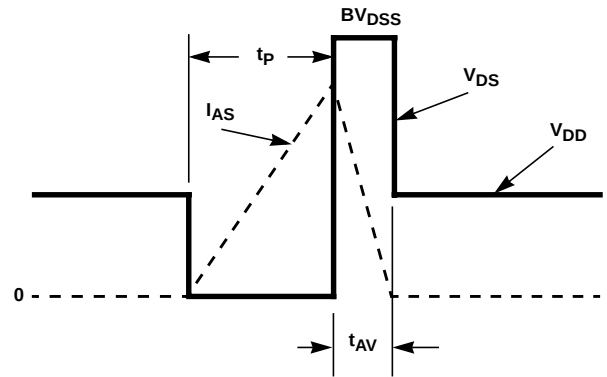


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

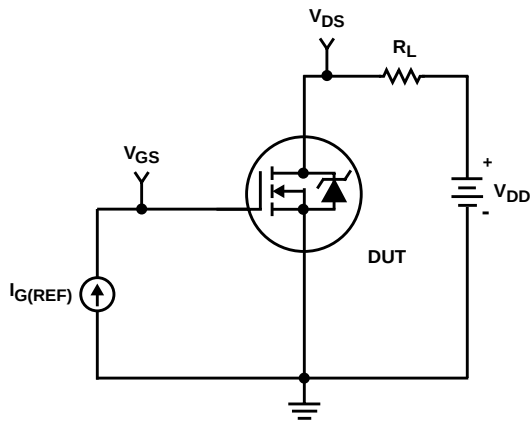


FIGURE 16. GATE CHARGE TEST CIRCUIT

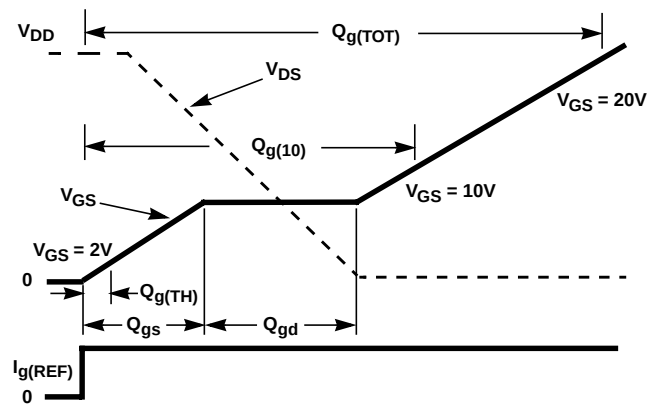


FIGURE 17. GATE CHARGE WAVEFORM

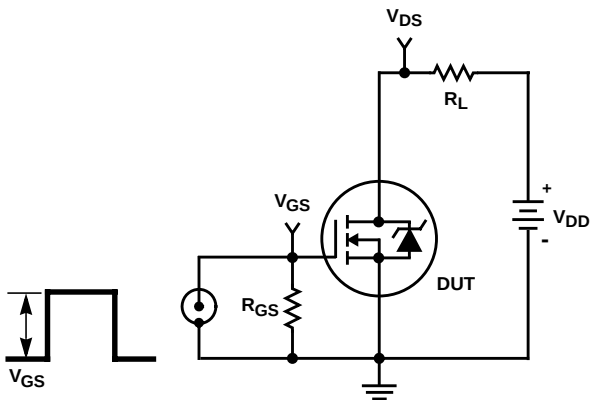


FIGURE 18. SWITCHING TIME TEST CIRCUIT

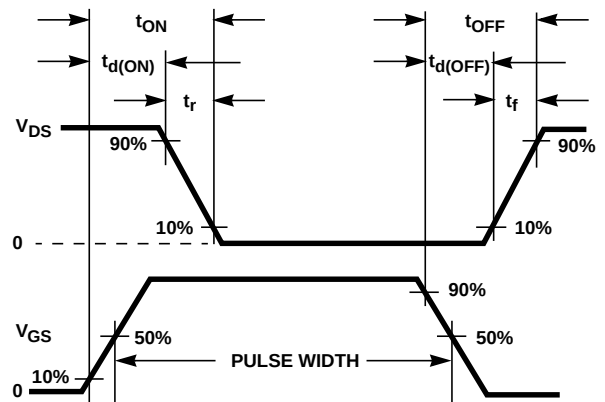


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

PSPICE Electrical Model

.SUBCKT HUF75345 2 1 3 ; rev 3 Feb 99

CA 12 8 5.55e-9
CB 15 14 5.55e-9
CIN 6 8 3.45e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 56.7
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 2.6e-9
LSOURCE 3 7 1.1e-9
KGATE LSOURCE LGATE 0.0085

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 1e-4
RGATE 9 20 0.36
RLDRAIN 2 5 10
RLGATE 1 9 26
RLSOURCE 3 7 11
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 3.15e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

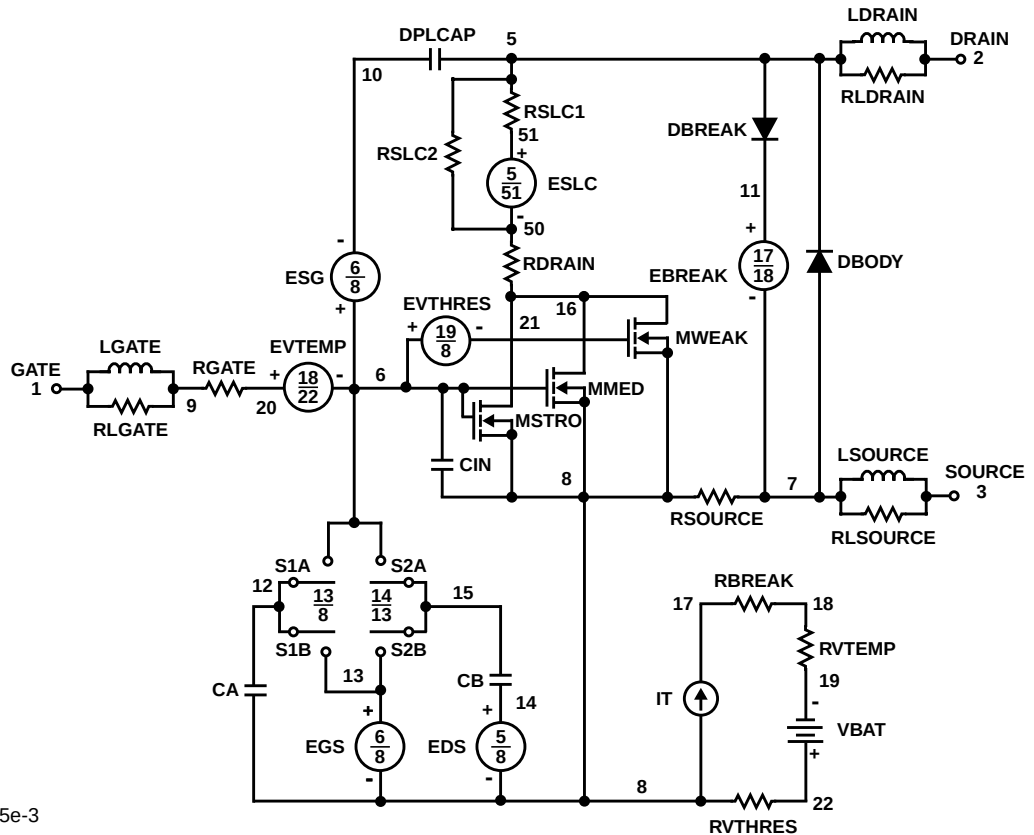
ESLC 51 50 VALUE={ (V(5,51)/ABS(V(5,51))) * (PWR(V(5,51)/(1e-6*500),3.5)) }

.MODEL DBODYMOD D (IS = 6e-12 RS = 1.4e-3 IKF = 20 XTI = 5 TRS1 = 2.75e-3 TRS2 = 5.0e-6 CJO = 5.5e-9 TT = 5.9e-8 M = 0.5 VJ = 0.75)
.MODEL DBREAKMOD D (RS = 2.8e-2 IKF = 30 TRS1 = -4.0e-3 TRS2 = 1.0e-6)
.MODEL DPLCAPMOD D (CJO = 6.75e-9 IS = 1e-30 M = 0.88 VJ = 1.45 FC = 0.5)
.MODEL MMEDMOD NMOS (VTO = 2.93 KP = 13.75 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 0.36)
.MODEL MSTROMOD NMOS (VTO = 3.23 KP = 96 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u Lambda = 0.06)
.MODEL MWEAKMOD NMOS (VTO = 2.35 KP = 0.02 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 3.6)
.MODEL RBREAKMOD RES (TC1 = 8.0e-4 TC2 = 4.0e-6)
.MODEL RDRAINMOD RES (TC1 = 1.5e-1 TC2 = 6.5e-4)
.MODEL RSLCMOD RES (TC1 = 1.0e-4 TC2 = 1.05e-6)
.MODEL RSOURCEMOD RES (TC1 = 1.0e-3 TC2 = 0)
.MODEL RVTHRESMOD RES (TC1 = -1.5e-3 TC2 = -2.6e-5)
.MODEL RVTEMPMOD RES (TC1 = -2.75e-3 TC2 = 1.45e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -9.00 VOFF = -4.00)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.00 VOFF = -9.00)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.00 VOFF = 0.50)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.50 VOFF = 0.00)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SPICE Thermal Model

REV 5 February 1999

HUF75345

CTHERM1 th 6 6.3e-3
CTHERM2 6 5 1.5e-2
CTHERM3 5 4 2.0e-2
CTHERM4 4 3 3.0e-2
CTHERM5 3 2 8.0e-2
CTHERM6 2 tl 1.5e-1

RTHERM1 th 6 5.0e-3
RTHERM2 6 5 1.8e-2
RTHERM3 5 4 5.0e-2
RTHERM4 4 3 8.5e-2
RTHERM5 3 2 1.0e-1
RTHERM6 2 tl 1.1e-1

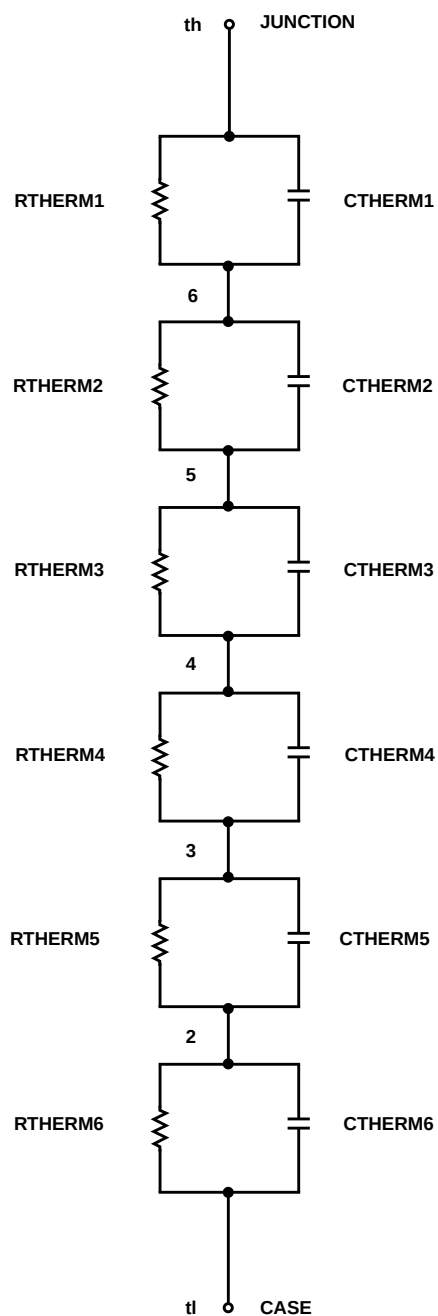
SABER Thermal Model

SABER thermal model HUF75345

template thermal_model th tl
thermal_c th, tl

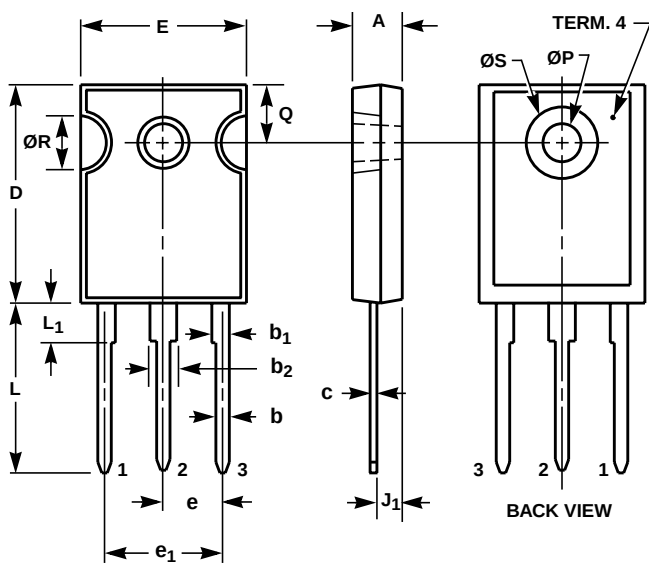
```
{
ctherm.ctherm1 th 6 = 6.3e-3
ctherm.ctherm2 6 5 = 1.5e-2
ctherm.ctherm3 5 4 = 2.0e-2
ctherm.ctherm4 4 3 = 3.0e-2
ctherm.ctherm5 3 2 = 8.0e-2
ctherm.ctherm6 2 tl = 1.5e-1
```

```
rtherm.rtherm1 th 6 = 5.0e-3
rtherm.rtherm2 6 5 = 1.8e-2
rtherm.rtherm3 5 4 = 5.0e-2
rtherm.rtherm4 4 3 = 8.5e-2
rtherm.rtherm5 3 2 = 1.0e-1
rtherm.rtherm6 2 tl = 1.1e-1
}
```



TO-247

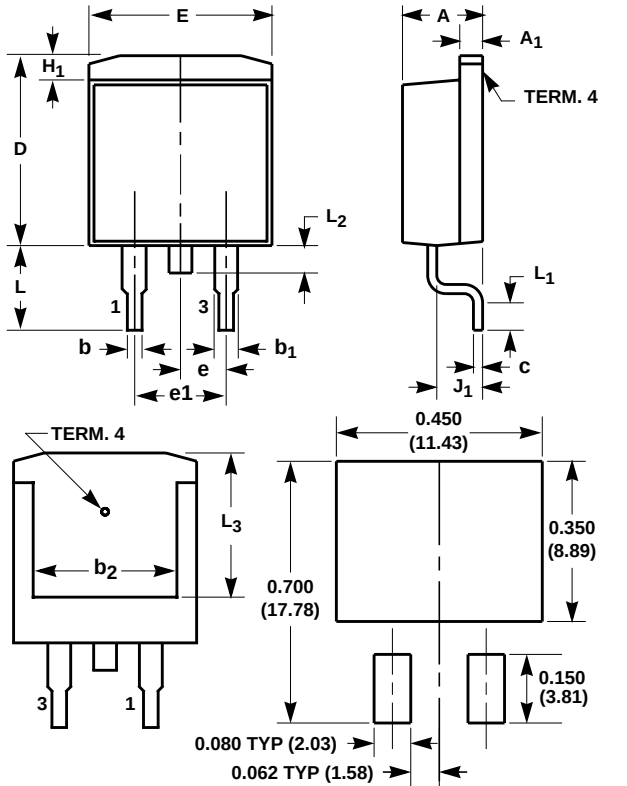
3 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b ₁	0.060	0.070	1.53	1.77	1, 2
b ₂	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.219 TYP		5.56 TYP		4
e ₁	0.438 BSC		11.12 BSC		4
J ₁	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L ₁	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L₁.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

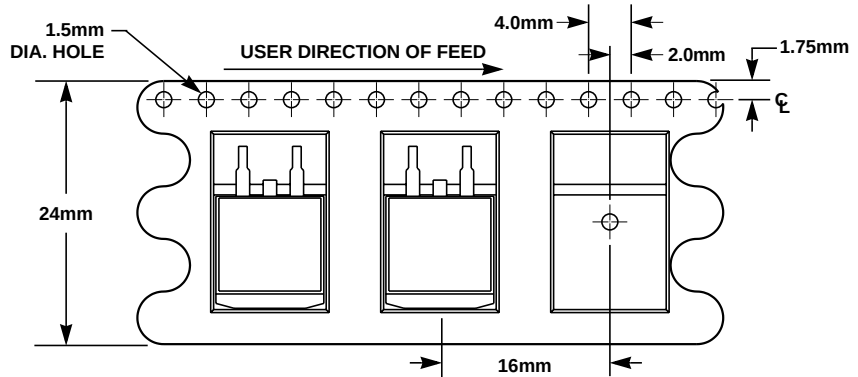
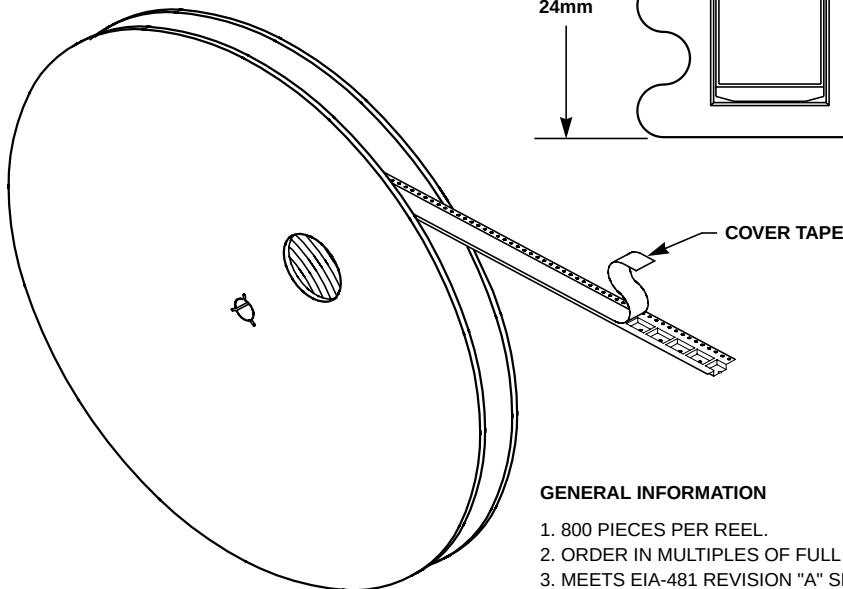
TO-263AB SURFACE MOUNT JEDEC TO-263AB PLASTIC PACKAGE


MINIMUM PAD SIZE RECOMMENDED FOR
SURFACE-MOUNTED APPLICATIONS

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	4, 5
b	0.030	0.034	0.77	0.86	4, 5
b ₁	0.045	0.055	1.15	1.39	4, 5
b ₂	0.310	-	7.88	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		7
e ₁	0.200 BSC		5.08 BSC		7
H ₁	0.045	0.055	1.15	1.39	-
J ₁	0.095	0.105	2.42	2.66	-
L	0.175	0.195	4.45	4.95	-
L ₁	0.090	0.110	2.29	2.79	4, 6
L ₂	0.050	0.070	1.27	1.77	3
L ₃	0.315	-	8.01	-	2

NOTES:

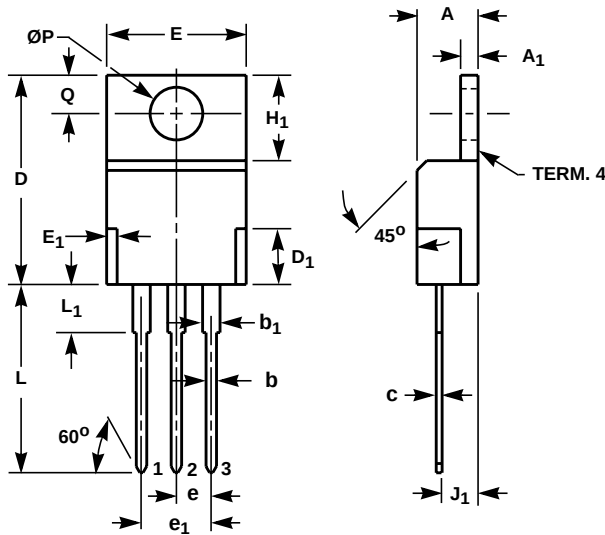
1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
2. L₃ and b₂ dimensions established a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L₁ is the terminal length for soldering.
7. Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 10 dated 5-99.

TO-263AB
24mm TAPE AND REEL

GENERAL INFORMATION

1. 800 PIECES PER REEL.
2. ORDER IN MULTIPLES OF FULL REELS ONLY.
3. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

TO-220AB

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b ₁	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D ₁	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E ₁	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e ₁	0.200 BSC		5.08 BSC		5
H ₁	0.235	0.255	5.97	6.47	-
J ₁	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L ₁	0.130	0.150	3.31	3.81	2
$\varnothing P$	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L₁.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 7-97.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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