WM8961-6208-FL32-M

Example Configurations

DOC TYPE:	EXAMPLE CONFIGURATIONS
BOARD REFERENCE:	6208-EV1 and WM8961-6208-FL32-M-REV1
BOARD TYPE:	Customer Main and Mini Board
WOLFSON DEVICE(S):	WM8961
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INTRODUCTION

The WM8961 is an ultra-low power stereo CODEC with 1W stereo class D speaker drivers and ground referenced headphone drivers. The device operates in slave mode and can be controlled by a software 2-wire interface. The WM8961 is provided on a MINI board (WM8961-6208-FL32-M-REV1) which connects to the 6208-EV1-REV1 MAIN board. This forms what will be referred to as the WM8961 evaluation board.

The WM8961 customer evaluation board provides full functionality for the evaluation of the WM8961 device.

The purpose of this document is to detail common configurations for evaluation board operation. Contained in this document are:

- Register settings for internal configuration of the WM8961 device.
- Details on evaluation board setup and configuration.

This document can be used as a base line for evaluation board configuration when beginning to use the WM8961 customer evaluation board. Please note that all register settings supplied in this document are suitable to setup the required path but may not be optimised for quiet power up or other considerations that will be necessary for any end application. Please consult the latest datasheet for information on such considerations.

Software to configure the evaluation board is available from your local Wolfson representative, or can be downloaded from http://www.wolfsonmicro.com/support/drivers

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TERMINOLOGY

AIF	Audio Interface
USB	Universal Serial Bus
EVB	Evaluation Board
MCU	Microprocessor Control Unit
S/PDIF	Sony / Philips Digital Interface Format

DEFAULT JUMPER SETTINGS

The WM8961 customer evaluation board should be received with the jumper settings as shown in Figure 1.

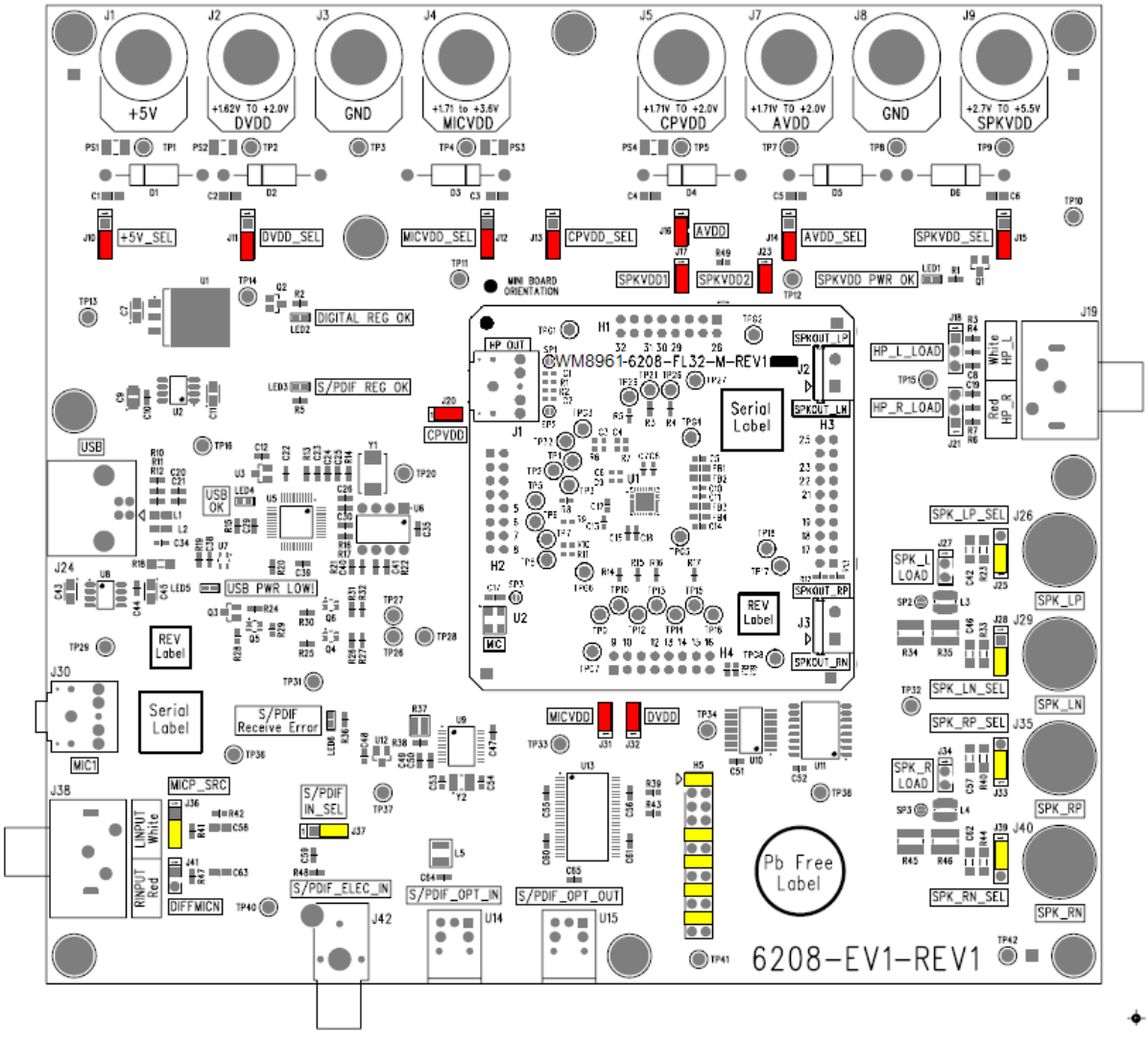

Figure 1 Default Jumper Settings

EXAMPLE CONFIGURATIONS

The following example configurations are independent of whether power is applied to the board from external power supplies or from the USB interface.

DAC TO HEADPHONE PLAYBACK (0DB VOLUME SETTING)

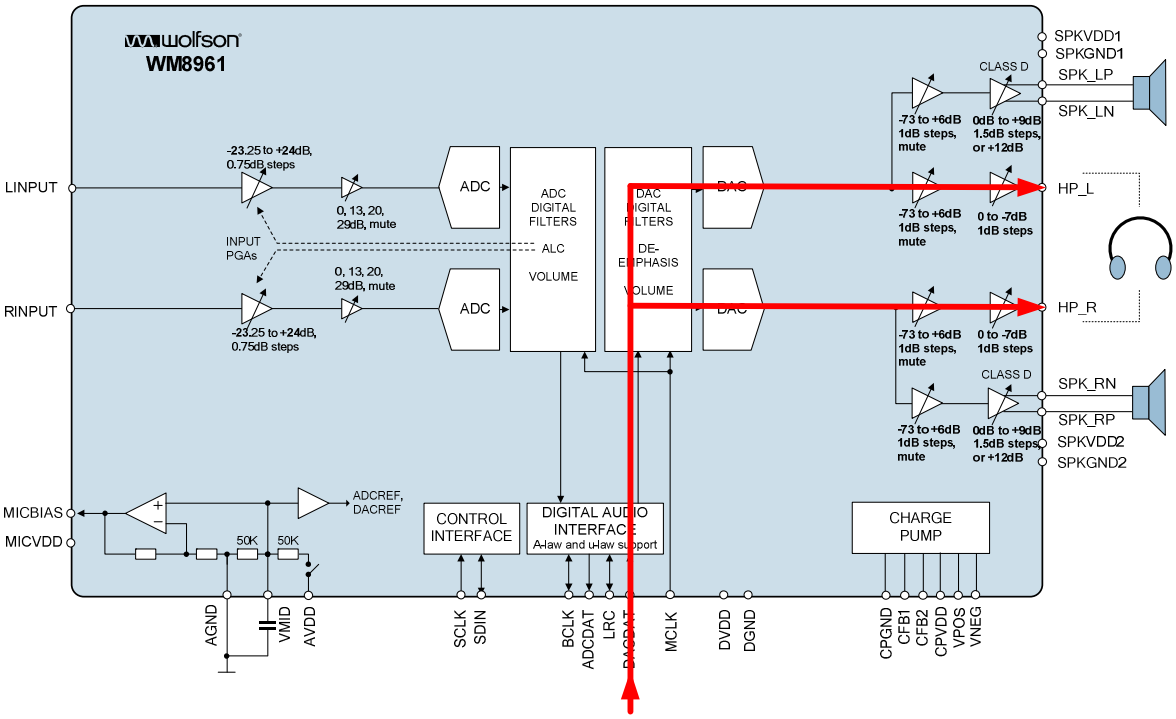

Figure 2 WM8961 Block Diagram for DAC to Headphone Playback

The configuration is as follows:-

- Powered and programmed from the USB interface.
- Clocks and DAC digital input data supplied from S/PDIF electrical input.
- AIF format (DIN and DOUT) = 24 bit I2S through S/PDIF Analogue headphone output

To configure this path, the external jumpers should be set as shown in Table 7. The jumpers, input signals and output signals are shown in Figure 10 in the “Jumper settings” section.

This configuration uses the control write interface and the registers programmed are given in Table 8.

JUMPERS	JUMPER STATUS	DESCRIPTION
J37	1 – 2	**S/PDIF_IN_SEL** Select the S/PDIF electrical input.
H5	1-2 9-10 13-14 17-18 21-22	**AIF Interface** These links needed for connection to external clock source and Digital Din derived from the S/PDIF interface.
J18,J21	1 - 2	**Headphone Load** Select 32R load
J10	2 - 3	**USB power supply selected for all supplies**

Table 1 Jumper Settings for DAC to Headphone Playback

The jumpers, input signals and output signals are shown in Figure 10 in the “Jumper settings” section.

REGISTER	SETTING	COMMENT
0x0F - write	0x0000	Reset device if required
0x0F - read	-	Read Chip ID (=0x1801)
0x08 - write	0x01F4	Enable system clocks
0x57 - write	0x0020	Enable the write sequencer, DAC to headphone playback with -20dB volume setting
0x5A - write	0x0080	Start the write sequencer to configure pre-programmed enable of the DAC playback (digital input to headphone output) path. Analogue input PGAs still muted.
Allow enough time for the sequencer to finish		
0x5D - read	-	Read status of write sequencer and wait until the WSEQ_BUSY,bit0,=0 which indicates that the DAC playback path has been configured. Then continue.
0x02 - write	0x0079	Set the left headphone volume to 0dB
0x03 - write	0x0179	Set the right headphone volume to 0dB and update headphone volume OUT1VU

Table 2 Register Settings for DAC to Headphone Playback (0dB volume setting)

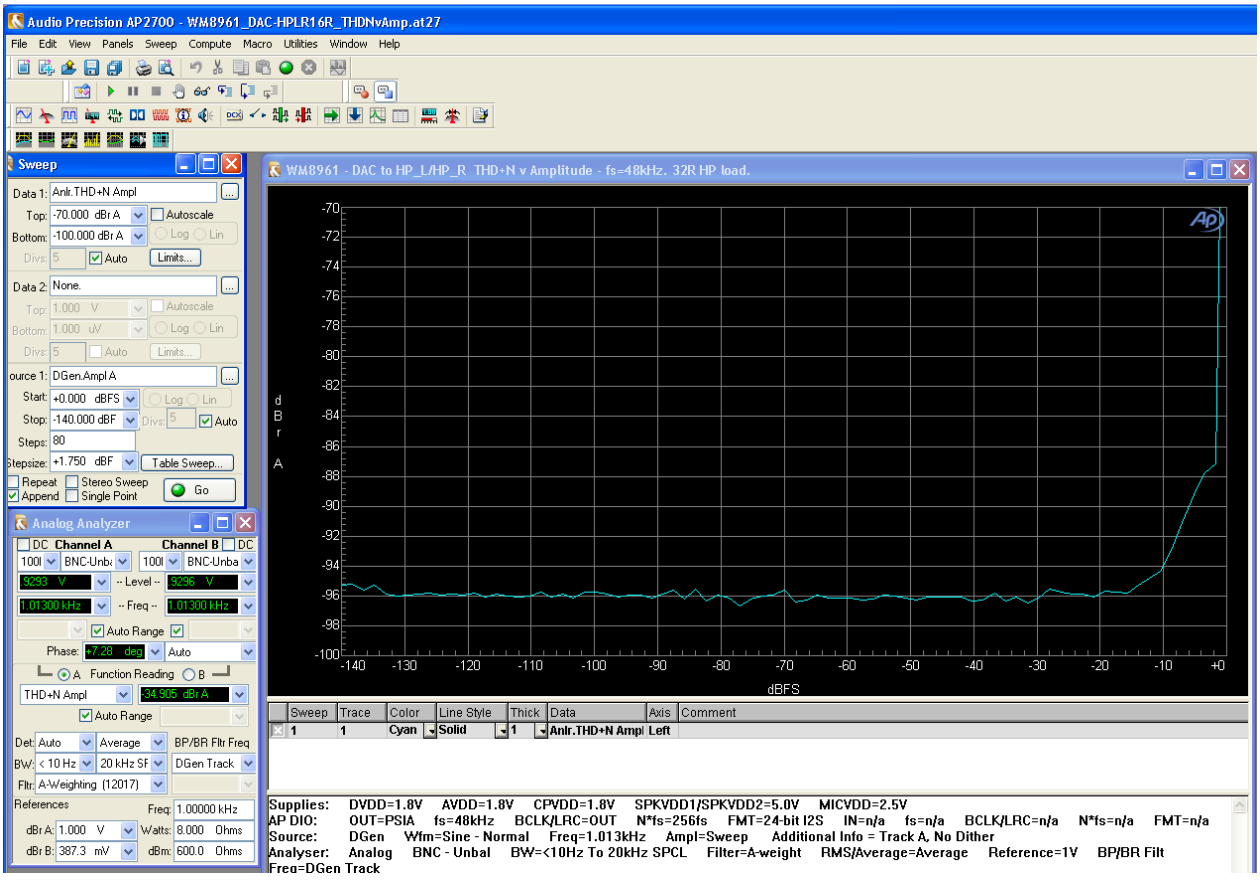

Figure 3 WM8961 Performance Plot for DAC to Headphone Playback (0dB volume setting, 32R load)

DAC TO SPEAKER AND HEADPHONE PLAYBACK

Note: In order to simplify the configuration of DAC to speaker playback, the headphone output should first be enabled.

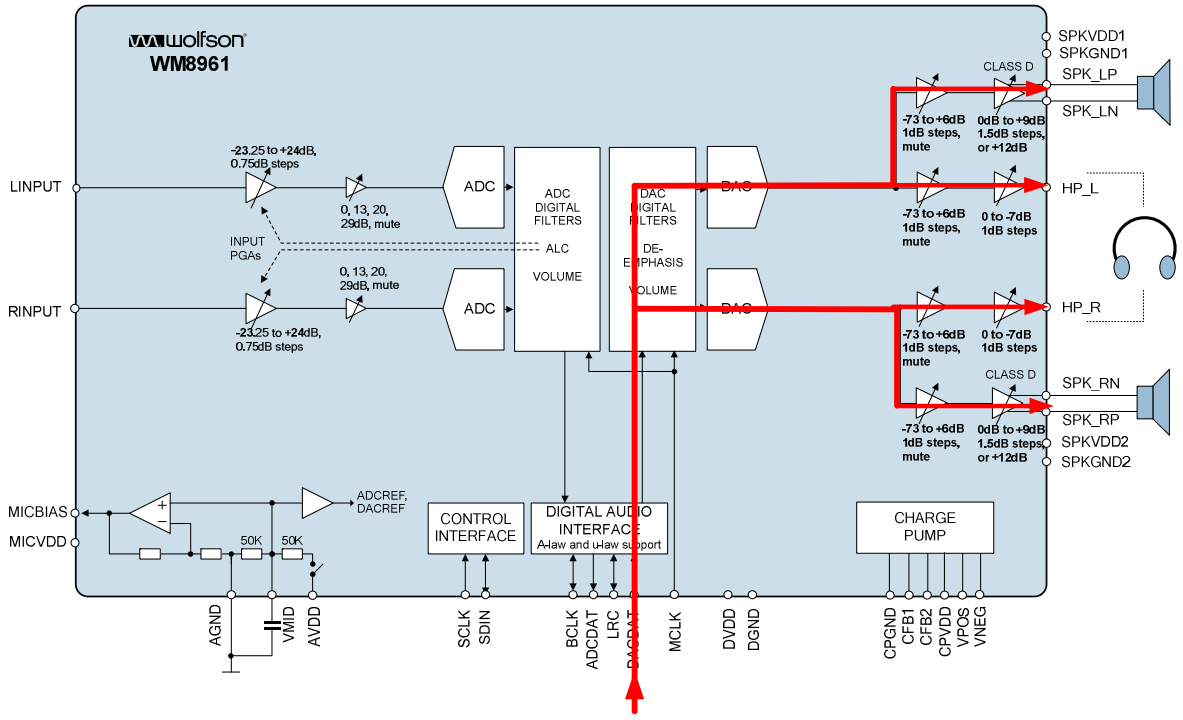

Figure 4 WM8961 Block Diagram for DAC to Speaker and Headphone Playback

The example configuration is as follows:-

- Configured from the USB interface.
- SPKVDD powered from external +5V. This is recommended since typical USB power supplies are not capable of providing enough current for full speaker performance
- All other supplies powered from USB
- Clocks and DAC digital input data supplied via H5.
- AIF format DACDAT IN = 24 bit I2S
- Analogue speaker outputs
- Class D speaker outputs with on board 8.2Ω load.

To configure this path, the external jumpers should be set as shown in Table 3. The jumpers, input signals and output signals are shown in Figure 11 in the “Jumper settings” section. This configuration uses the registers programmed as given in Table 4.

JUMPERS	JUMPER STATUS	DESCRIPTION
J15	1 – 2	**SPKVDD external supply**
J8-J9	Apply external SPKVDD	2.7-5.5v
J10	2 - 3	**USB power supply selected for all other supplies**
J25 J27	1 – 2 Link fitted	**SPK_LP_SEL** Left channel positive analogue output on J26 with 8.2Ω load and no filter.
J28	1 – 2	**SPK_LN_SEL** Left channel negative analogue output on J29 with 8.2Ω load and no filter.
J33 J34	1 – 2 Link fitted	**SPK_RP_SEL** Right channel positive analogue output on J35 with 8.2Ω load and no filter.
J39	1 – 2	**SPK_RN_SEL** Right channel negative analogue output on J40 with 8.2Ω load and no filter.
H5	1-2 9-10 13-14 17-18 21-22	**AIF Interface** These links needed for connection to external clock source and Digital Din derived from the S/PDIF interface.

Table 3 Jumper Settings for DAC to Speaker and Headphone Playback

REGISTER	SETTING	COMMENT
0x0F - write	0x0000	Reset device if required
0x0F - read	-	Read Chip ID (=0x1801)
0x08 - write	0x01F4	Enable system clocks
0x57 - write	0x0020	Enable the write sequencer, DAC to headphone playback with -20dB volume setting.
0x5A - write	0x0080	Start the write sequencer to configure pre-programmed enable of the DAC playback (digital input to headphone output) path. Analogue input PGAs still muted.
Allow enough time for the sequencer to finish		
0x5D - read	-	Read status of write sequencer and wait until the WSEQ_BUSY,bit0,=0 which indicates that the DAC playback path has been configured. Then continue.
0x1A - write	0x01FC	Enable the Speaker PGAs, SPKL_PGA and SPKR_PGA
0x33 - write	0x0001	Program the CLASSD_ACGAIN to x1.5
0x31 - write	0x00C0	Enable the speakers SPKR_ENA and SPKL_ENA
0x28 - write	0x0079	Set the left speaker volume SPKLVOL to 0dB (which defaults to mute), change on zero cross only
0x29 - write	0x0079	Set the right speaker volume SPKRVOL to 0dB (which defaults to mute), change on zero cross only
0x29 - write	0x0179	Update speaker volume SPKVU

Table 4 Register Settings for DAC to Speaker and Headphone Outputs

The above configuration enables the speaker and the headphone outputs.

SWITCHING BETWEEN HEADPHONE AND SPEAKERS

With DAC to speaker and headphone playback enabled, switching between headphone and speaker outputs should be done using the PGA and mute bits as shown in Table 5 and Table 6. This achieves best pop-click performance.

To save power, it may also be desirable to apply power management settings in addition to the settings shown, however note that disabled PGAs leave a resistive path hence do not achieve the published mute attenuation specifications.

0x02 - write	0x012F	Headphone L mute
0x03 - write	0x012F	Headphone R mute
0x28 - write	0x0079	Set the left speaker volume SPKRVOL to 0dB
0x29 - write	0x0179	Set the right speaker volume to 0dB and update speaker volume SPKVU

Table 5 Switching from Headphone playback to Speaker Playback

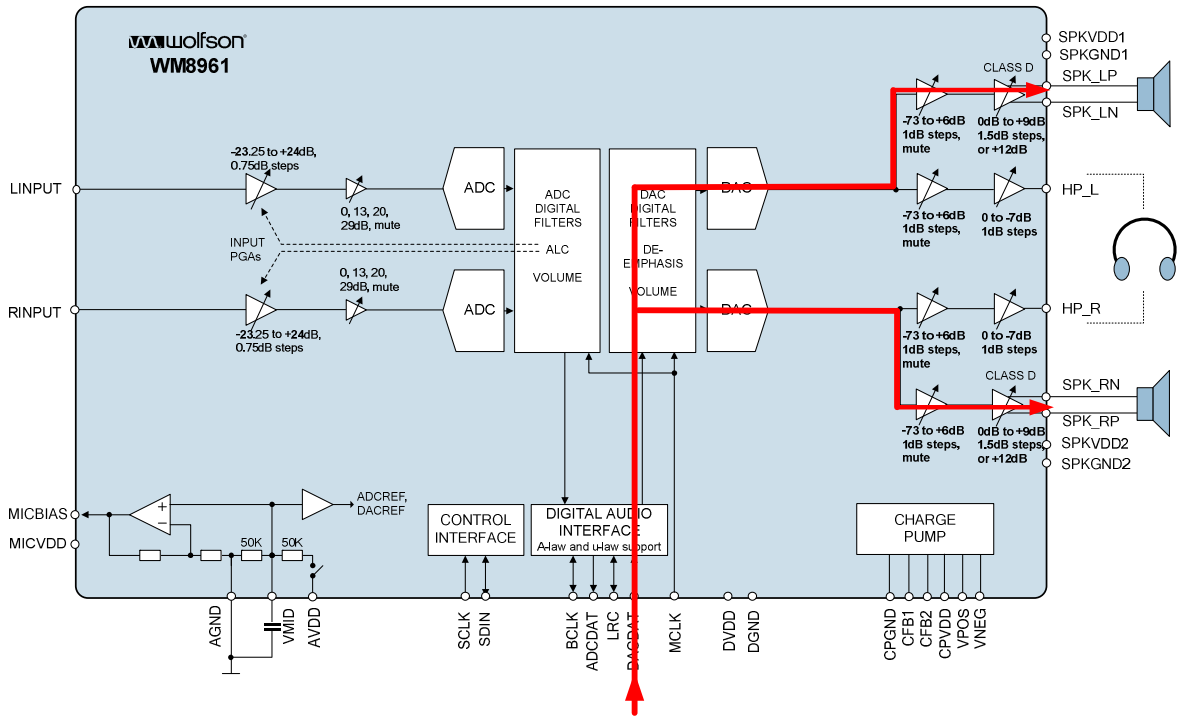

Figure 5 WM8961 Block Diagram for DAC to Speaker Playback

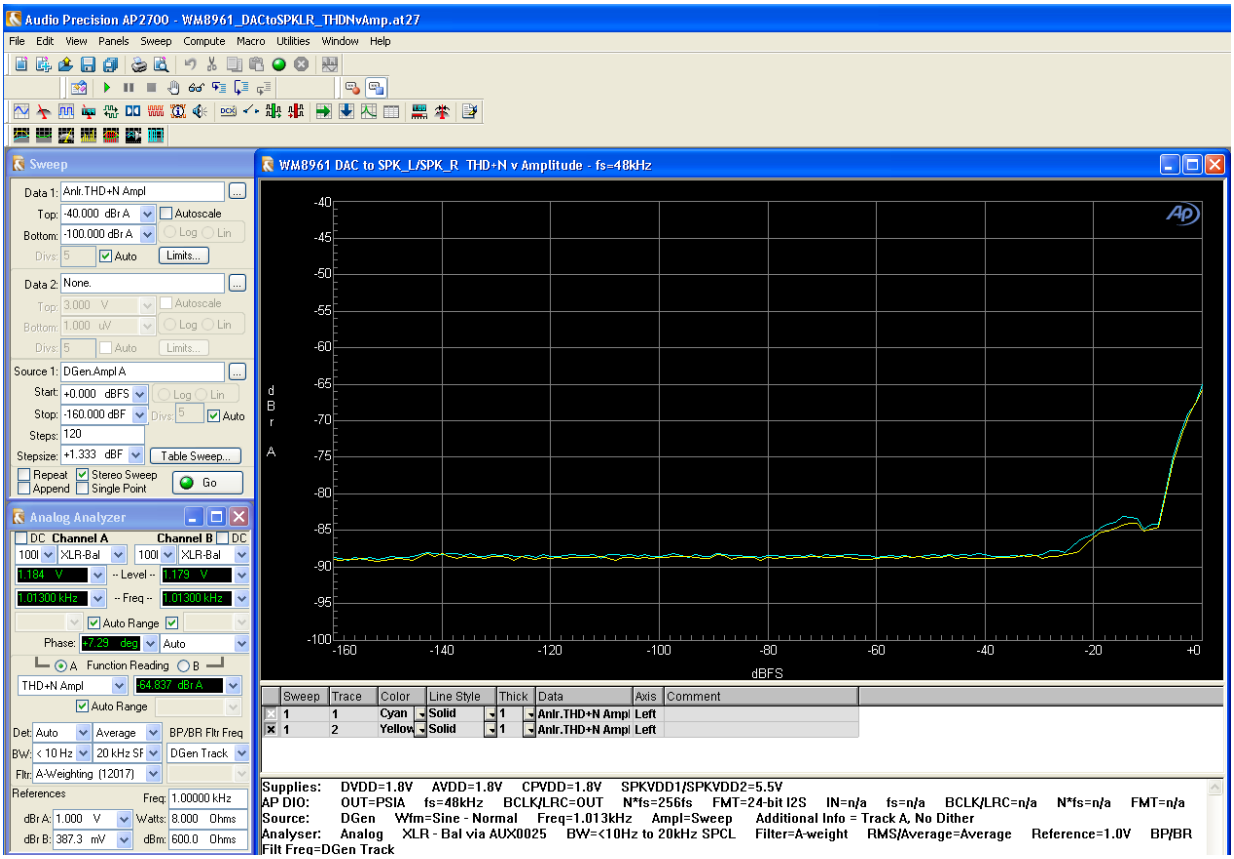

Figure 6 WM8961 Performance Plot for DAC to Speaker Playback

REGISTER	SETTING	COMMENT
0x02 - write	0x0079	Set the left headphone volume to 0dB
0x03 - write	0x0179	Set the right headphone volume to 0dB and update headphone volume OUT1VU
0x28 - write	0x002F	Speaker L mute
0x29 - write	0x012F	Speaker R mute

Table 6 Switching from Speaker Playback to Headphone Playback (0dB volume setting)

LRINPUT TO ADC RECORD

Note: In order to simplify the configuration of LRINPUT to ADC recording, the headphone output should first be enabled.

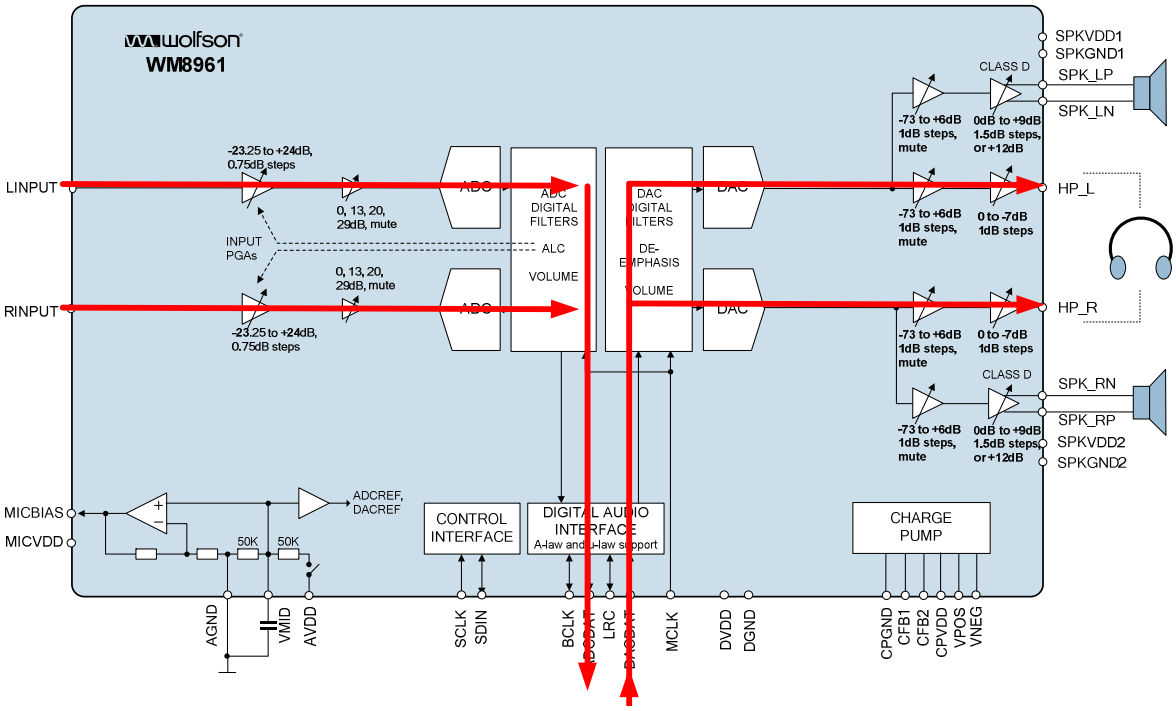

Figure 7 WM8961 Block Diagram for LRINPUT to ADC Record

The configuration is as follows:-

- Powered and programmed from the USB interface.
- Clocks and DAC digital input data supplied from S/PDIF electrical input.
- Digital output data through S/PDIF output.
- AIF format (DIN and DOUT) = 24 bit I2S through S/PDIF
- Analogue Line input
- Analogue headphone output

To configure this path, the external jumpers should be set as shown in Table 7. The jumpers, input signals and output signals are shown in Figure 10 in the “Jumper settings” section. This configuration uses the control write interface and the registers programmed are given in Table 8.

JUMPERS	JUMPER STATUS	DESCRIPTION
J37	1 – 2	**S/PDIF_IN_SEL** Select the S/PDIF electrical input.
J36	2 - 3	**MICP_SRC** Select line level phono analogue input
J10	2 - 3	**USB power supply selected for all supplies**
H5	1-2 9-10 13-14 17-18 21-22	**AIF Interface** These links needed for connection to external clock source and Digital Din derived from the S/PDIF interface. Also connect DOUT to S/PDIF output.

Table 7 Jumper Settings for LRINPUT to ADC Record

REGISTER	SETTING	COMMENT
0x0F - write	0x0000	Reset device if required
0x0F - read	-	Read Chip ID (=0x1801)
0x08 - write	0x01F4	Enable system clocks
0x57 - write	0x0020	Enable the write sequencer.
0x5A - write	0x0080	Start the write sequencer to configure pre-programmed enable of the DAC playback (digital input to headphone output) path. Analogue input PGAs still muted.
Allow enough time for the sequencer to finish		
0x5D - read	-	Read status of write sequencer and wait until the WSEQ_BUSY,bit0,=0 which indicates that the DAC playback path has been configured. Then continue.
0x5A - write	0x0092	Start the write sequencer to configure pre-programmed enable of the ADC record (line input to digital output) path
Allow enough time for the sequencer to finish		
0x5D - read	-	Read status of write sequencer and wait until the WSEQ_BUSY,bit0,=0. Then continue.
0x00 - write	0x011F	Unmute left analogue input, leave input PGA volume gain at default 0dB
0x01 - write	0x011F	Unmute right analogue input, leave input PGA volume gain at default 0dB

Table 8 Register Settings for LRINPUT to ADC Record

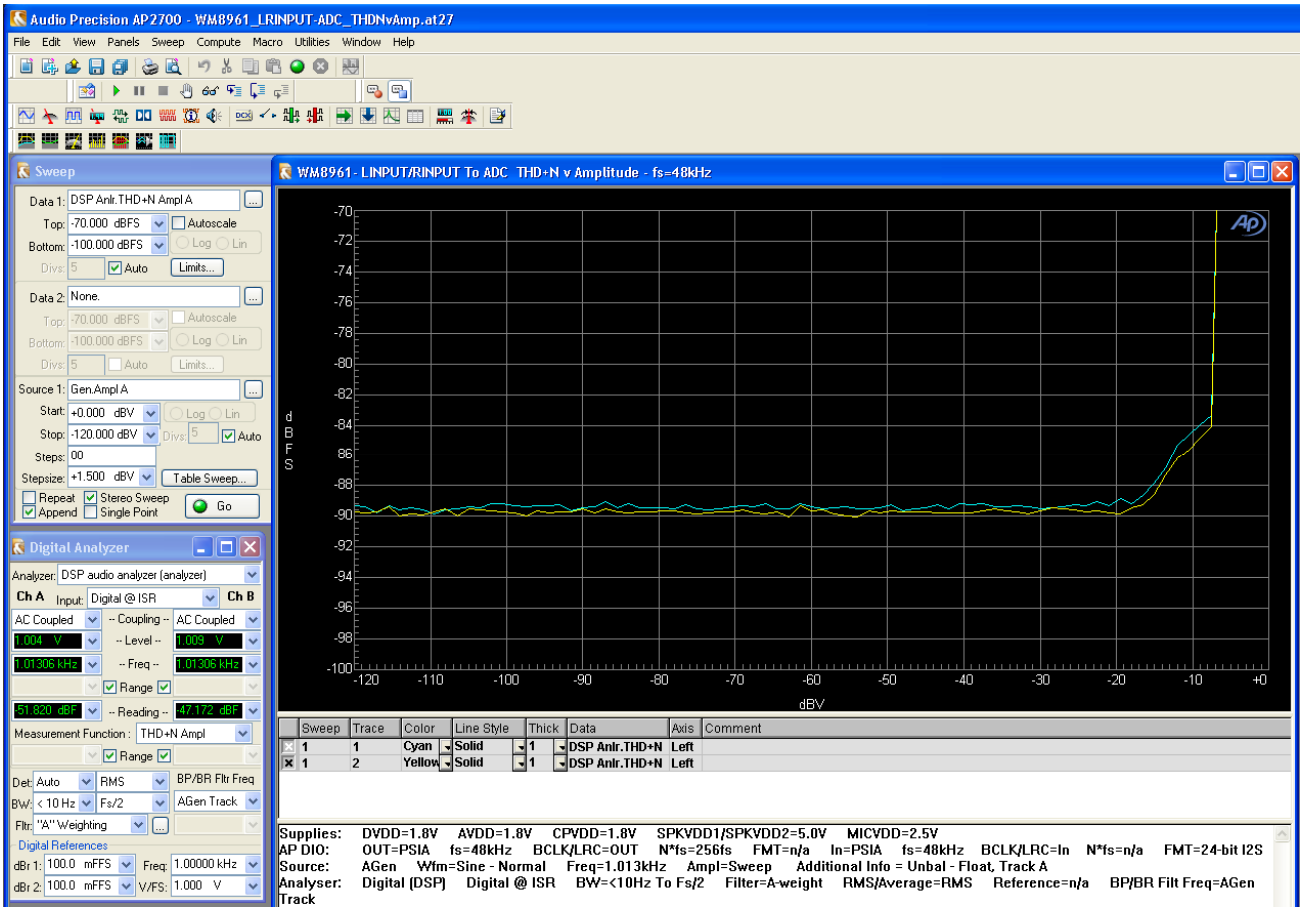

Figure 8 WM8961 Performance Plot for LRINPUT to ADC Record (0dBFS signal)

GENERAL HARDWARE SETUP INFORMATION

BOARD POWER SUPPLIES

The WM8961 customer evaluation board power supplies can be supplied using one of two sources:

- Individual external power supplies
- Derived from the USB connection or an external +5V.

The evaluation board can be powered either from the 4mm power lead receptacles (see Table 10) or from the USB/+5V host. Selection of using external power supplies or USB/+5V powered is made using the links shown in Table 9.

REF-DES	LINK STATUS	DESCRIPTION
J10 (+5V_SEL)	1 - 2 2 - 3	**+5V Power Source Select** +5V 4mm power jack receptacle selected USB power source selected (see note 1) [default setting]
J11 (DVDD_SEL)	1 - 2 2 - 3	**DVDD Power Source Select** DVDD 4mm power jack receptacle selected 1.8v regulator, derived from either USB power source or 5V power selected (depending on J10) [default setting]
J12 (MICVDD_SEL)	1 - 2 2 - 3	**MICVDD Power Source Select** MIC_VDD 4mm power jack receptacle selected 1.8v regulator, derived from either USB power source or 5V power selected (depending on J10) [default setting]
J13 (CPVDD_SEL)	1 - 2 2 - 3	**CPVDD Power Source Select** 1.8v regulator, derived from either USB power source or 5V power selected (depending on J10) [default setting]
J14 (AVDD_SEL)	1 - 2 2 - 3	**AVDD Power Source Select** AVDD 4mm power jack receptacle selected 1.8v regulator, derived from either USB power source or 5V power selected (depending on J10) [default setting]
J15 (SPKVDD_SEL)	1 - 2 2 - 3	**SPKVDD1 and SPK2VDD Power Source Select** SPKVDD 4mm power jack receptacle selected USB power source (not recommended - see note 1) or 5V power source selected (depending on J10) [default setting]

Table 9 Power Supply Source Select

Notes:

1. USB nominal supply voltage is 5v, however this will reduce with several USB devices powered off the PC, or when a hub is used. In particular, under extreme load conditions (such as using the speaker output at full power), the voltage may drop to around 4v or lower. **Hence the USB power source is not recommended for evaluating the speaker outputs.**

If the board is being powered using external power supplies, using appropriate power leads with 4mm connectors, supplies can be connected as described in Table 10.

REF-DES	SOCKET NAME	SUPPLY
J1	+5V	+5V
J2	DVDD	+1.62V to +2.0V
J3	GND	0V
J4	MICVDD	+1.71V to +3.6V
J5	CPVDD	+1.71V to +2.0V
J7	AVDD	+1.71V to +2.0V
J8	GND	0V
J9	SPKVDD	+2.7V to +5.5V

Table 10 External Power Supply Connections

Note: Refer to the datasheet for limitations on individual supply voltages.

Important: Exceeding the recommended maximum voltage can damage EVB components. Under voltage may cause improper operation of some or all of the EVB components.

POWER SUPPLY CURRENT MONITORING

MEASURING CURRENT

The WM8961 current drawn by the WM8961 from each power supply on the customer evaluation can be measured at the red jumper links. To measure current, the red jumper, shown in Table 11, should be replaced by a current measuring meter.

REF-DES	LINK NAME	SUPPLY CURRENT
J16	AVDD	AVDD
J17	SPKVDD1	SPKVDD1 (see note)
J20	CPVDD	CPVDD
J23	SPKVDD2	SPKVDD2 (see note)
J31	MICVDD	MICVDD
J32	DVDD	DVDD

Table 11 Power Supply Current Measuring Links

Note: There is a quiescent current drawn by the test equipment filter as described in the following section.

TEST EQUIPMENT FILTER

The speaker output test equipment filter as shown in figure 6 is populated for best performance when measuring the speaker output. There is a quiescent current through SPKVDD1/2 associated with this filter. Removing the capacitors C42, C46, C57, C62 as shown in Figure 9 will reduce the quiescent current through SPKVDD1/2, hence is the best solution for current measurements.

Removing this filter may affect speaker audio performance when using measurement equipment, due to the class D switching frequency. A class D measurement filter such as the Audio Precision AUX0025 (see http://www.ap.com) is effective at filtering out such frequencies however note that AUX0025 also has a quiescent current associated with it. Using such a class D measurement filter or leaving the components on the PCB is the best solution for performance measurement.

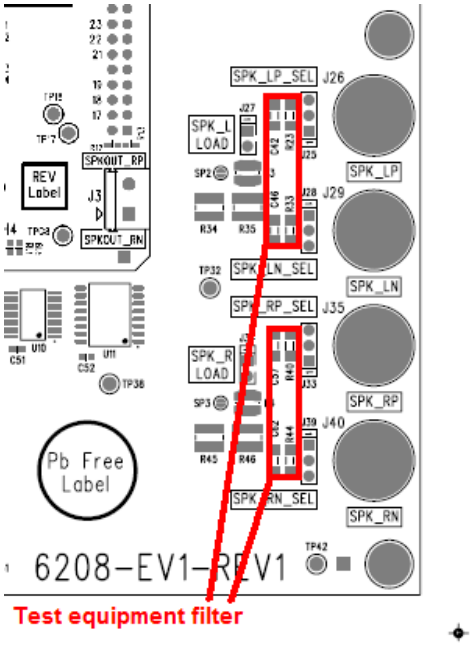

Figure 9 WM8961 Speaker Output Test Equipment Filter

S/PDIF INPUTS

The WM8961 evaluation board supports both electrical and optical input of the S/PDIF stream. This signal may be input via a standard phono connector J42 or via the optical receivers U14. The selection is made using header J37.Refer to Table 12 S/PDIF Input Connections for details.

REF-DES	LINK STATUS	DESCRIPTION
J37		**S/PDIF Input Source Select**
	1 - 2	Electrical input selected [default setting]
	2 - 3	Optical input selected

Table 12 S/PDIF Input Connections

DIGITAL INPUTS AND CLOCK INPUTS

The WM8961 evaluation board allows AIF data and clocks to be applied through a 24 pin header (H5) or through the S/PDIF interface. The following Table 13 shows the connections necessary. When H5 is not being used, the links should be put in place as described in this table.

REF-DES	PIN	DESCRIPTION
H5	1-2	AIF LRCLK input. Requires link between pins 1-2 when H5 not connected to external source.
	9-10	AIF BCLK input. Requires link between pins 9-10 when H5 not connected to external source.
	13-14	AIF Digital Input Data. Requires link between pins 13-14 when H5 not connected to external source.
	17-18	AIF MCLK input. Requires link between pins 17-18 when H5 not connected to external source.
	21-22	AIF Digital output Data. Requires link between pins 21-22 when H5 not connected to external source.

Table 13 AIF Input via Header H5

ANALOGUE INPUTS

The WM8961 evaluation board is equipped to connect either a line level signal or a microphone input signal.

LINE INPUT

A line level input signal can be connected to the WM8961 via the dual Phono connector J38. If this interface is used, then header J36 should have pins 2-3 linked and no link fitted to J41 (see Table 14)

REF-DES	LINK STATUS	DESCRIPTION
J36		**MICP_SRC**
	1 - 2	Microphone (MIC1) selected as input source
	2 – 3	Line input (Phono connector J36) selected as input source
	No link fitted	Isolate MIC1 from MICBIAS
J41		**DIFFMICN**
	Link fitted	Microphone (MIC1) selected as input source
	No link fitted	Line input (Phono connector J36) selected as input source. Also isolates MIC1 from MICBIAS.

Table 14 Analogue Input Source Selection

MICROPHONE INPUT

A single-ended microphone can be connected to the input connector MIC1. For connection details see Table 14.

ANALOGUE OUTPUTS

HEADPHONE OUTPUT

The WM8961 evaluation board allows monitoring of the WM8961 analogue headphone outputs directly from the WM8961 device outputs. The WM8961 headphone outputs are available on the phono socket J19. The headphone output load can be selected between 16Ω and 32Ω using the headers J18 and J21.The selection of output load is shown in following table.

REF-DES	LINK STATUS	DESCRIPTION
J18		**HP_L_LOAD**
	1 - 2	Left channel headphone output load = 32Ω
	2 - 3	Left channel headphone output load = 16Ω
J21		**HP_R_LOAD**
	1 - 2	Right channel headphone output load = 32Ω
	2 - 3	Right channel headphone output load = 16Ω

Table 15 Headphone Output Load Selection

CLASS D SPEAKER OUTPUTS

The WM8961 evaluation board allows speaker connection using the gold coloured binding posts. The evaluation board also offers the capability of providing a test load to the WM8961 Class D speaker drivers as well as allowing the connection of test equipment (AP2) filter.

The Class D speaker connections, load selection and test equipment filter selection are shown in Table 16, Table 17 and Table 18.

REF-DES	DESCRIPTION
J26	**SPK_LP** Class D left speaker positive connection output
J29	**SPK_LN** Class D left speaker negative connection output
J35	**SPK_RP** Class D right speaker positive connection output
J40	**SPK_RN** Class D right speaker negative connection output

Table 16 Class D Speaker Output Connections

REF-DES	LINK STATUS	DESCRIPTION
J27		**SPK_L_LOAD**
	Link in place	8.2Ω load presented to Class D left speaker output
	No link in place	No load presented to Class D left speaker output
J34		**SPK_R_LOAD**
	Link in place	8.2Ω load presented to Class D right speaker output
	No link in place	No load presented to Class D right speaker output

Table 17 Class D Speaker Output Load Connections

REF-DES	LINK STATUS	DESCRIPTION
J25	1-2	**SPK_LP_SEL** Low Pass Filter **not** connected to Class D left speaker +ve output
	2-3	Low Pass Filter connected to Class D left speaker +ve output
J28	1-2	**SPK_LN_SEL** Low Pass Filter **not** connected to Class D left speaker -ve output
	2-3	Low Pass Filter connected to Class D left speaker -ve output
J25	1-2	**SPK_RP_SEL** Low Pass Filter **not** connected to Class D right speaker +ve output
	2-3	Low Pass Filter connected to Class D right speaker +ve output
J28	1-2	**SPK_RN_SEL** Low Pass Filter **not** connected to Class D right speaker -ve output
	2-3	Low Pass Filter connected to Class D right speaker -ve output

Table 18 Class D Speaker Output Test Equipment Filter Connections

MCU CONTROL (VIA USB)

The WM8961 evaluation board is equipped with a USB interface MCU which allows interconnection with a PC in conjunction with the WM8961-EV1S evaluation software.

SOLDER PADS

Both the MAIN and MINI boards have solder pads connections. These are connections which when bridged, route signals to different connectors. The following table gives details on when the solder pad bridge should be connected.

BOARD	REF-DES	SP STATUS	DESCRIPTION
MINI	SP1	Not Bridged	Headphone Connector, J1, on MINI board used as headphone output.
	SP2	Not Bridged	
MINI	SP1	Bridged	Headphone Connector, J19, on MAIN board used as headphone output.
	SP2	Bridged	
MINI	SP3	Not Bridged	MINI board surface mount microphone, MIC, bias is not connected. This allows the MIC1 microphone jack socket on the MAIN board to be used as microphone input.
MINI	SP3	Bridged	MINI board surface mount microphone, MIC, has bias connected. If this is connected then do not use RINPUT to MINI board and remove MAIN board links J41 and J36 to isolate MAIN board MIC1 jack socket.
MAIN	SP2	Not Bridged	Left speaker output load includes a 10uH inductor.
	SP3	Not Bridged	Right speaker output load includes a 10uH inductor
MAIN	SP2	Bridged	Left speaker output load is resistive only.
	SP3	Bridged	Right speaker output load is resistive only.

Table 19 Main and Mini Board Solder Pad (SP) Connections

LED INDICATORS

The WM8961 evaluation board has a number of LEDs. Their function is described in Table 20.

LED	REF_DES	DESCRIPTION	
		LED OFF	LED ON
LED1	SPKVDD_PWR_OK	No Class D speaker voltage available.	Class D speaker voltage is OK
LED2	DIGITAL_REG_OK	Digital voltage regulator not operational.	+1.8V Digital Voltage regulator OK
LED3	S/PDIF_REG_OK	No S/PDIF Power detected	+3.3V S/PDIF Voltage regulator OK
LED4	USB_OK	USB Interface non-operational	USB Interface operational
LED5	USB_PWR_LOW!	USB Power OK. **Note**: this does not guarantee that there is sufficient power to drive speaker outputs within specified distortion levels – an external supply is recommended for SPKVDD during speaker testing.	RED = USB Power is low. .
LED6	S/PDIF Receive Error	No S/PDIF error	RED = S/PDIF Error detected. Try moving J37 to select correct SPDIF source.

Table 20 LED Descriptions

JUMPER SETTINGS

DAC TO HEADPHONE OUTPUT AND LINE IN TO ADC

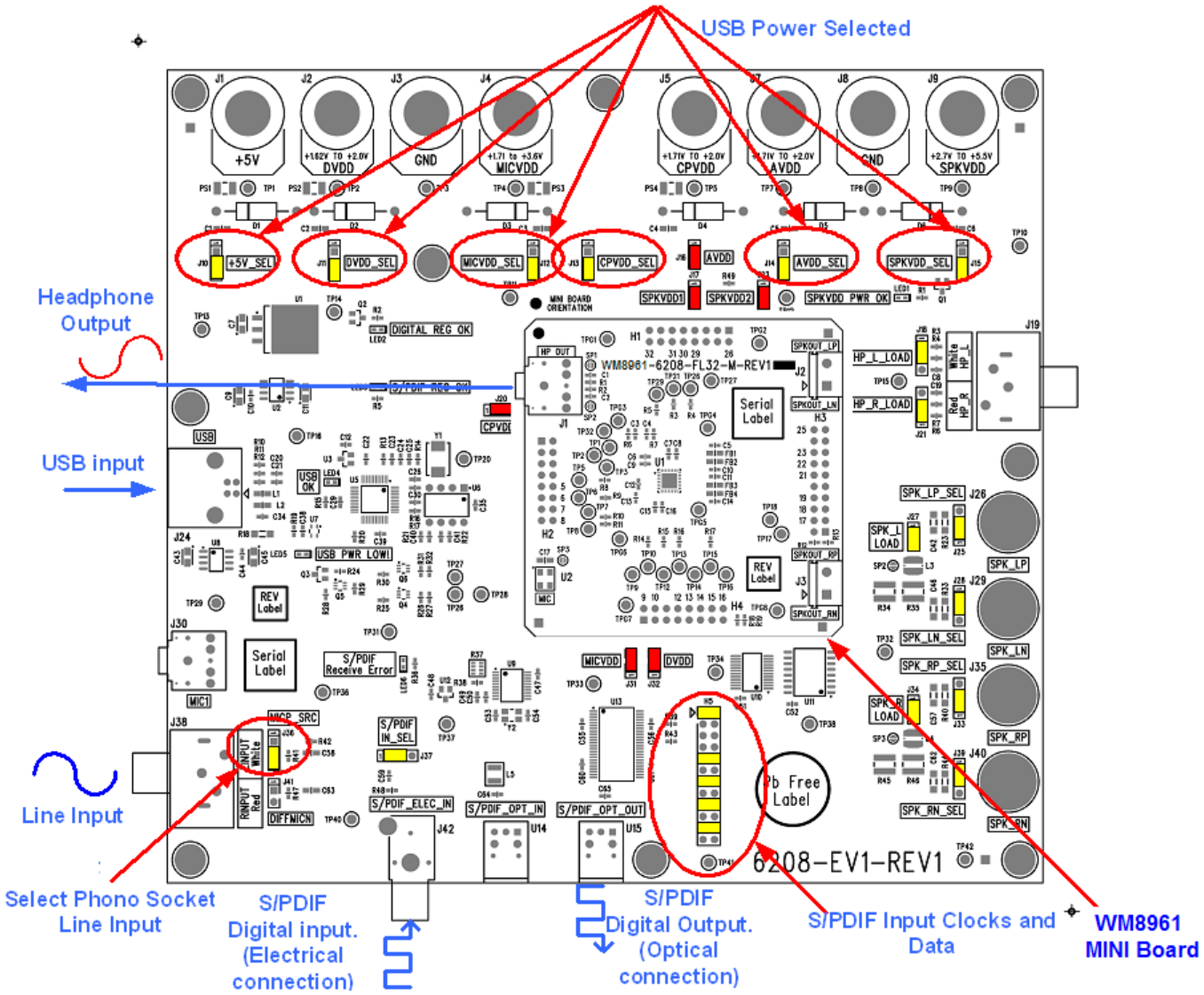

Figure 10 WM8961 Main and Mini Evaluation Board Configuration for DAC to Headphone Out and Line Input to ADC

DAC TO SPEAKER

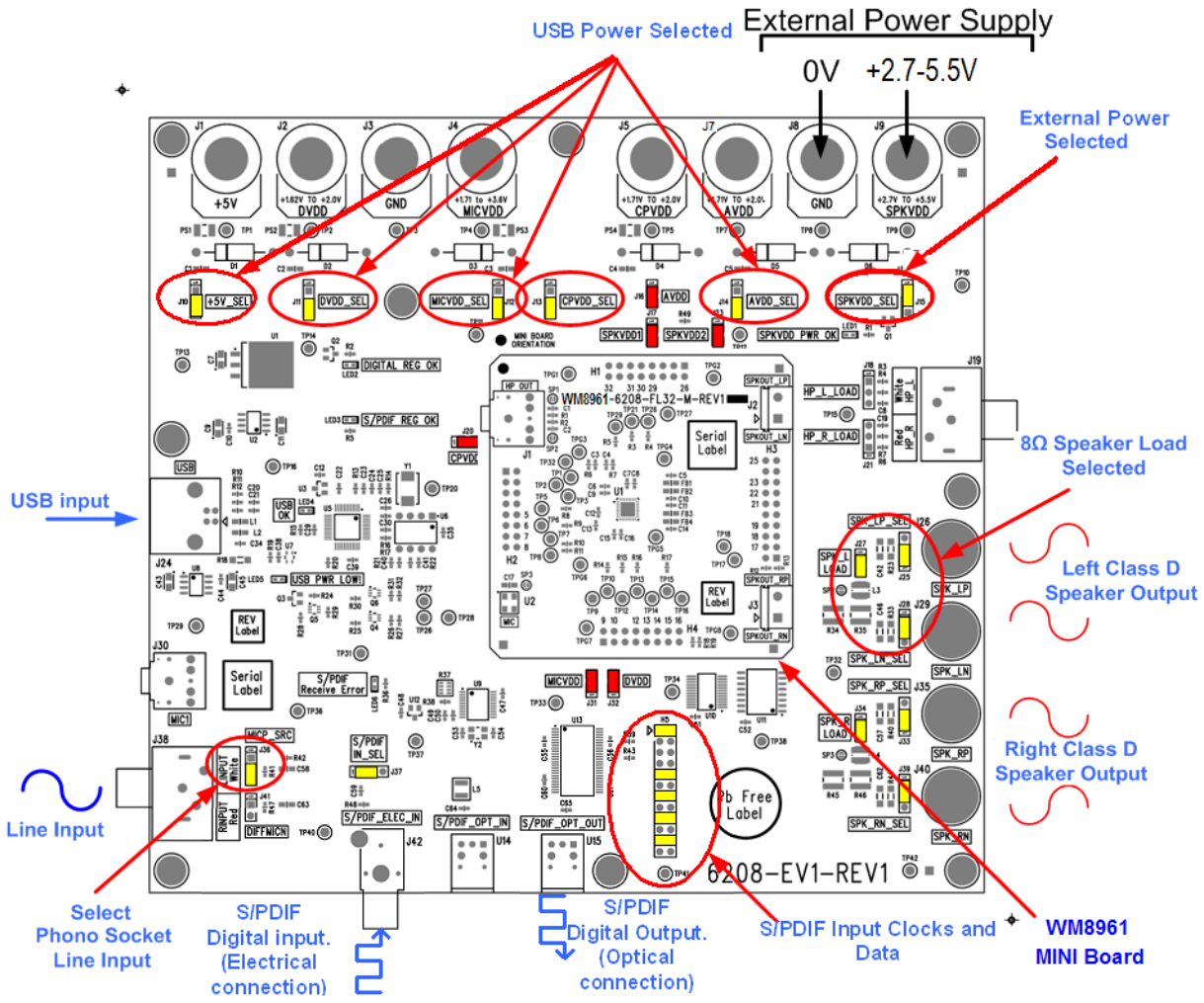

Figure 11 WM8961 Main and Mini Evaluation Board Configuration for DAC to Speaker

WM8961-6208-FL32-M STAND-ALONE BOARD CONFIGURATION

The WM8961 mini board can be used a stand-alone module for direct connection to a processor board via flying leads or dedicated headers. This section details important considerations and provides all information required to do this without risking damage to the device.

CONNECTION DIAGRAM

The diagram, Figure 12, below shows the connections required to power-up and control the WM8961 mini board. Connections can be made through flying leads or with 2.54mm pitch headers compatible with those on the mini board.

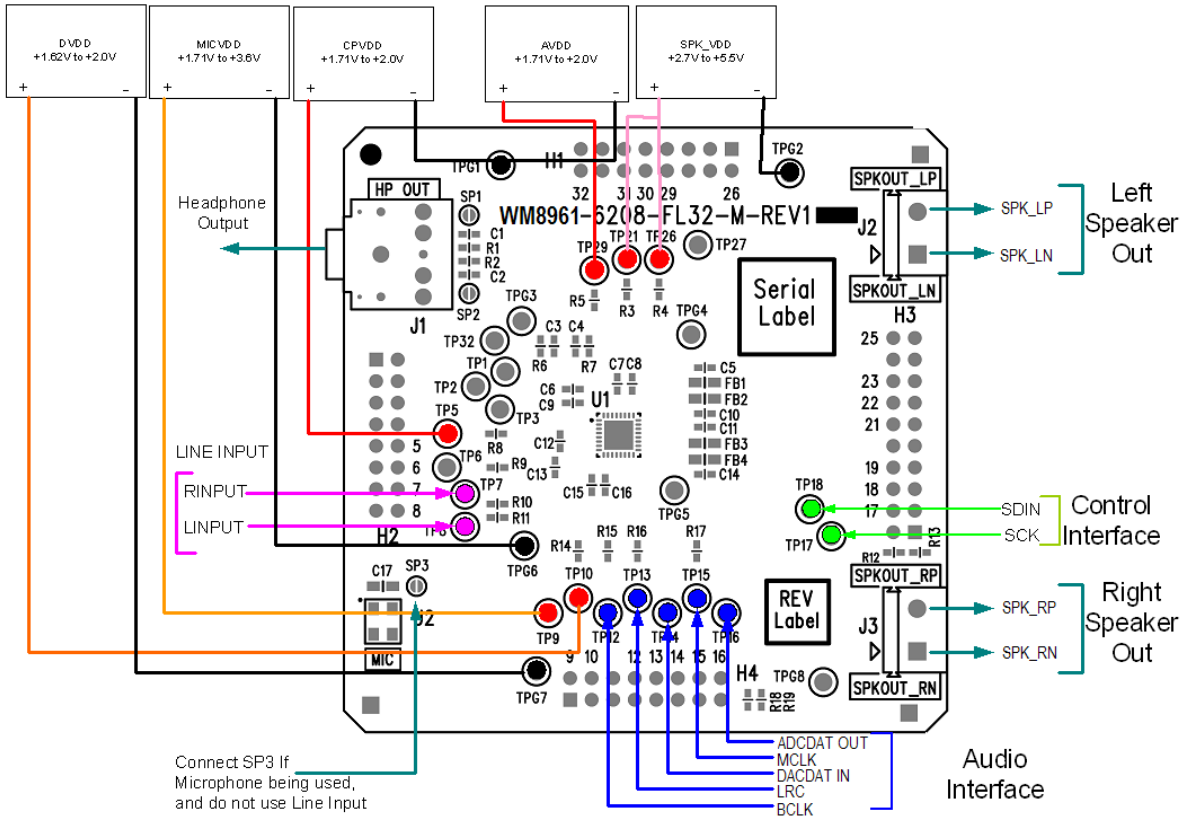

Figure 12 WM8961 Mini Board Stand Alone Connections

APPLICATION SUPPORT

If you require more information or require technical support, please contact the Wolfson Microelectronics Applications group through the following channels:

Email: apps@wolfsonmicro.com
Telephone Apps: +44 (0) 131 272 7070
Fax: +44 (0) 131 272 7001
Mail: Applications Engineering at the address on the last page

or contact your local Wolfson representative.

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