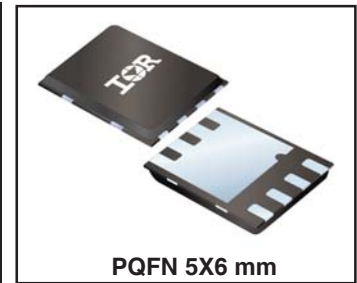
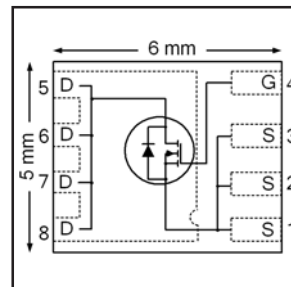


V_{DS}	40	V
R_{DS(on)} max (@ V _{GS} = 10V)	2.6	mΩ
Q_g (typical)	73	nC
R_G (typical)	1.2	Ω
I_D (@ T _{mb} = 25°C)	100 Ⓢ	A



Applications

- Secondary Side Synchronous Rectification
- Inverters for DC Motors
- DC-DC Brick Applications
- Boost Converters

Features and Benefits

Features

Low R _{DS(on)} (≤ 2.6mΩ)
Low Thermal Resistance to PCB (≤ 0.8°C/W)
100% R _g tested
Low Profile (≤ 0.9 mm)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant Containing no Lead, no Bromide and no Halogen
MSL1, Industrial Qualification

results in
⇒

Benefits

Lower Conduction Losses
Enables better thermal dissipation
Increased Reliability
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Base Part Number	Package Type	Standard Pack		Orderable part number	Note
		Form	Quantity		
IRFH5004PBF	PQFN 5mm x 6mm	Tape and Reel	4000	IRFH5004TRPBF	EOL notice #259
	PQFN 5mm x 6mm	Tape and Reel	1000	IRFH5004TR2PBF	

Absolute Maximum Ratings

	Parameter	Max.	Units
V _{DS}	Drain-to-Source Voltage	40	V
V _{GS}	Gate-to-Source Voltage	±20	
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V	28	A
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ 10V	23	
I _D @ T _{mb} = 25°C	Continuous Drain Current, V _{GS} @ 10V	100 Ⓢ	
I _D @ T _{mb} = 100°C	Continuous Drain Current, V _{GS} @ 10V	100 Ⓢ	
I _{DM}	Pulsed Drain Current ①	400	W
P _D @ T _A = 25°C	Power Dissipation ⑤	3.6	
P _D @ T _{mb} = 25°C	Power Dissipation ⑤	156	
	Linear Derating Factor ⑤	0.029	
T _J	Operating Junction and	-55 to + 150	°C
T _{STG}	Storage Temperature Range		

Notes ① through ⑤ are on page 8

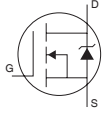
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.04	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	2.1	2.6	m Ω	$V_{GS} = 10V, I_D = 50A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 150\mu A$
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	-5.6	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 40V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
gfs	Forward Transconductance	91	—	—	S	$V_{DS} = 15V, I_D = 50A$
Q_g	Total Gate Charge	—	73	110	nC	$V_{DS} = 20V$ $V_{GS} = 10V$ $I_D = 50A$ See Fig.17 & 18
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	15	—		
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	6.1	—		
Q_{gd}	Gate-to-Drain Charge	—	27	—		
Q_{godr}	Gate Charge Overdrive	—	25	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	33.1	—		
Q_{oss}	Output Charge	—	27	—	nC	$V_{DS} = 16V, V_{GS} = 0V$
R_G	Gate Resistance	—	1.2	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	$V_{DD} = 20V, V_{GS} = 10V$ $I_D = 50A$ $R_G = 1.8\Omega$ See Fig.15
t_r	Rise Time	—	39	—		
$t_{d(off)}$	Turn-Off Delay Time	—	28	—		
t_f	Fall Time	—	16	—		
C_{iss}	Input Capacitance	—	4490	—	pF	$V_{GS} = 0V$ $V_{DS} = 20V$ $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	970	—		
C_{rss}	Reverse Transfer Capacitance	—	460	—		

Avalanche Characteristics

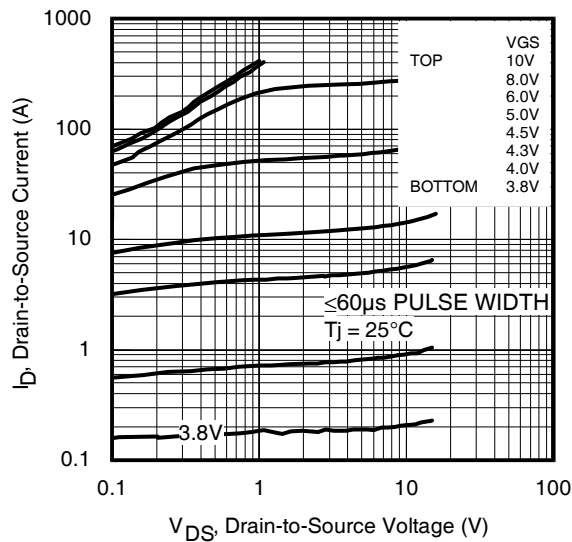
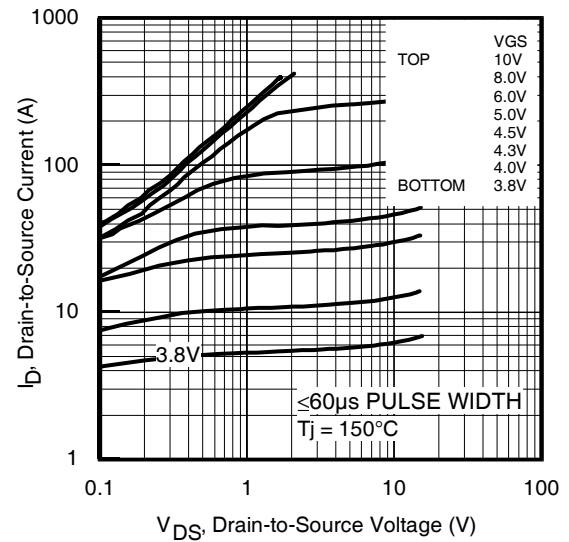
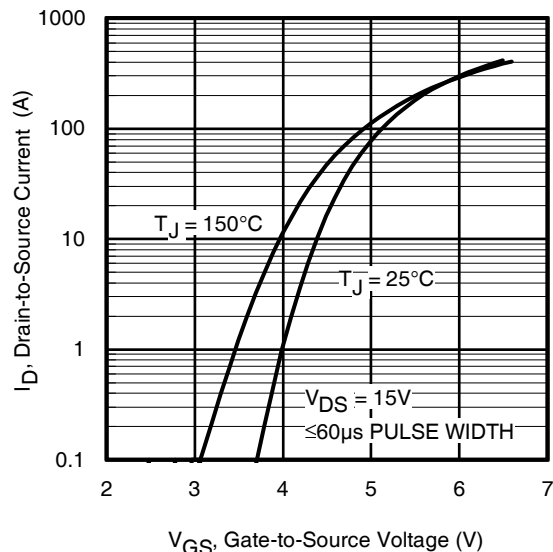
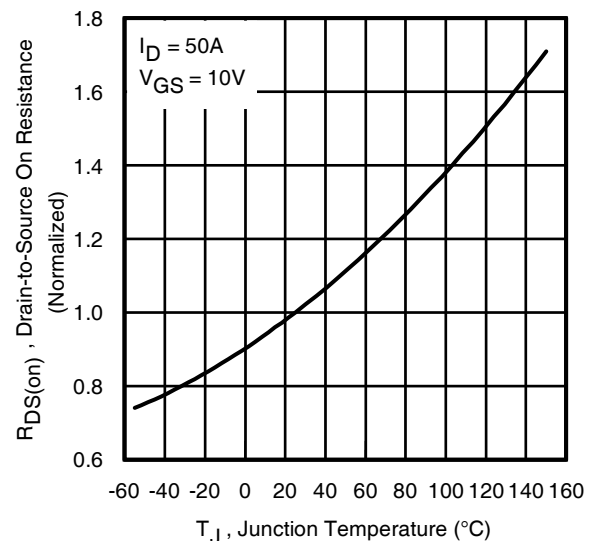
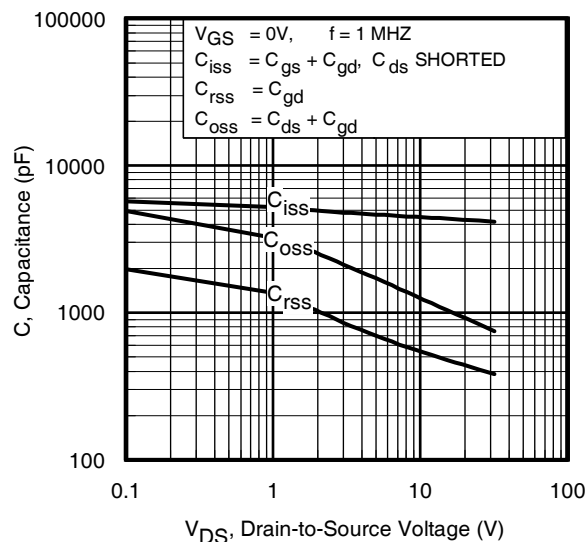
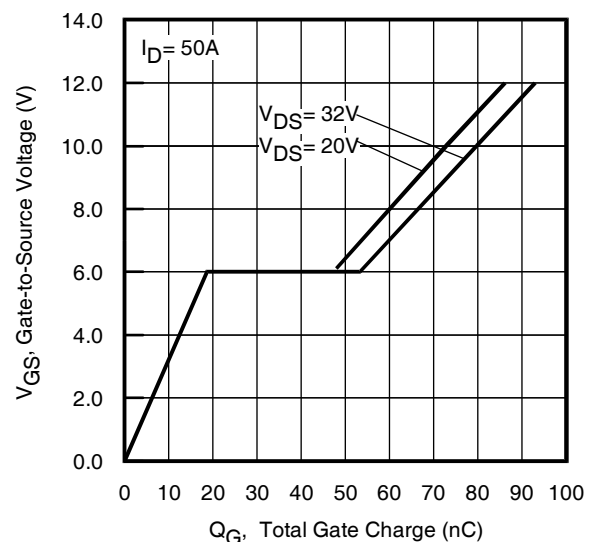
	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	340	mJ
I_{AR}	Avalanche Current ①	—	50	A

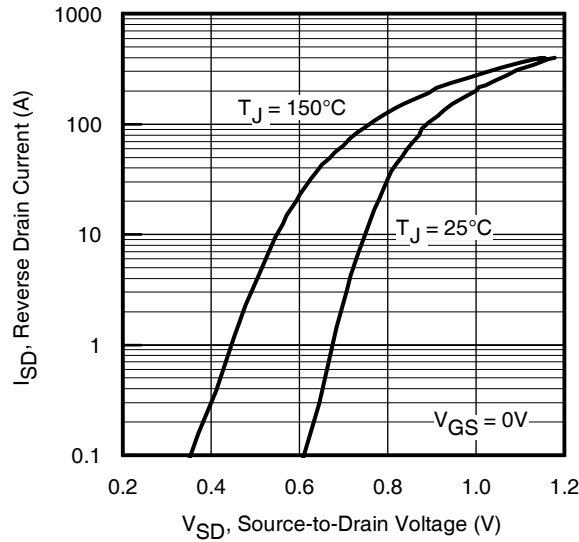
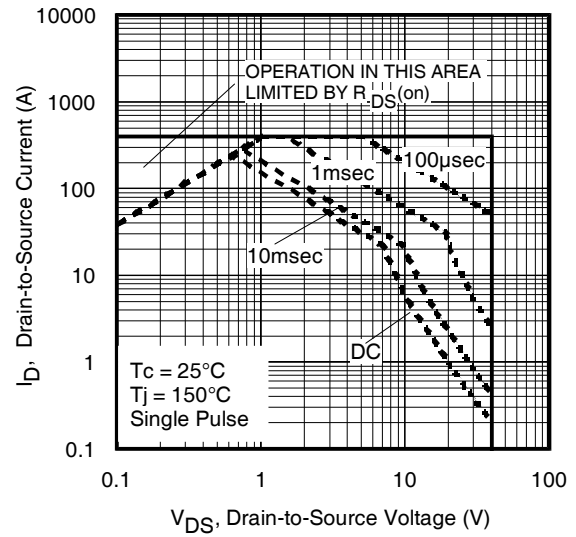
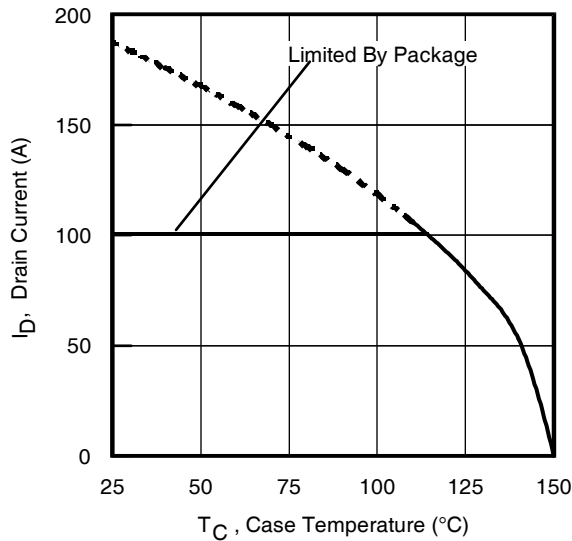
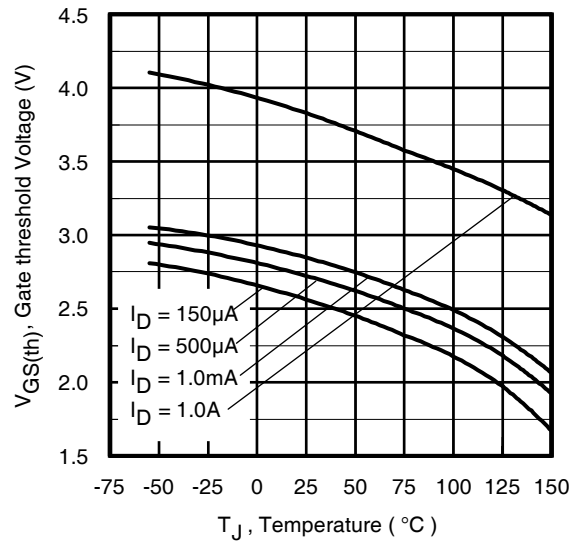
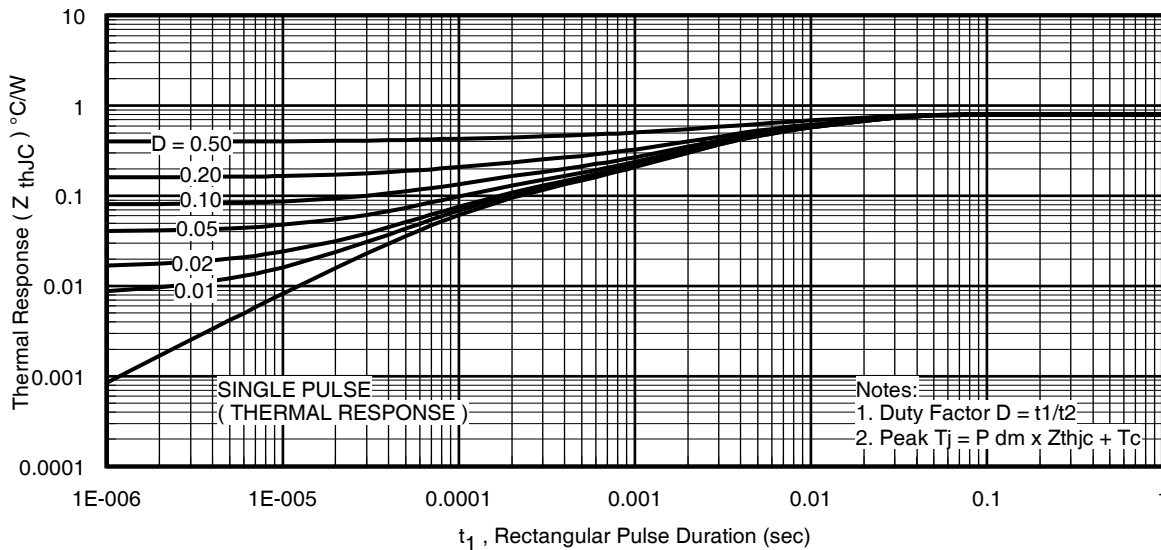
Diode Characteristics

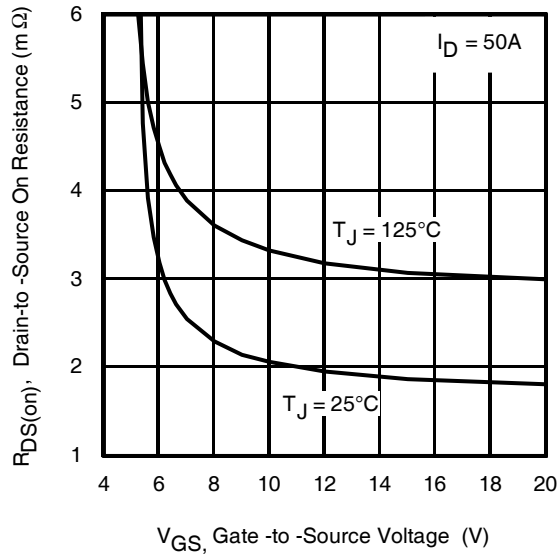
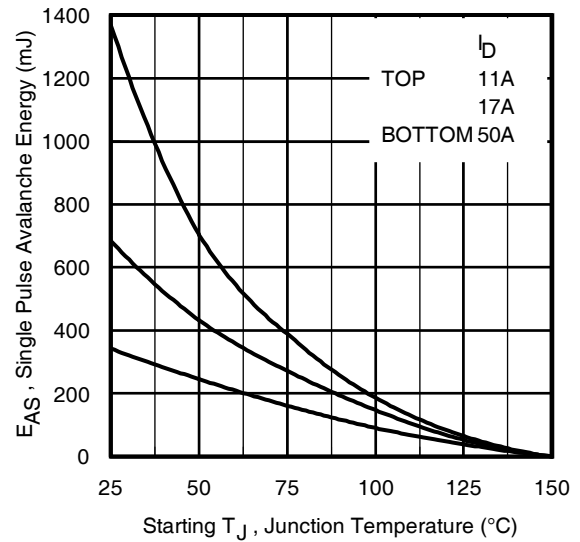
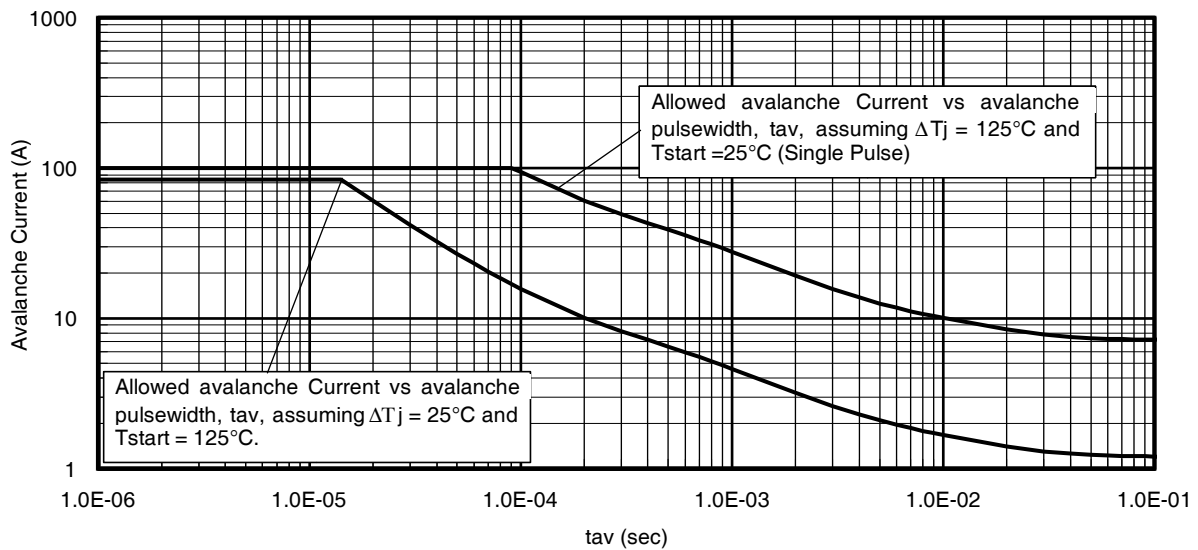
	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode) ⑥	—	—	100	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	400		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	$T_J = 25^\circ\text{C}, I_S = 50A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	32	48	ns	$T_J = 25^\circ\text{C}, I_F = 50A, V_{DD} = 20V$
Q_{rr}	Reverse Recovery Charge	—	100	150	nC	$di/dt = 300A/\mu s$ ③
t_{on}	Forward Turn-On Time	Time is dominated by parasitic Inductance				

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC-mb}$	Junction-to-Mounting Base	0.5	0.8	$^\circ\text{C/W}$
$R_{\theta JC}$ (Top)	Junction-to-Case ④	—	15	
$R_{\theta JA}$	Junction-to-Ambient ⑤	—	35	
$R_{\theta JA} (<10s)$	Junction-to-Ambient ⑤	—	33	


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Threshold Voltage vs. Temperature

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Mounting Base


Fig 12. On-Resistance vs. Gate Voltage

Fig 13. Maximum Avalanche Energy vs. Drain Current

Fig 14. Typical Avalanche Current vs. Pulsewidth

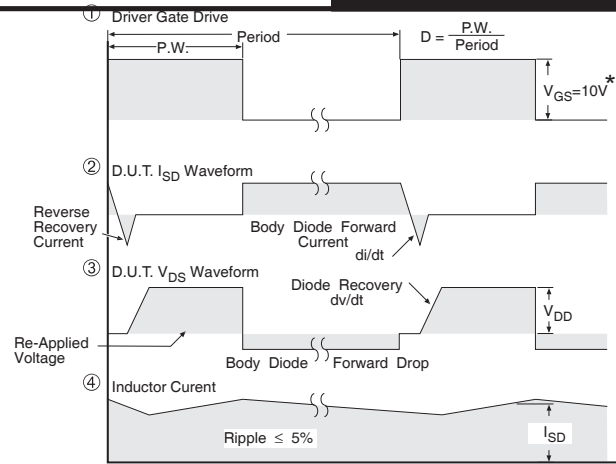
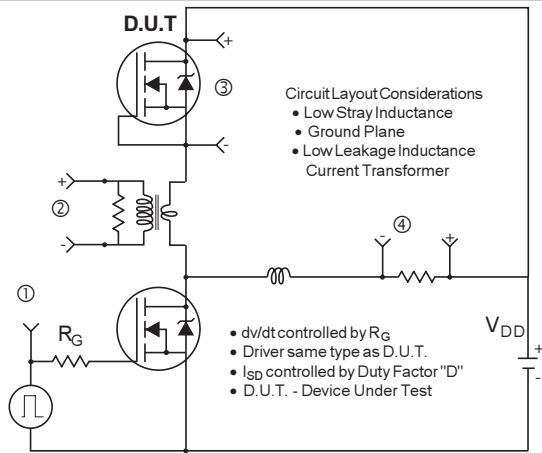


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

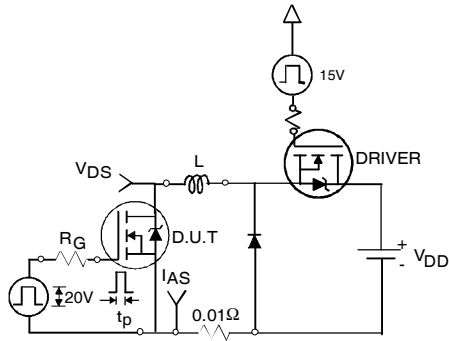


Fig 16a. Unclamped Inductive Test Circuit

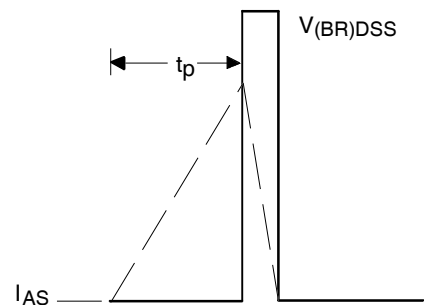


Fig 16b. Unclamped Inductive Waveforms

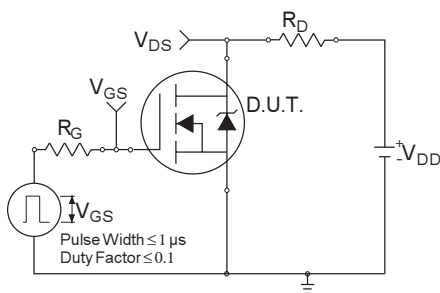


Fig 17a. Switching Time Test Circuit

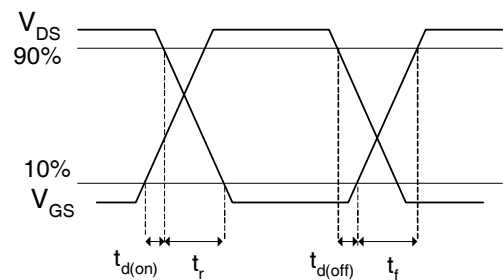


Fig 17b. Switching Time Waveforms

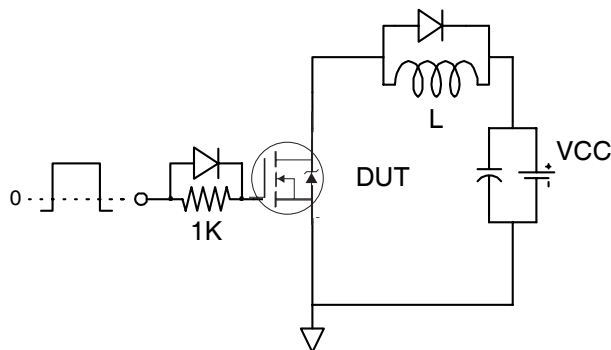


Fig 18a. Gate Charge Test Circuit

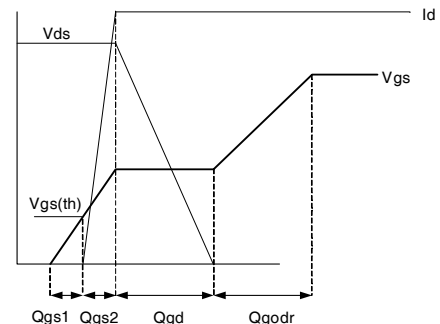
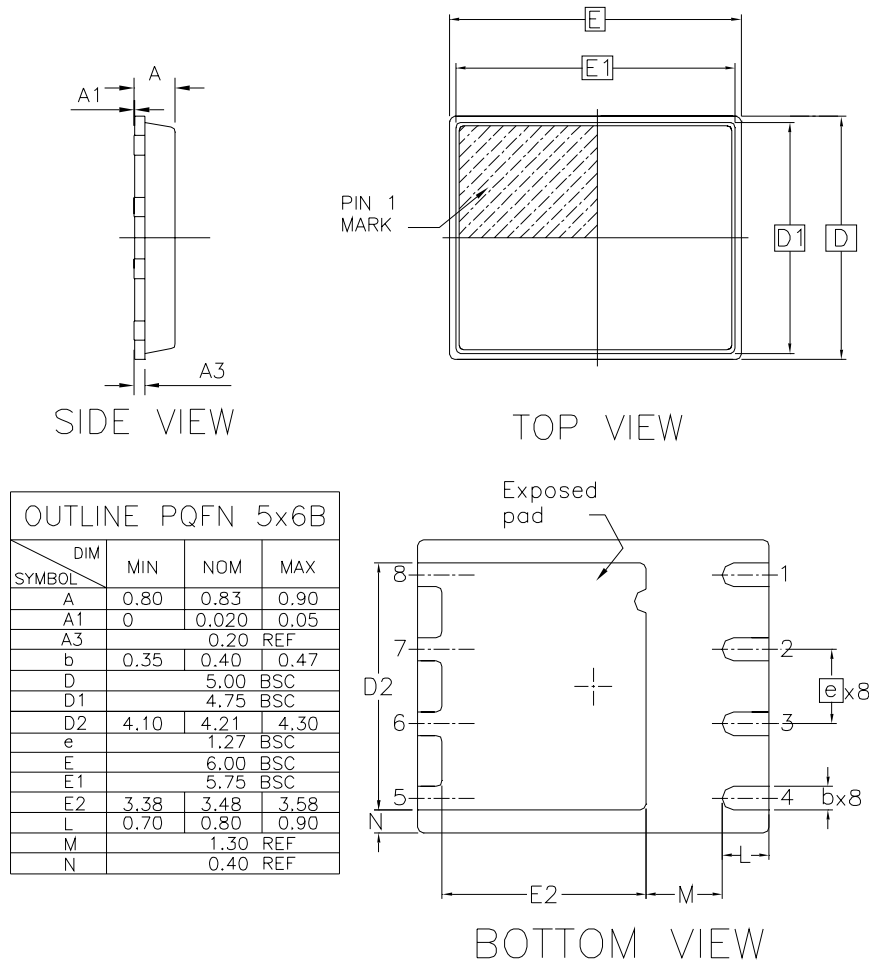


Fig 18b. Gate Charge Waveform

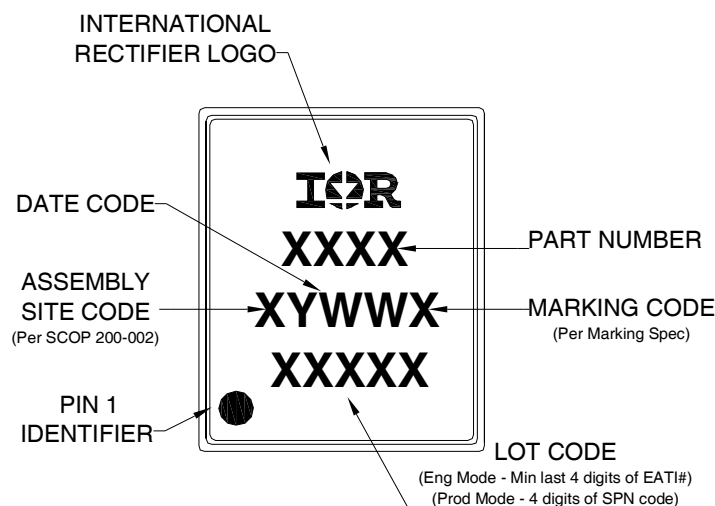
PQFN 5x6 Outline "B" Package Details



For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>

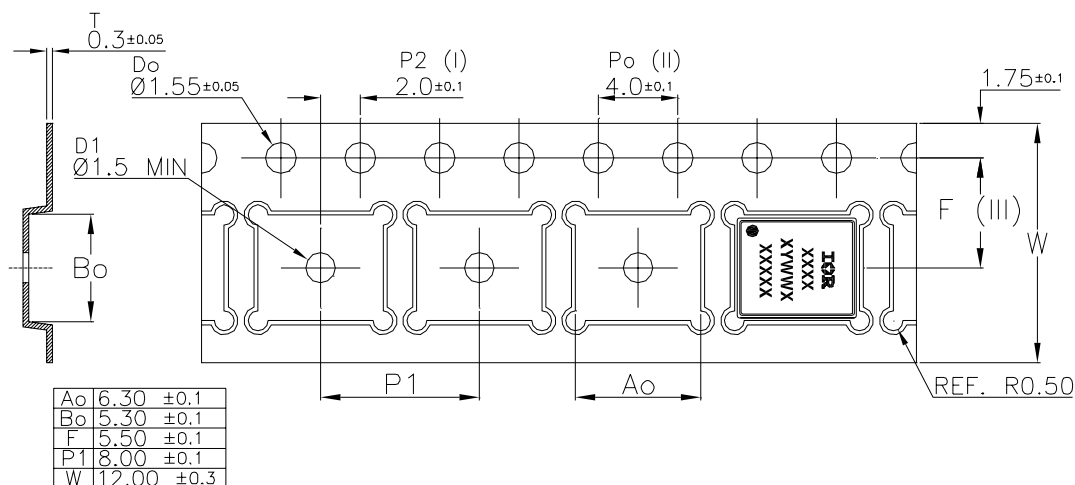
For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

PQFN 5x6 Outline "B" Part Marking



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

PQFN 5x6 Outline "B" Tape and Reel



Qualification information[†]

Qualification level	Industrial ^{††} (per JEDEC JESD47F ^{†††} guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D ^{†††})
RoHS compliant	Yes	

[†] Qualification standards can be found at International Rectifier's web site

<http://www.irf.com/product-info/reliability>

^{††} Higher qualification ratings may be available should the user have such requirements.

Please contact your International Rectifier sales representative for further information:

<http://www.irf.com/whoto-call/salesrep/>

^{†††} Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting T_J = 25°C, L = 0.27mH, R_G = 50Ω, I_{AS} = 50A.
- ③ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ④ R_θ is measured at T_J of approximately 90°C.
- ⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material.
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package is limited to 100A by production test capability.

Revision History

Date	Comment
1/13/2014	• Updated ordering information to reflect the End-Of-Life (EOL) of the mini-reel option (EOL notice #259). • Updated data sheet with the new IR corporate template.

International
 Rectifier

IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245, USA

To contact International Rectifier, please visit <http://www.irf.com/whoto-call/>