CY62177DV30 MoBL®

32-Mbit (2 M × 16) Static RAM

Features

- Very high speed: 55 ns
- Wide voltage range: 2.20 V–3.60 V
- Ultra-low active power
  - Typical active current: 2 mA at f = 1 MHz
  - Typical active current: 15 mA at f = f_{max}
- Ultra low standby power
- Easy memory expansion with $\overline{CE}_1$, CE_2 and $\overline{OE}$ features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed/power
- Packages offered in a 48-ball fine ball grid array (FBGA)

Functional Description

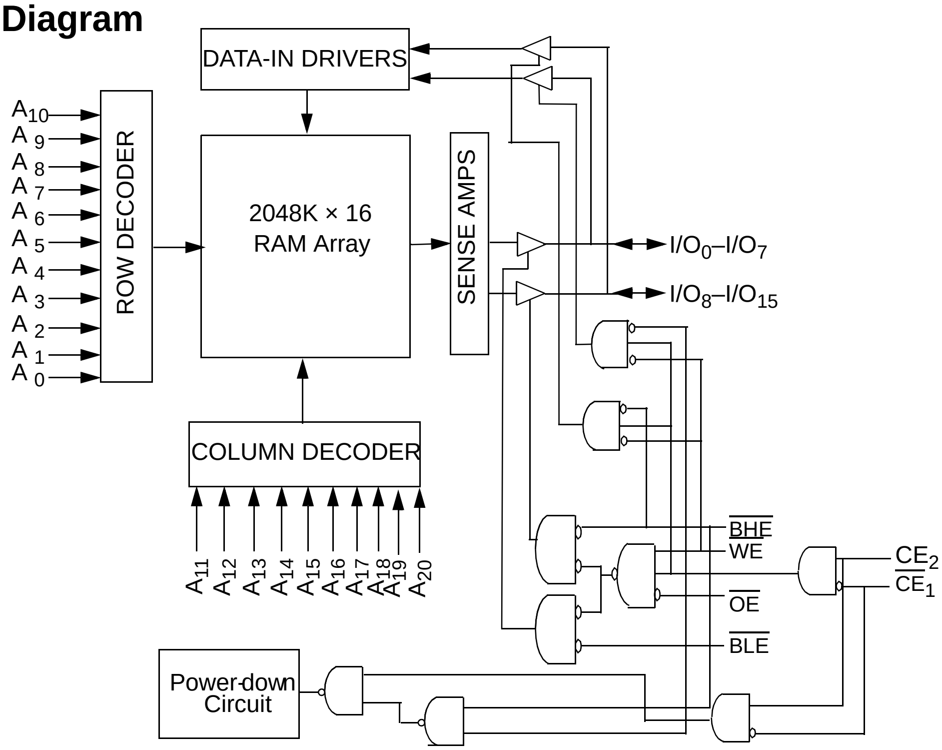
The CY62177DV30 is a high-performance CMOS static RAM organized as 2M words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones.The device also has an automatic power-down feature that significantly reduces power consumption. The device can also be put into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE}_1$HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{20}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{20}).

Reading from the device is accomplished by taking Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table for a complete description of read and write modes.

For a complete list of related documentation, click here.

Logic Block Diagram



Contents

Pin Configuration[1]

Figure 1. 48-Ball FBGATop View

	1	2	3	4	5	6
A	$\overline{BLE}$	$\overline{OE}$	A_0	A_1	A_2	CE_2
B	I/O_8	$\overline{BHE}$	A_3	A_4	$\overline{CE}_1$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SS}	I/O_{11}	A_{17}	A_7	I/O_3	Vcc
E	V_{CC}	I/O_{12}	DNU	A_{16}	I/O_4	Vss
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	A_{19}	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	A_{18}	A_8	A_9	A_{10}	A_{11}	A_{20}

Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC}(mA)				Standby I_{SB2}(μA)	
					f = 1 MHz		f = f_{max}			
	Min	Typ[2]	Max		Typ[2]	Max	Typ[2]	Max	Typ[2]	Max
CY62177DV30LL	2.2	3.0	3.6	55	2	4	15	30	5	50

Notes
1. DNU pins have to be left floating or tied to Vss to ensure proper application.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .... –65 °C to + 150 °C

Ambient temperature with power applied .... –55 °C to + 125 °C

Supply voltage to ground potential ...... –0.3 V to V_{CC} + 0.3 V

DC voltage applied to outputs in High Z state[3, 4] .... –0.3 V to V_{CC} + 0.3 V

DC input voltage[3, 4]........................... –0.3 V to V_{CC} + 0.3 V

Output current into outputs (LOW) .... 20 mA

Static discharge voltage.. >2001 V (per MIL-STD-883, method 3015)

Latch-up current... >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[5]
CY62177DV30LL	Industrial	–40 °C to +85 °C	2.20 V to 3.60 V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ[6]	Max	Unit
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA	V_{CC} = 2.20 V	2.0	–	–	V
		I_{OH} = –1.0 mA	V_{CC} = 2.70 V	2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 0.1 mA	V_{CC} = 2.20 V	–	–	0.4	V
		I_{OL} = 2.1 mA	V_{CC} = 2.70 V	–	–	0.4	V
V_{IH}	Input HIGH voltage	V_{CC} = 2.2 V to 2.7 V		1.8	–	V_{CC} +0.3 V	V
		V_{CC} = 2.7 V to 3.6 V		2.2	–	V_{CC} +0.3 V	V
V_{IL}	Input LOW voltage	V_{CC} = 2.2 V to 2.7 V		–0.3	–	0.6	V
		V_{CC} = 2.7 V to 3.6 V		–0.3	–	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{MAX} = $1/t_{RC}$	V_{CC} = V_{CCmax} I_{OUT} = 0 mA CMOS levels		15	30	mA
		f = 1 MHz			2	4	mA
I_{SB1}	Automatic CE power-down current—CMOS inputs	$\overline{CE}_1$ ≥ V_{CC}–0.2 V, CE_2 < 0.2 V, V_{IN} ≥ V_{CC}–0.2 V, V_{IN} ≤ 0.2 V) f = f_{MAX} (address and data only), f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$ and $\overline{BLE}$), V_{CC} = 3.60 V		–	5	100	µA
I_{SB2}	Automatic CE power-down current—CMOS inputs	$\overline{CE}_1$ ≥ V_{CC} – 0.2 V, CE_2 < 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = 3.60 V		–	5	50	µA

Notes

3. $V_{IL(min.)}$ = –2.0 V for pulse durations less than 20 ns.
4. $V_{IH(Max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
5. Full device AC operation requires linear V_{CC} ramp from 0 to $V_{CC(min)}$ ≥ 500 µs.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ.)}$, T_A = 25 °C

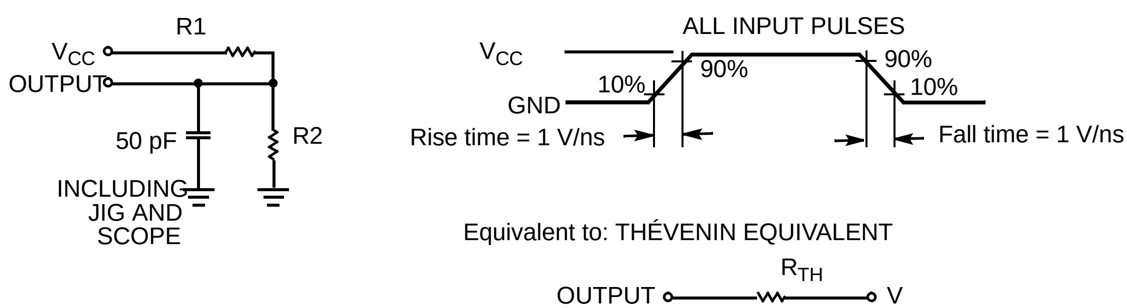
Capacitance

Parameter[7]	Description	Test Conditions	Max.	Unit
C_{IN}	Input capacitance	$T_A = 25\ °C$, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	12	pF
C_{OUT}	Output capacitance		12	pF

Thermal Resistance

Parameter[7]	Description	Test Conditions	BGA	Unit
θ_{JA}	Thermal resistance (Junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	55	°C/W
θ_{JC}	Thermal resistance (Junction to case)		16	°C/W

AC Test Loads and Waveforms



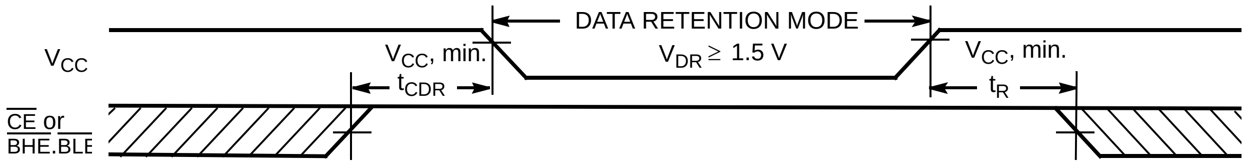
Parameters	2.5 V (2.2 V to 2.7 V)	3.0 V (2.7 V to 3.6 V)	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min	Typ[8]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	–	V
I_{CCDR}	Data retention current	$\overline{V_{CC}} = 1.5$ V $\overline{CE_1} \geq V_{CC} - 0.2$ V, $CE_2 < 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	–	25	µA
t_{CDR}[7]	Chip deselect to data retention time		0	–	–	ns
t_R[9]	Operation recovery time		55	–	–	ns

Notes
7. Tested initially and after any design or process changes that may affect these parameters.
8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25\ °C$
9. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100\ \mu s$ or stable at $V_{CC(min.)} \geq 100\ \mu s$.

Data Retention Waveform[10, 11]



Switching Characteristics Over the Operating Range

Parameter[11, 12]	Description	Min	Max	Unit
READ CYCLE				
t_{RC}	Read cycle time	55	–	ns
t_{AA}	Address to data valid	–	55	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[13]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[13, 14]	–	20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[13]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[13, 14]	–	20	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down	–	55	ns
t_{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to data valid	–	55	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to Low Z[13]	10	–	ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z[13, 14]	–	20	ns
WRITE CYCLE[15, 16]				
t_{WC}	Write cycle time	55	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	40	–	ns
t_{AW}	Address set-up to write end	40	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address set-up to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	40	–	ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to write end	40	–	ns
t_{SD}	Data set-up to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[13, 14]	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[13]	10	–	ns

Notes

10. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.
11. $\overline{CE}$ is the logical combination of $\overline{CE_1}$ and CE_2. When $\overline{CE_1}$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE_1}$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
12. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 ns/V, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the “AC Test Loads and Waveforms” section.
13. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
14. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
15. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
16. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms[17]

Figure 2. Read Cycle 1 (Address Transition Controlled)[18, 19]

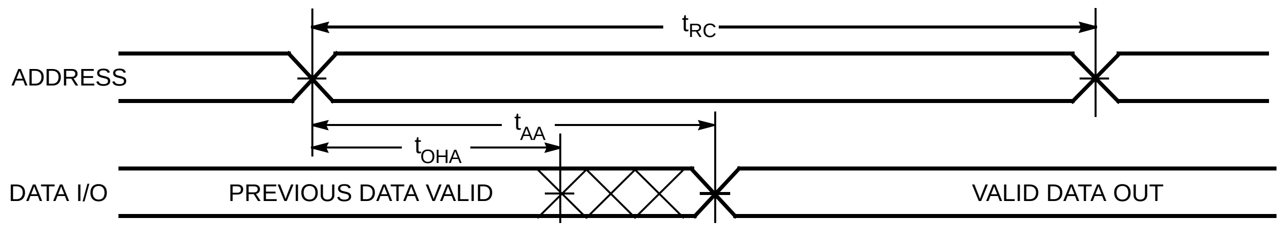
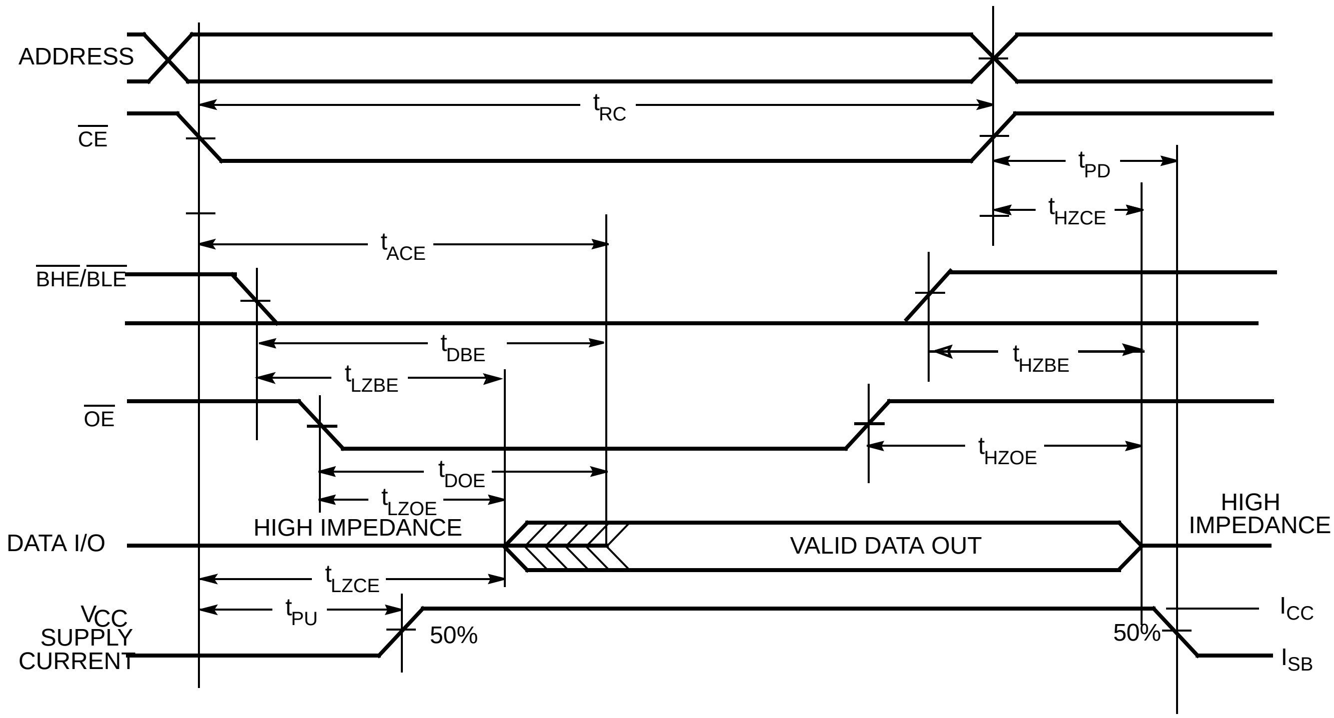


Figure 3. Read Cycle 2 (OE Controlled)[19, 20, 21]



Notes

17. All Read/Write switching waveforms are shown for 16-bit data transactions only.
18. The device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$.
19. $\overline{WE}$ is HIGH for read cycle.
20. Address valid prior to or coincident with $\overline{CE}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW.
21. $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.

Switching Waveforms[17] (continued)

Figure 4. Write Cycle 1 ($\overline{WE}$ Controlled)[22, 23, 24, 25, 26]

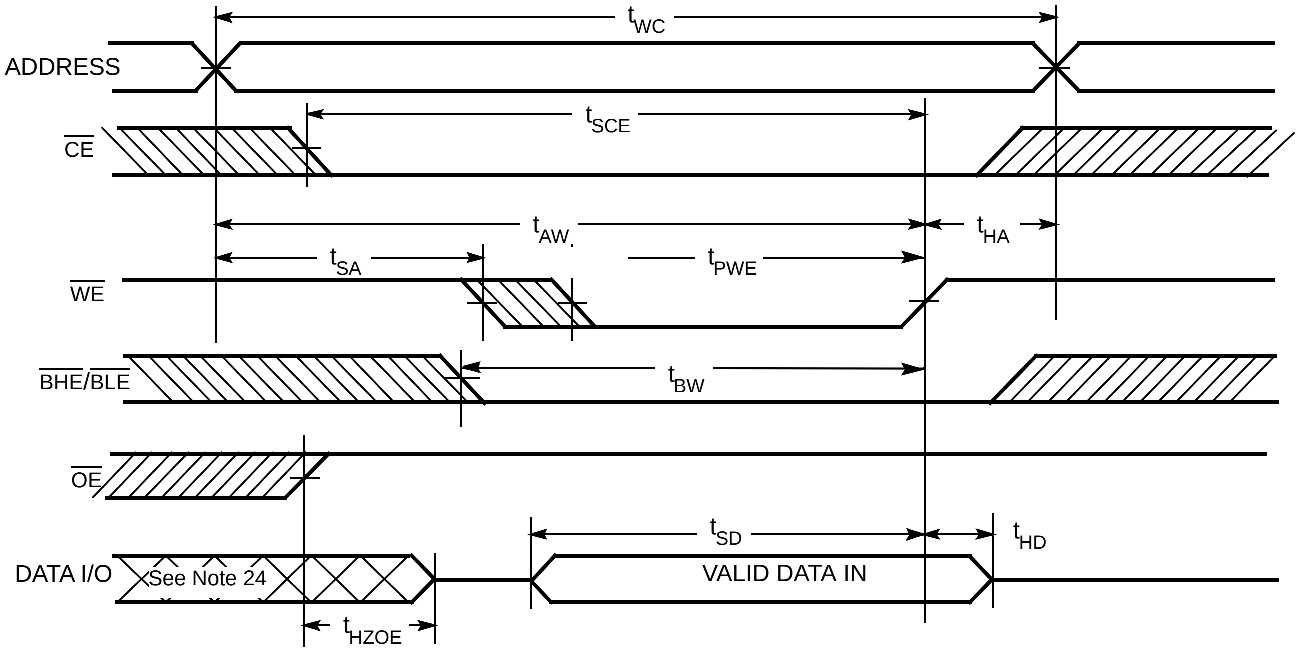
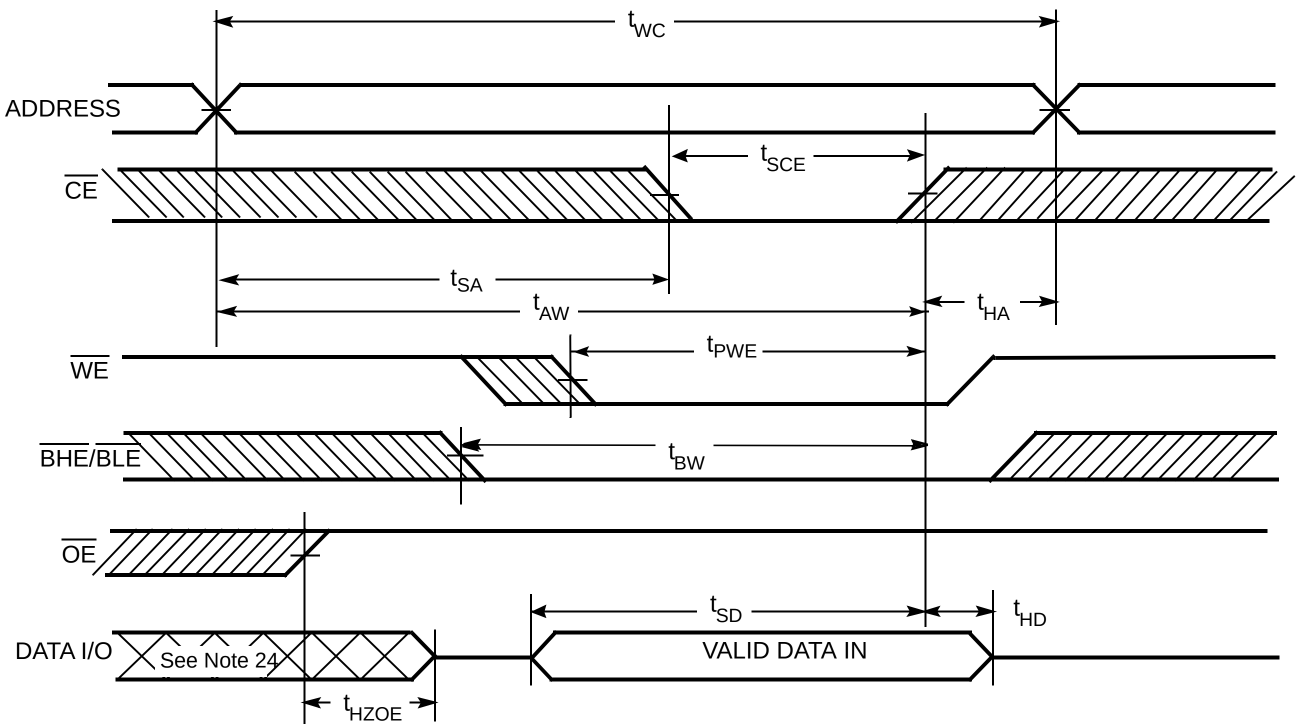


Figure 5. Write Cycle 2 ($\overline{CE}$ Controlled)[22, 23, 24, 25, 26]



Notes

22. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
23. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high-impedance state.
24. During this period, the I/Os are in output state and input signals should not be applied.
25. $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
26. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms[17] (continued)

Figure 6. Write Cycle 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[27, 28, 29, 30]

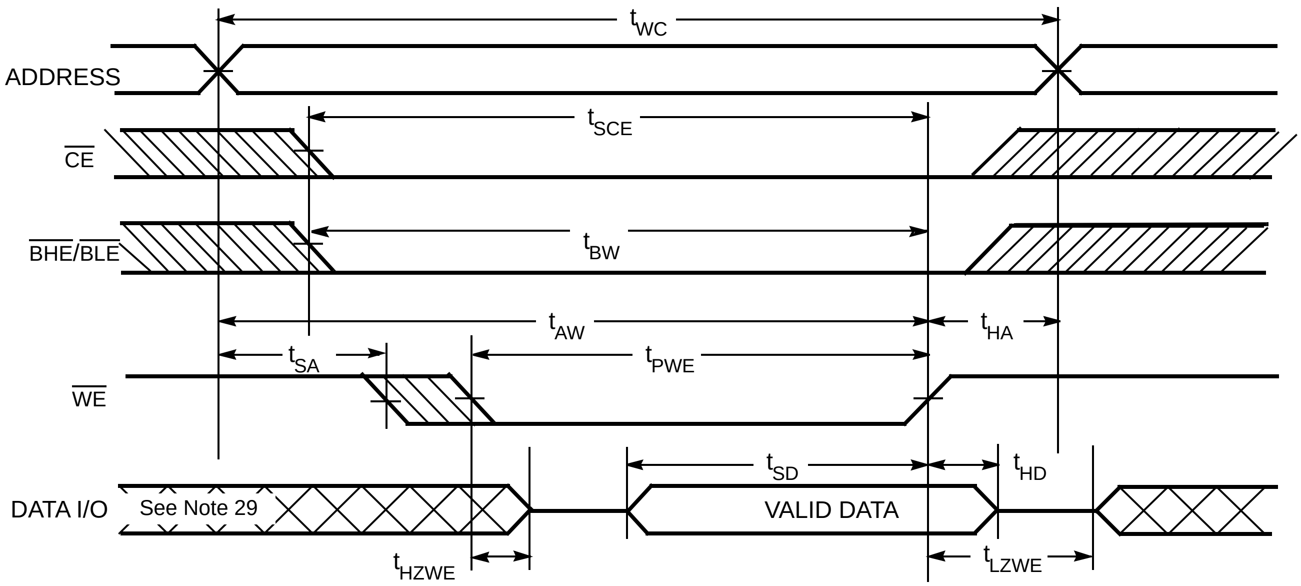
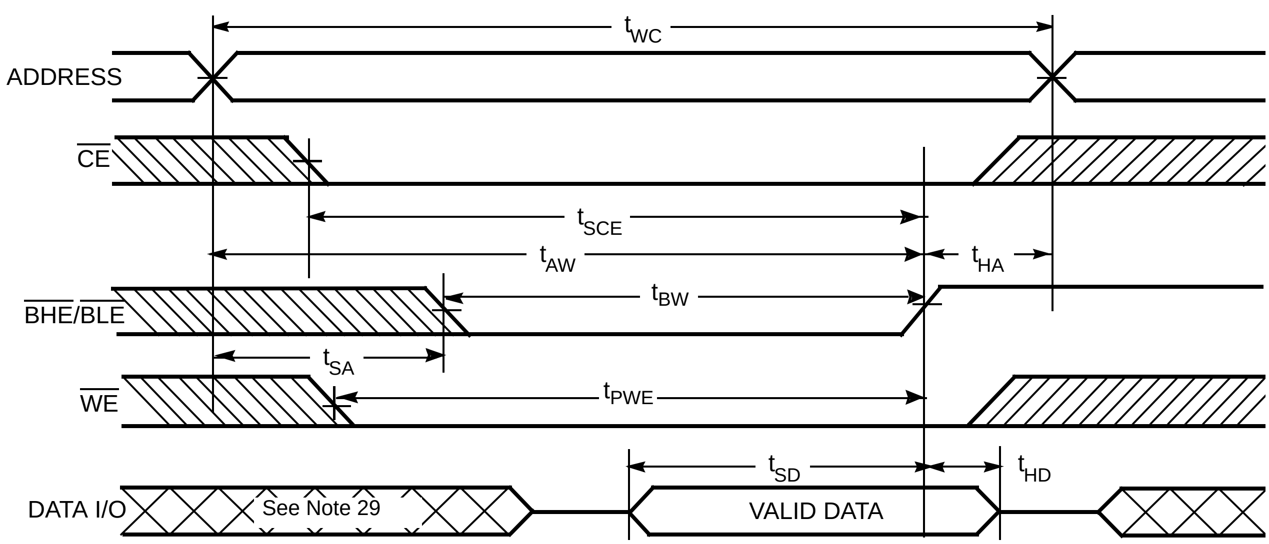


Figure 7. Write Cycle 4 ($\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW)[27, 28, 29]



Notes

27. $\overline{CE}$ is the logical combination of $\overline{CE_1}$ and CE_2. When $\overline{CE_1}$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE_1}$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
28. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high-impedance state.
29. During this period, the I/Os are in output state and input signals should not be applied.
30. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.

Truth Table

$\overline{CE}_1$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/power-down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect/power-down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect/power-down	Standby (I_{SB})
L	H	H	L	L	L	Data out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data out (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	High Z (I/O_0–I/O_7); Data Out (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	L	X	L	L	Data in (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data in (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	High Z (I/O_0–I/O_7); Data in (I/O_8–I/O_{15})	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62177DV30LL-55BAXI	51-85191	48-ball FBGA (8 mm × 9.5 mm × 1.2 mm) (Pb-free)	Industrial

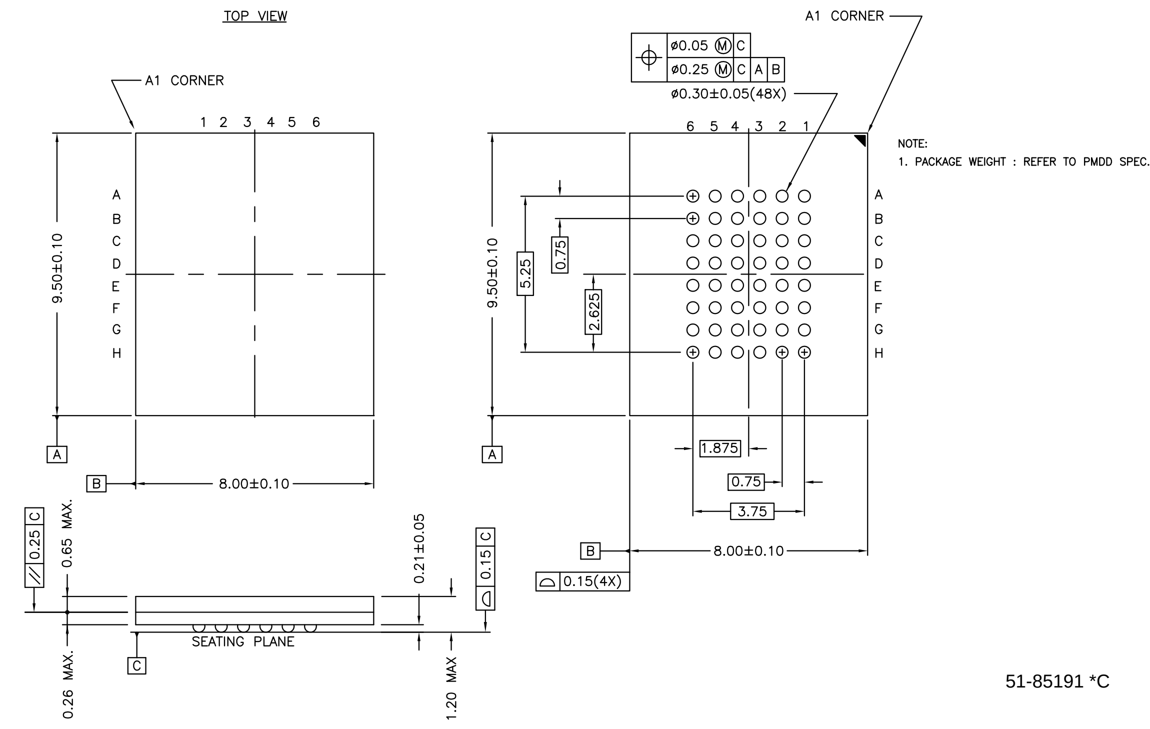
Ordering Code Definitions

CY 621 7 7D V30 LL 55 BAX I

- I: Temperature Grade
  I = Industrial
- BAX: Package Type = BAX :48-ball FBGA (Pb-free)
- 55: Speed Grade = 55ns
- LL: Low Power
- V30: Voltage Range (3 V Typical)
- 7D: Bus Width = X16
  D = 130nm Technology
- 7: Density = 32 Mbit
- 621: MoBL SRAM Family
- CY: Company ID: CY = Cypress

Package Diagram

Figure 8. 48 ball FBGA (8 × 9.5 × 1.2 mm) (51-85191)



Reference Information

Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
I/O	input/output
SRAM	static random access memory
FBGA	fine ball grid array

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
μA	microampere
mA	milliampere
MHz	megahertz
ns	nanosecond
pF	picofarad
V	volt
Ω	ohm
W	watt

Document History Page

Document Title: CY62177DV30 MoBL® 32-Mbit (2 M × 16) Static RAM Document #: 38-05633				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	251075	AJU	See ECN	New Datasheet
*A	330363	AJU	See ECN	Changed title of data sheet from CYM62177DV30 to CY62177DV30 Added second chip enable (CE_2) Added footnote #12 on page 5
*B	400960	NXR	See ECN	Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Changed I_{SB1} from 60 and 40 μA to 100 μA for the L and LL versions for both the 55 and the 70 ns speed bins respectively.
*C	469187	NXR	See ECN	Converted from Preliminary to Final Changed the $I_{SB2(Max)}$ from 40 μA to 50 μA for LL version of both 45 ns and 55 ns speed bins Changed the $I_{CCDR(Max)}$ from 20 μA to 25 μA for LL version Updated the Ordering Information table
*D	2896036	AJU	03/19/10	Removed inactive parts from Ordering Information. Updated package diagram. Updated links in Sales, Solutions, and Legal Information.
*E	3153110	RAME	01/25/2011	Updated datasheet as per template Removed CY62177DV30L related info Removed 70 ns speed bin related info Added Ordering Code Definitions Added Reference Information and Units of Measure table
*F	3329873	RAME	07/27/11	Removed footnote # 8 and its reference because of single package availability. Updated template and styles according to current Cypress standards. Added acronyms and units. Removed reference to AN1064 SRAM system guidelines.
*G	3685455	MEMJ	07/20/2012	Added Note 16. Updated text in Switching Waveforms diagrams. Updated Package Diagram.
*H	4576526	MEMJ	11/21/2014	Added related documentation hyperlink in page 1. Updated Figure 8 in Package Diagram (spec 51-85191 *B to *C). Added Note 16 in Switching Characteristics Over the Operating Range. Added note reference 16 in the Switching Characteristics table. Added Note 30 in Switching Waveforms[17]. Added note reference 30 in Figure 6.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 5