Features

- **EE Programmable 65,536 x 1-, 131,072 x 1-, 262,144 x 1-, 524,288 x 1-, 1,048,576 x 1-, 2,097,152 x 1-, and 4,194,304 x 1-bit Serial Memories Designed to Store Configuration Programs for Field Programmable Gate Arrays (FPGAs)**
- **Supports both 3.3V and 5.0V Operating Voltage Applications**
- **In-System Programmable (ISP) via Two-Wire Bus**
- **Simple Interface to SRAM FPGAs**
- **Compatible with Atmel AT6000, AT40K and AT94K Devices, Altera® FLEX®, APEX™ Devices, ORCA®, Xilinx® XC3000, XC4000, XC5200, Spartan®, Virtex™ FPGAs**
- **Cascadable Read-back to Support Additional Configurations or Higher-density Arrays**
- **Very Low-power CMOS EEPROM Process**
- **Programmable Reset Polarity**
- **Available in 6 mm x 6 mm x 1 mm 8-lead LAP (Pin-compatible with 8-lead SOIC/VOIC Packages), 8-lead PDIP, 8-lead SOIC, 20-lead PLCC, 20-lead SOIC, 44-lead PLCC and 44-lead TQFP Packages**
- **Emulation of Atmel's AT24CXXX Serial EEPROMs**
- **Low-power Standby Mode**
- **High-reliability**
  - **Endurance: 100,000 Write Cycles**
  - **Data Retention: 90 Years for Industrial Parts (at 85°C) and 190 Years for Commercial Parts (at 70°C)**
- **Green (Pb/Halide-free/RoHS Compliant) Package Options Available**

1. Description

The AT17LV series FPGA Configuration EEPROMs (Configurators) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. The AT17LV series device is packaged in the 8-lead LAP, 8-lead PDIP, 8-lead SOIC, 20-lead PLCC, 20-lead SOIC, 44-lead PLCC and 44-lead TQFP, see Table 1-1. The AT17LV series Configurators uses a simple serial-access procedure to configure one or more FPGA devices. The user can select the polarity of the reset function by programming four EEPROM bytes. These devices also support a write-protection mechanism within its programming mode.

The AT17LV series configurators can be programmed with industry-standard programmers, Atmel's ATDH2200E Programming Kit or Atmel's ATDH2225 ISP Cable.

FPGA Configuration EEPROM Memory

AT17LV65
AT17LV128
AT17LV256
AT17LV512
AT17LV010
AT17LV002
AT17LV040

3.3V and 5V System Support

2321H–CNFG–03/06

Table 1-1. AT17LV Series Packages

Package	AT17LV65/ AT17LV128/ AT17LV256	AT17LV512/ AT17LV010	AT17LV002	AT17LV040
8-lead LAP	Yes	Yes	Yes	(3)
8-lead PDIP	Yes	Yes	–	–
8-lead SOIC	Yes	Use 8-lead LAP(1)	Use 8-lead LAP(1)	(3)
20-lead PLCC	Yes	Yes	Yes	–
20-lead SOIC	Yes(2)	Yes(2)	Yes(2)	–
44-lead PLCC	–	–	Yes	Yes
44-lead TQFP	–	–	Yes	Yes

Notes:
1. The 8-lead LAP package has the same footprint as the 8-lead SOIC. Since an 8-lead SOIC package is not available for the AT17LV512/010/002 devices, it is possible to use an 8-lead LAP package instead.
2. The pinout for the AT17LV65/128/256 devices is not pin-for-pin compatible with the AT17LV512/010/002 devices.
3. Refer to the AT17Fxxx datasheet, available on the Atmel web site.

2. Pin Configuration

Figure 2-1. 8-lead LAP

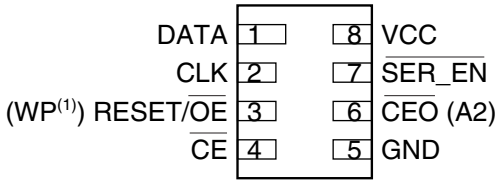


Figure 2-2. 8-lead SOIC

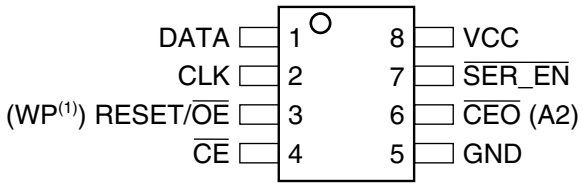


Figure 2-3. 8-lead PDIP

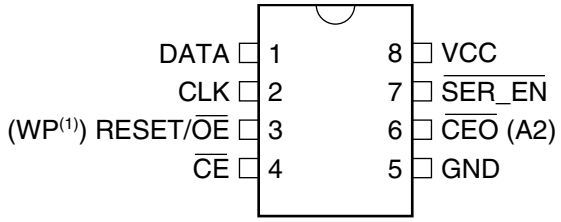
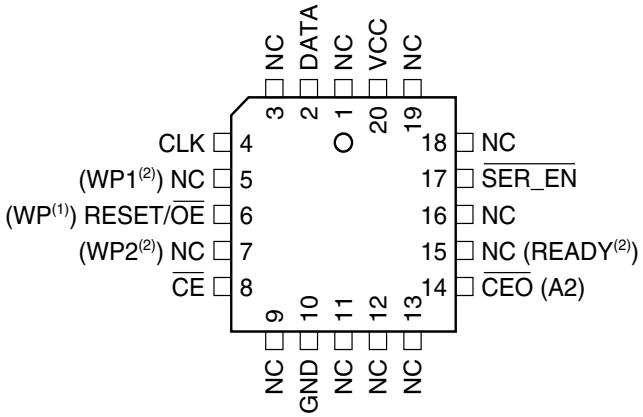
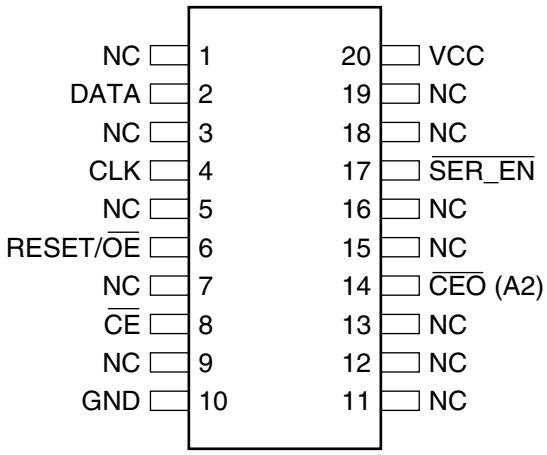


Figure 2-4. 20-lead PLCC



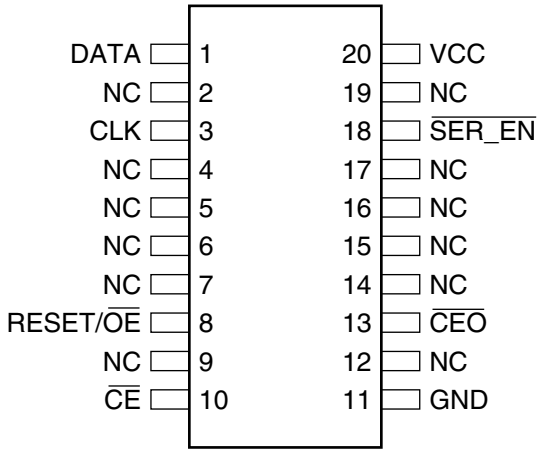
Notes: 1. This pin is only available on AT17LV65/128/256 devices.
2. This pin is only available on AT17LV512/010/002 devices.
3. The $\overline{CEO}$ feature is not available on the AT17LV65 device.

Figure 2-5. 20-lead SOIC[1]



Note: 1. This pinout only applies to AT17LV65/128/256 devices.

Figure 2-6. 20-lead SOIC[1]



Notes: 1. This pinout only applies to AT17LV512/010/002 devices.
2. The CEO feature is not available on the AT17LV65 device.

Figure 2-7. 44 PLCC

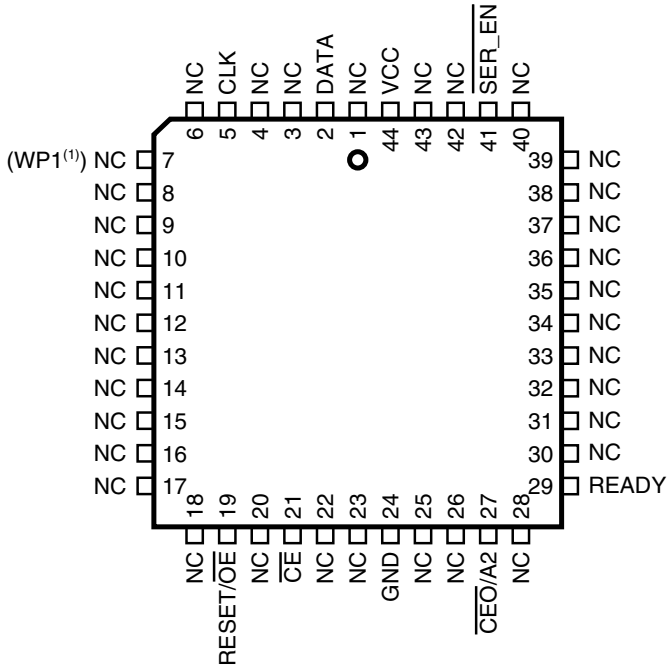
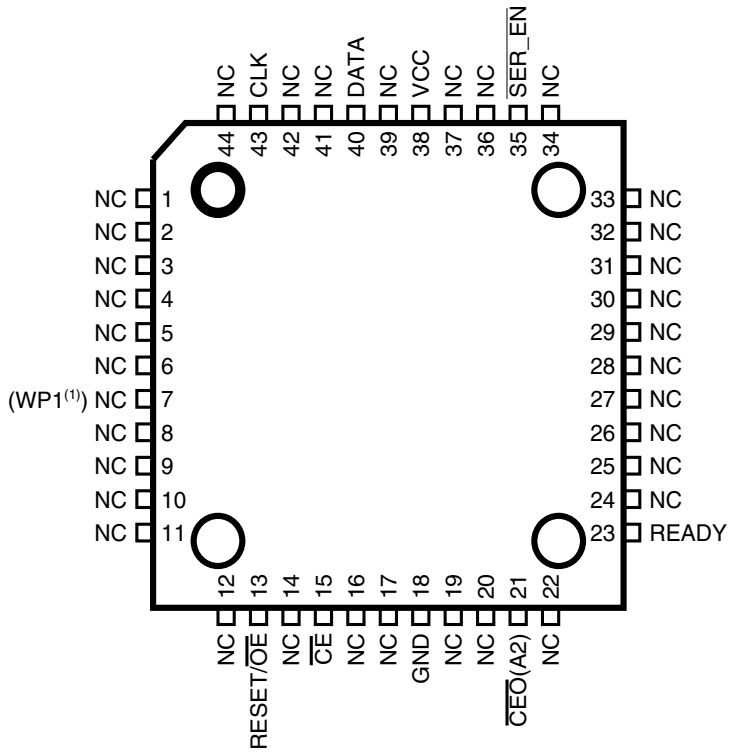
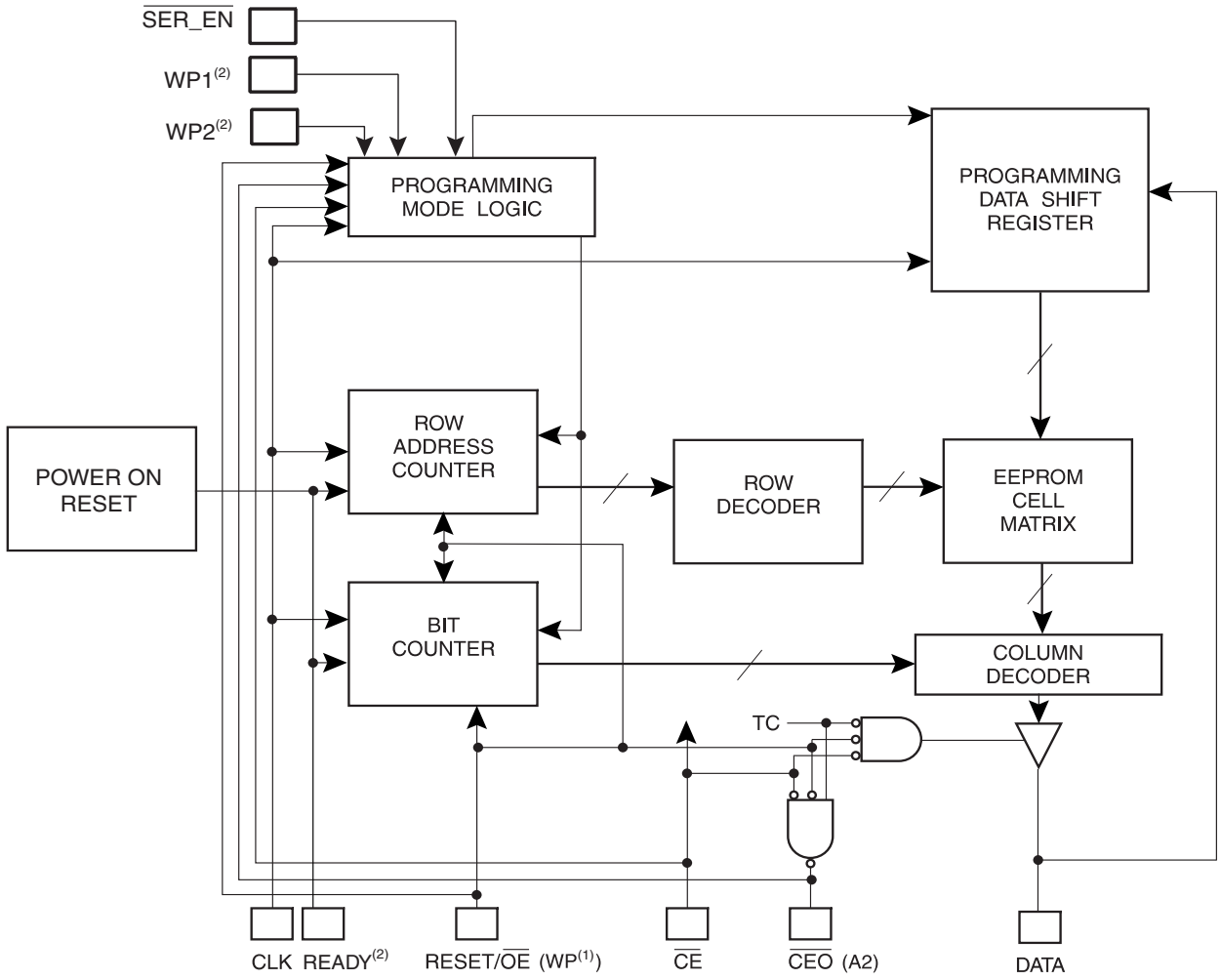


Figure 2-8. 44 TQFP



Note: 1. This pin is only available on AT17LV002 devices.

Figure 2-9. Block Diagram



Notes: 1. This pin is only available on AT17LV65/128/256 devices.
2. This pin is only available on AT17LV512/010/002 devices.
3. The $\overline{CEO}$ feature is not available on the AT17LV65 device.

3. Device Description

The control signals for the configuration EEPROM ($\overline{CE}$, RESET/$\overline{OE}$ and CCLK) interface directly with the FPGA device control signals. All FPGA devices can control the entire configuration process and retrieve data from the configuration EEPROM without requiring an external intelligent controller.

The configuration EEPROM RESET/$\overline{OE}$ and $\overline{CE}$ pins control the tri-state buffer on the DATA output pin and enable the address counter. When RESET/$\overline{OE}$ is driven High, the configuration EEPROM resets its address counter and tri-states its DATA pin. The $\overline{CE}$ pin also controls the output of the AT17LV series configurator. If $\overline{CE}$ is held High after the RESET/$\overline{OE}$ reset pulse, the counter is disabled and the DATA output pin is tri-stated. When $\overline{OE}$ is subsequently driven Low, the counter and the DATA output pin are enabled. When RESET/$\overline{OE}$ is driven High again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of $\overline{CE}$.

When the configurator has driven out all of its data and $\overline{CEO}$ is driven Low, the device tri-states the DATA pin to avoid contention with other configurators. Upon power-up, the address counter is automatically reset.

This is the default setting for the device. Since almost all FPGAs use RESET Low and OE High, this document will describe $\overline{RESET}$/OE.

4. Pin Description

		AT17LV65/ AT17LV128/ AT17LV256			AT17LV512/ AT17LV010			AT17LV002					AT17LV040	
Name	I/O	8 DIP/ LAP/ SOIC	20 PLCC	20 SOIC	8 DIP/ LAP	20 PLCC	20 SOIC	8 DIP/ LAP/ SOIC	20 PLCC	20 SOIC	44 PLCC	44 TQFP	44 PLCC	44 TQFP
DATA	I/O	1	2	2	1	2	1	1	2	1	2	40	2	40
CLK	I	2	4	4	2	4	3	2	4	3	5	43	5	43
WP1	I	–	–	–	–	5	–	–	5	–	–	–	–	–
RESET/OE	I	3	6	6	3	6	8	3	6	8	19	13	19	13
WP2	I				–	7	–	–	7	–	–	–	–	–
$\overline{CE}$	I	4	8	8	4	8	10	4	8	10	21	15	21	15
GND		5	10	10	5	10	11	5	10	11	24	18	24	18
$\overline{CEO}$	O	6	14	14	6	14	13	6	14	13	27	21	27	21
A2	I						–			–				
READY	O	–	–	–	–	15	–	–	15	–	29	23	29	23
$\overline{SER\_EN}$	I	7	17	17	7	17	18	7	17	18	41	35	41	35
V_{CC}		8	20	20	8	20	20	8	20	20	44	38	44	38

Note: 1. The $\overline{CEO}$ feature is not available on the AT17LV65 device.

4.1 DATA

Three-state DATA output for configuration. Open-collector bi-directional pin for programming.

4.2 CLK

Clock input. Used to increment the internal address and bit counter for reading and programming.

4.3 WP1

WRITE PROTECT (1). Used to protect portions of memory during programming. Disabled by default due to internal pull-down resistor. This input pin is not used during FPGA loading operations. This pin is only available on AT17LV512/010/002 devices.

4.4 RESET/$\overline{OE}$

Output Enable (active High) and RESET (active Low) when $\overline{SER\_EN}$ is High. A Low level on $\overline{RESET}/\overline{OE}$ resets both the address and bit counters. A High level (with $\overline{CE}$ Low) enables the data output driver. The logic polarity of this input is programmable as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE. For most applications, RESET should be programmed active Low. This document describes the pin as $\overline{RESET}/\overline{OE}$.

4.5 WP

Write protect (WP) input (when $\overline{CE}$ is Low) during programming only ($\overline{SER\_EN}$ Low). When WP is Low, the entire memory can be written. When WP is enabled (High), the lowest block of the memory cannot be written. This pin is only available on AT17LV65/128/256 devices.

4.6 WP2

WRITE PROTECT (2). Used to protect portions of memory during programming. Disabled by default due to internal pull-down resistor. This input pin is not used during FPGA loading operations. This pin is only available on AT17LV512/010 devices.

4.7 $\overline{CE}$

Chip Enable input (active Low). A Low level (with OE High) allows CLK to increment the address counter and enables the data output driver. A High level on $\overline{CE}$ disables both the address and bit counters and forces the device into a low-power standby mode. Note that this pin will *not* enable/disable the device in the Two-Wire Serial Programming mode ($\overline{SER\_EN}$ Low).

4.8 GND

Ground pin. A 0.2 µF decoupling capacitor between V_{CC} and GND is recommended.

4.9 CEO

Chip Enable Output (active Low). This output goes Low when the address counter has reached its maximum value. In a daisy chain of AT17LV series devices, the $\overline{CEO}$ pin of one device must be connected to the $\overline{CE}$ input of the next device in the chain. It will stay Low as long as $\overline{CE}$ is Low and OE is High. It will then follow CE until OE goes Low; thereafter, $\overline{CEO}$ will stay High until the entire EEPROM is read again. This $\overline{CEO}$ feature is not available on the AT17LV65 device.

4.10 A2

Device selection input, A2. This is used to enable (or select) the device during programming (i.e., when $\overline{\text{SER\_EN}}$ is Low). A2 has an internal pull-down resistor.

4.11 READY

Open collector reset state indicator. Driven Low during power-up reset, released when power-up is complete. It is recommended to use a 4.7 kΩ pull-up resistor when this pin is used.

4.12 $\overline{\text{SER\_EN}}$

Serial enable must be held High during FPGA loading operations. Bringing $\overline{\text{SER\_EN}}$ Low enables the Two-Wire Serial Programming Mode. For non-ISP applications, $\overline{\text{SER\_EN}}$ should be tied to V_{CC}.

4.13 V_{CC}

3.3V (±10%) and 5.0V (±5% Commercial, ±10% Industrial) power supply pin.

5. FPGA Master Serial Mode Summary

The I/O and logic functions of any SRAM-based FPGA are established by a configuration program. The program is loaded either automatically upon power-up, or on command, depending on the state of the FPGA mode pins. In Master mode, the FPGA automatically loads the configuration program from an external memory. The AT17LV Serial Configuration EEPROM has been designed for compatibility with the Master Serial mode.

This document discusses the Atmel AT40K, AT40KAL and AT94KAL applications as well as Xilinx applications.

6. Control of Configuration

Most connections between the FPGA device and the AT17LV Serial EEPROM are simple and self-explanatory.

- The DATA output of the AT17LV series configurator drives DIN of the FPGA devices.
- The master FPGA CCLK output drives the CLK input of the AT17LV series configurator.
- The $\overline{\text{CEO}}$ output of any AT17LV series configurator drives the $\overline{\text{CE}}$ input of the next configurator in a cascaded chain of EEPROMs.
- $\overline{\text{SER\_EN}}$ must be connected to V_{CC} (except during ISP).
- The READY[1] pin is available as an open-collector indicator of the device's reset status; it is driven Low while the device is in its power-on reset cycle and released (tri-stated) when the cycle is complete.

Note: 1. This pin is not available for the AT17LV65/128/256 devices.

7. Cascading Serial Configuration EEPROMs

For multiple FPGAs configured as a daisy-chain, or for FPGAs requiring larger configuration memories, cascaded configurators provide additional memory.

After the last bit from the first configurator is read, the clock signal to the configurator asserts its $\overline{CEO}$ output Low and disables its DATA line driver. The second configurator recognizes the Low level on its $\overline{CE}$ input and enables its DATA output.

After configuration is complete, the address counters of all cascaded configurators are reset if the $\overline{RESET}$/OE on each configurator is driven to its active (Low) level.

If the address counters are not to be reset upon completion, then the $\overline{RESET}$/OE input can be tied to its inactive (High) level.

The AT17LV65 devices do not have the $\overline{CEO}$ feature to perform cascaded configurations.

8. AT17LV Series Reset Polarity

The AT17LV series configurator allows the user to program the reset polarity as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE. This feature is supported by industry-standard programmer algorithms.

9. Programming Mode

The programming mode is entered by bringing $\overline{SER\_EN}$ Low. In this mode the chip can be programmed by the Two-Wire serial bus. The programming is done at V_{CC} supply only. Programming super voltages are generated inside the chip.

10. Standby Mode

The AT17LV series configurators enter a low-power standby mode whenever $\overline{CE}$ is asserted High. In this mode, the AT17LV65/128/256 configurator consumes less than 50 µA of current at 3.3V (100 µA for the AT17LV512/010 and 200 µA for the AT17LV002/040). The output remains in a high-impedance state regardless of the state of the $\overline{OE}$ input.

11. Absolute Maximum Ratings*

Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to V_{CC} +0.5V
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	260°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

12. Operating Conditions

Symbol	Description		3.3V		5V		Units
			Min	Max	Min	Max	
V_{CC}	Commercial	Supply voltage relative to GND -0°C to +70°C	3.0	3.6	4.75	5.25	V
	Industrial	Supply voltage relative to GND -40°C to +85°C	3.0	3.6	4.5	5.5	V

13. DC Characteristics

V_{CC} = 3.3V ± 10%

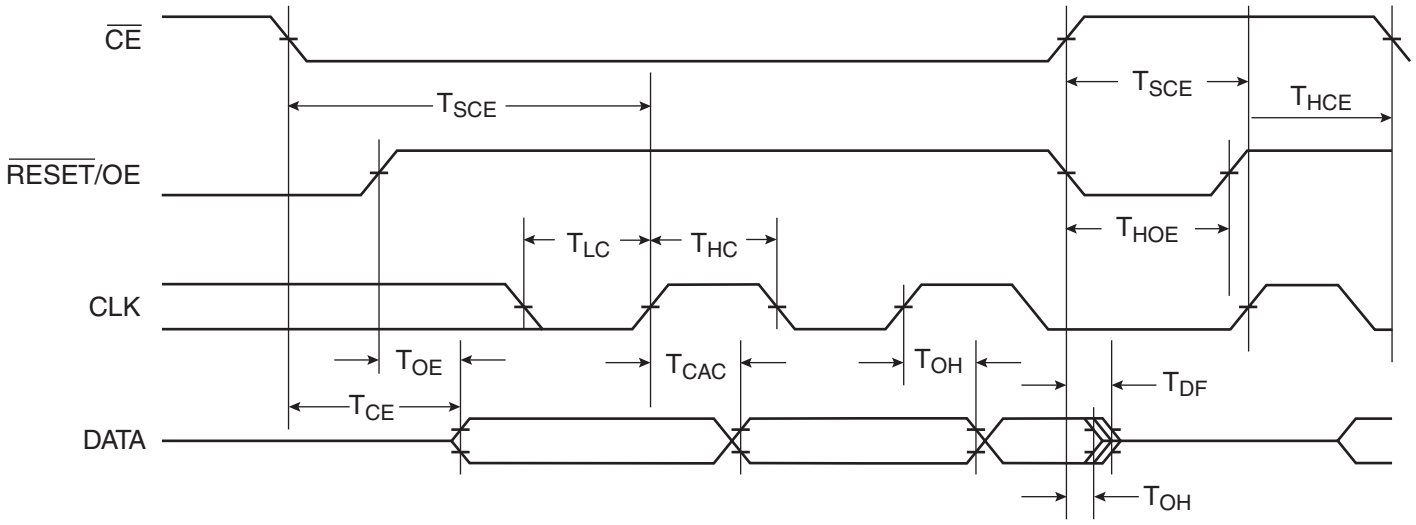
Symbol	Description		AT17LV65/ AT17LV128/ AT17LV256		AT17LV512/ AT17LV010		AT17LV002/ AT17LV040		Units
			Min	Max	Min	Max	Min	Max	
V_{IH}	High-level Input Voltage		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Low-level Input Voltage		0	0.8	0	0.8	0	0.8	V
V_{OH}	High-level Output Voltage (I_{OH} = -2.5 mA)	Commercial	2.4		2.4		2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)			0.4		0.4		0.4	V
V_{OH}	High-level Output Voltage (I_{OH} = -2 mA)	Industrial	2.4		2.4		2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)			0.4		0.4		0.4	V
I_{CCA}	Supply Current, Active Mode			5		5		5	mA
I_L	Input or Output Leakage Current (V_{IN} = V_{CC} or GND)		-10	10	-10	10	-10	10	µA
I_{CCS}	Supply Current, Standby Mode	Commercial		50		100		150	µA
		Industrial		100		100		150	µA

14. DC Characteristics

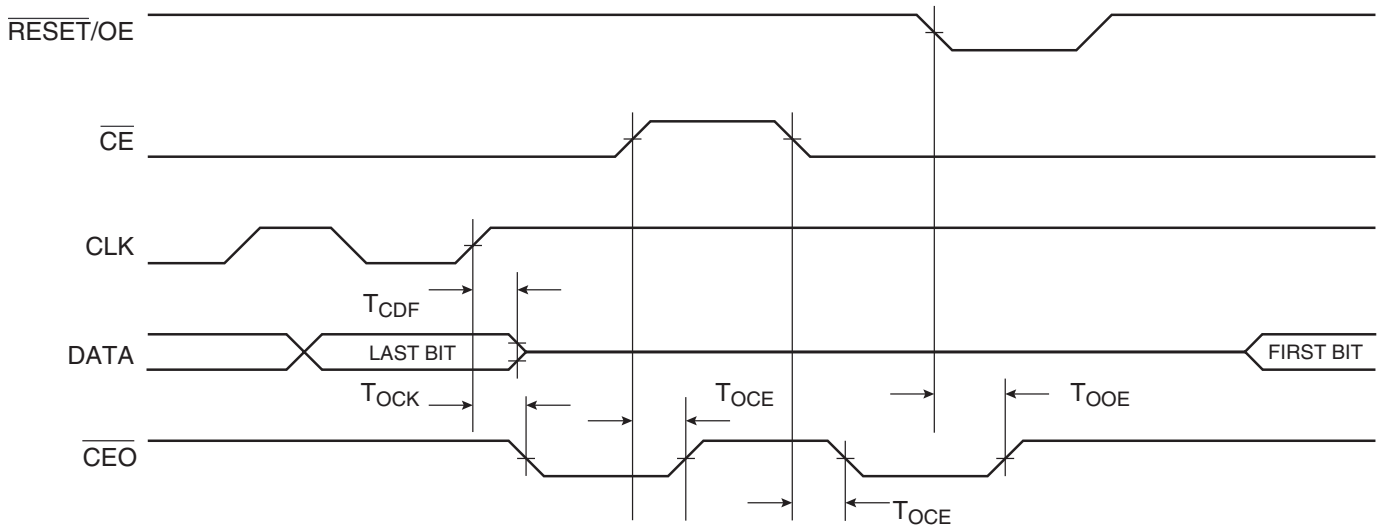
V_{CC} = 5V ± 5% Commercial; V_{CC} = 5V ± 10% Industrial

Symbol	Description		AT17LV65/ AT17LV128/ AT17LV256		AT17LV512/ AT17LV010		AT17LV002/ AT17LV040		Units
			Min	Max	Min	Max	Min	Max	
V_{IH}	High-level Input Voltage		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Low-level Input Voltage		0	0.8	0	0.8	0	0.8	V
V_{OH}	High-level Output Voltage (I_{OH} = -2.5 mA)	Commercial	3.7		3.86		3.86		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)			0.32		0.32		0.32	V
V_{OH}	High-level Output Voltage (I_{OH} = -2 mA)	Industrial	3.6		3.76		3.76		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)			0.37		0.37		0.37	V
I_{CCA}	Supply Current, Active Mode			10		10		10	mA
I_L	Input or Output Leakage Current (V_{IN} = V_{CC} or GND)		-10	10	-10	10	-10	10	µA
I_{CCS}	Supply Current, Standby Mode	Commercial		75		200		350	µA
		Industrial		150		200		350	µA

15. AC Waveforms



16. AC Waveforms when Cascading



17. AC Characteristics

V_{CC} = 3.3V ± 10%

Symbol	Description	AT17LV65/128/256				AT17LV512/010/002/040				Units
		Commercial		Industrial		Commercial		Industrial		
		Min	Max	Min	Max	Min	Max	Min	Max	
T_{OE}[1]	OE to Data Delay		50		55		50		55	ns
T_{CE}[1]	$\overline{CE}$ to Data Delay		60		60		55		60	ns
T_{CAC}[1]	CLK to Data Delay		75		80		55		60	ns
T_{OH}	Data Hold from $\overline{CE}$, OE, or CLK	0		0		0		0		ns
T_{DF}[2]	$\overline{CE}$ or OE to Data Float Delay		55		55		50		50	ns
T_{LC}	CLK Low Time	25		25		25		25		ns
T_{HC}	CLK High Time	25		25		25		25		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	35		60		30		35		ns
T_{HCE}	$\overline{CE}$ Hold Time from CLK (to guarantee proper counting)	0		0		0		0		ns
T_{HOE}	OE High Time (guarantees counter is reset)	25		25		25		25		ns
F_{MAX}	Maximum Clock Frequency		10		10		15		10	MHz

Notes: 1. AC test lead = 50 pF.

2. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

18. AC Characteristics when Cascading

V_{CC} = 3.3V ± 10%

Symbol	Description	AT17LV65/128/256				AT17LV512/010/002/040				Units
		Commercial		Industrial		Commercial		Industrial		
		Min	Max	Min	Max	Min	Max	Min	Max	
T_{CDF}[2]	CLK to Data Float Delay		60		60		50		50	ns
T_{OCK}[1]	CLK to $\overline{CEO}$ Delay		55		60		50		55	ns
T_{OCE}[1]	$\overline{CE}$ to $\overline{CEO}$ Delay		55		60		35		40	ns
T_{OOE}[1]	$\overline{RESET}$/OE to $\overline{CEO}$ Delay		40		45		35		35	ns
F_{MAX}	Maximum Clock Frequency		8		8		12.5		10	MHz

Notes: 1. AC test lead = 50 pF.

2. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

19. AC Characteristics

V_{CC} = 5V ± 5% Commercial; V_{CC} = 5V ± 10% Industrial

		AT17LV65/128/256				AT17LV512/010/002/040				
		Commercial		Industrial		Commercial		Industrial		
Symbol	Description	Min	Max	Min	Max	Min	Max	Min	Max	Units
T_{OE}[1]	OE to Data Delay		30		35		30		35	ns
T_{CE}[1]	$\overline{CE}$ to Data Delay		45		45		45		45	ns
T_{CAC}[1]	CLK to Data Delay		50		55		50		50	ns
T_{OH}	Data Hold from $\overline{CE}$, OE, or CLK	0		0		0		0		ns
T_{DF}[2]	$\overline{CE}$ or OE to Data Float Delay		50		50		50		50	ns
T_{LC}	CLK Low Time	20		20		20		20		ns
T_{HC}	CLK High Time	20		20		20		20		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	35		40		20		25		ns
T_{HCE}	$\overline{CE}$ Hold Time from CLK (to guarantee proper counting)	0		0		0		0		ns
T_{HOE}	OE High Time (guarantees counter is reset)	20		20		20		20		ns
F_{MAX}	Maximum Clock Frequency		12.5		12.5		15		15	MHz

Notes: 1. AC test lead = 50 pF.

2. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

20. AC Characteristics when Cascading

V_{CC} = 5V ± 5% Commercial; V_{CC} = 5V ± 10% Industrial

		AT17LV65/128/256				AT17LV512/010/002/040				
		Commercial		Industrial		Commercial		Industrial		
Symbol	Description	Min	Max	Min	Max	Min	Max	Min	Max	Units
T_{CDF}[2]	CLK to Data Float Delay		50		50		50		50	ns
T_{OCK}[1]	CLK to $\overline{CEO}$ Delay		35		40		35		40	ns
T_{OCE}[1]	$\overline{CE}$ to $\overline{CEO}$ Delay		35		35		35		35	ns
T_{OOE}[1]	$\overline{RESET}$/OE to $\overline{CEO}$ Delay		30		35		30		30	ns
F_{MAX}	Maximum Clock Frequency		10		10		12.5		12.5	MHz

Notes: 1. AC test lead = 50 pF.

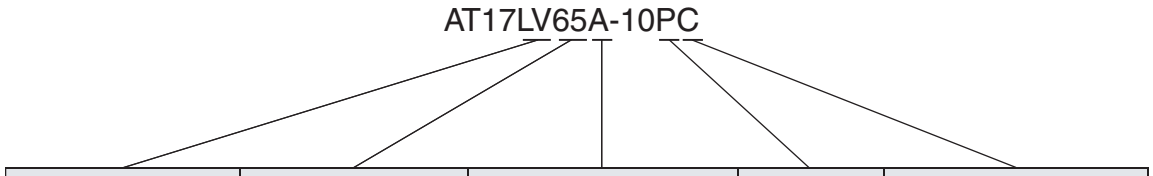
2. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

21. Thermal Resistance Coefficients[1]

Package Type			AT17LV65/ AT17LV128/ AT17LV256	AT17LV512/ AT17LV010	AT17LV002	AT17LV040
8CN 4	Leadless Array Package (LAP)	θ_{JC} [°C/W]	45	45	45	–
		θ_{JA} [°C/W][2]	115.71	135.71	159.60	–
8P3	Plastic Dual Inline Package (PDIP)	θ_{JC} [°C/W]	37	37	–	–
		θ_{JA} [°C/W][2]	107	107	–	–
8S1	Plastic Gull Wing Small Outline (SOIC)	θ_{JC} [°C/W]	45	–	–	–
		θ_{JA} [°C/W][2]	150	–	–	–
20J	Plastic Leaded Chip Carrier (PLCC)	θ_{JC} [°C/W]	35	35	35	–
		θ_{JA} [°C/W][2]	90	90	90	–
20S2	Plastic Gull Wing Small Outline (SOIC)	θ_{JC} [°C/W]				–
		θ_{JA} [°C/W][2]				–
44A	Thin Plastic Quad Flat Package (TQFP)	θ_{JC} [°C/W]	–	–	17	17
		θ_{JA} [°C/W][2]	–	–	62	62
44J	Plastic Leaded Chip Carrier (PLCC)	θ_{JC} [°C/W]	–	–	15	15
		θ_{JA} [°C/W][2]	–	–	50	50

Notes: 1. For more information refer to the “Thermal Characteristics of Atmel’s Packages”, available on the Atmel web site.
2. Airflow = 0 ft/min.

Figure 21-1. Ordering Code



Voltage	Size (Bits)	Special Pinouts	Package	Temperature
3.0V to 5.5V	65 = 65K 128 = 128K 256 = 256K 512 = 512K 010 = 1M 002 = 2M 040 = 4M	A = Altera Blank = Xilinx/Atmel/ Other	C = 8CN4 P = 8P3 N = 8S1 J = 20J S = 20S2 TQ = 44A BJ = 44J	C = Commercial I = Industrial U = Fully Green

Package Type	
8CN4	8-lead, 6 mm x 6 mm x 1 mm, Leadless Array Package (LAP) – Pin-compatible with 8-lead SOIC/VOID Packages
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
20J	20-lead, Plastic J-leaded Chip Carrier (PLCC)
20S2	20-lead, 0.300" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
44A	44-lead, Thin (1.0 mm) Plastic Quad Flat Package Carrier (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)

22. Ordering Information

22.1 Standard Package Options

Memory Size	Ordering Code	Package	Operation Range
64-Kbit[1]	AT17LV65-10CC	8CN4	Commercial (0°C to 70°C)
	AT17LV65-10PC	8P3	
	AT17LV65-10NC	8S1	
	AT17LV65-10JC	20J	
	AT17LV65-10SC	20S2	
	AT17LV65-10CI	8CN4	Industrial (-40°C to 85°C)
	AT17LV65-10PI	8P3	
	AT17LV65-10NI	8S1	
	AT17LV65-10JI	20J	
	AT17LV65-10SI	20S2	
128-Kbit[1]	AT17LV128-10CC	8CN4	Commercial (0°C to 70°C)
	AT17LV128-10PC	8P3	
	AT17LV128-10NC	8S1	
	AT17LV128-10JC	20J	
	AT17LV128-10SC	20S2	
	AT17LV128-10CI	8CN4	Industrial (-40°C to 85°C)
	AT17LV128-10PI	8P3	
	AT17LV128-10NI	8S1	
	AT17LV128-10JI	20J	
	AT17LV128-10SI	20S2	
256-Kbit[1]	AT17LV256-10CC	8CN4	Commercial (0°C to 70°C)
	AT17LV256-10PC	8P3	
	AT17LV256-10NC	8S1	
	AT17LV256-10JC	20J	
	AT17LV256-10SC	20S2	
	AT17LV256-10CI	8CN4	Industrial (-40°C to 85°C)
	AT17LV256-10PI	8P3	
	AT17LV256-10NI	8S1	
	AT17LV256-10JI	20J	
	AT17LV256-10SI	20S2	
512-Kbit[1]	AT17LV512-10CC	8CN4	Commercial (0°C to 70°C)
	AT17LV512-10PC	8P3	
	AT17LV512-10JC	20J	
	AT17LV512-10SC	20S2	
	AT17LV512-10CI	8CN4	Industrial (-40°C to 85°C)
	AT17LV512-10PI	8P3	
	AT17LV512-10JI	20J	
	AT17LV512-10SI	20S2	

22.1 Standard Package Options (Continued)

Memory Size	Ordering Code	Package	Operation Range
1-Mbit[1]	AT17LV010-10CC	8CN4	Commercial (0°C to 70°C)
	AT17LV010-10PC	8P3	
	AT17LV010-10JC	20J	
	AT17LV010-10SC	20S2	
	AT17LV010-10CI	8CN4	Industrial (-40°C to 85°C)
	AT17LV010-10PI	8P3	
	AT17LV010-10JI	20J	
	AT17LV010-10SI	20S2	
2-Mbit[1]	AT17LV002-10CC	8CN4	Commercial (0°C to 70°C)
	AT17LV002-10JC	20J	
	AT17LV002-10SC	20S2	
	AT17LV002-10TQC	44A	
	AT17LV002-10BJC	44J	
	AT17LV002-10CI	8CN4	Industrial (-40°C to 85°C)
	AT17LV002-10JI	20J	
	AT17LV002-10SI	20S2	
	AT17LV002-10TQI	44A	
	AT17LV002-10BJI	44J	
4-Mbit[1]	AT17LV040-10TQC AT17LV040-10BJC	44A 44J	Commercial (0°C to 70°C)
	AT17LV040-10TQI AT17LV040-10BJI	44A 44J	Industrial (-40°C to 85°C)

Notes: 1. For operating 5V operating voltage, please refer to the corresponding AC and DC Characteristics.

2. The last-time buy is April 11, 2006 for shaded parts.

3. For the -10CC and -10CI packages, customers may migrate to AT17LVXXX-10CU.

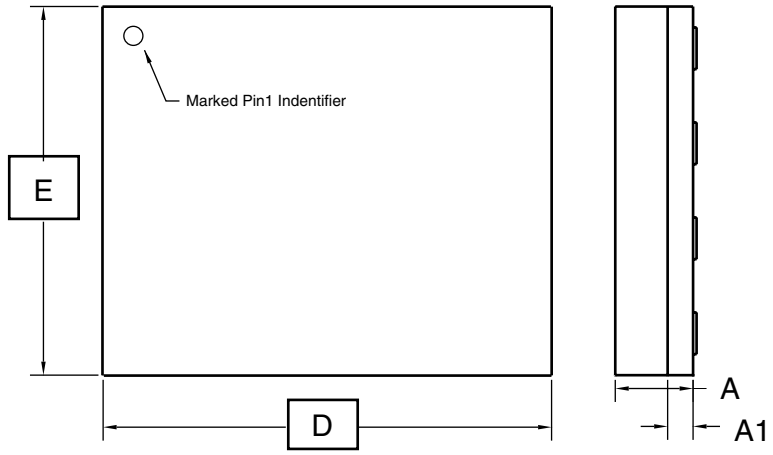
22.2 Green Package Options (Pb/Halide-free/RoHS Compliant)

Memory Size	Ordering Code	Package	Operation Range
256-Kbit[1]	AT17LV256-10CU	8CN4	Industrial (-40°C to 85°C)
	AT17LV256-10JU	20J	
	AT17LV256-10NU	8S1	
	AT17LV256-10PU	8P3	
	AT17LV256-10SU	20S2	
512-Kbit[1]	AT17LV512-10CU	8CN4	Industrial (-40°C to 85°C)
	AT17LV512-10JU	20J	
1-Mbit[1]	AT17LV010-10CU	8CN4	Industrial (-40°C to 85°C)
	AT17LV010-10JU	20J	
	AT17LV010-10PU	8P3	
2-Mbit[1]	AT17LV002-10CU	8CN4	Industrial (-40°C to 85°C)
	AT17LV002-10JU	20J	
	AT17LV002-10SU	20S2	
	AT17LV002-10TQU	44A	
4-Mbit[1]	AT17LV040-10TQU	44A	Industrial (-40°C to 85°C)

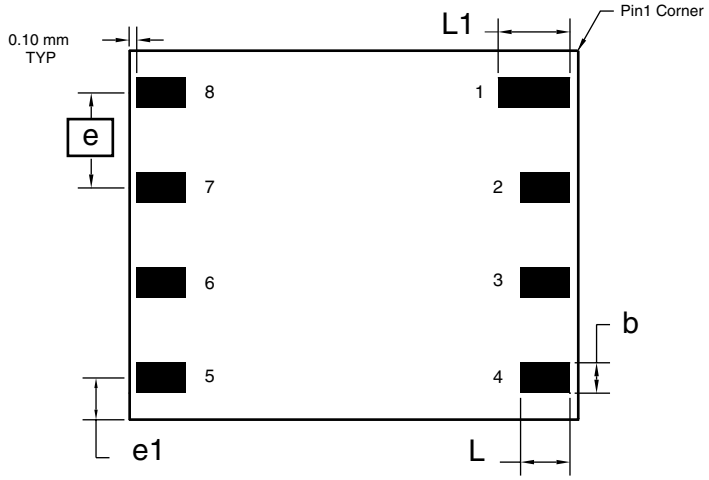
Note: 1. For operating 5V operating voltage, please refer to the corresponding AC and DC Characteristics.

23. Packaging Information

23.1 8CN4 – LAP



Top View Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

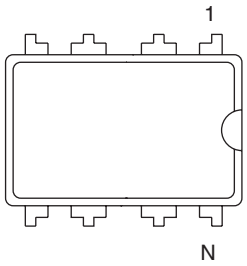
SYMBOL	MIN	NOM	MAX	NOTE
A	0.94	1.04	1.14	
A1	0.30	0.34	0.38	
b	0.45	0.50	0.55	1
D	5.89	5.99	6.09	
E	4.89	5.99	6.09	
e		1.27 BSC		
e1		1.10 REF		
L	0.95	1.00	1.05	1
L1	1.25	1.30	1.35	1

Note: 1. Metal Pad Dimensions.

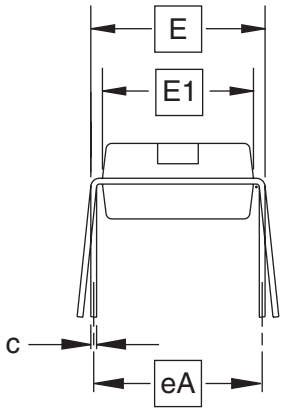
11/14/01

2325 Orchard Parkway San Jose, CA 95131	**TITLE** **8CN4**, 8-lead (6 x 6 x 1.04 mm Body), Lead Pitch 1.27 mm, Leadless Array Package (LAP)	**DRAWING NO.** 8CN4	**REV.** A

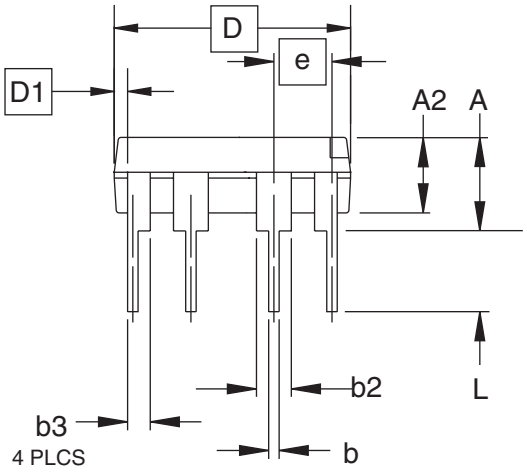
23.2 8P3 – PDIP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

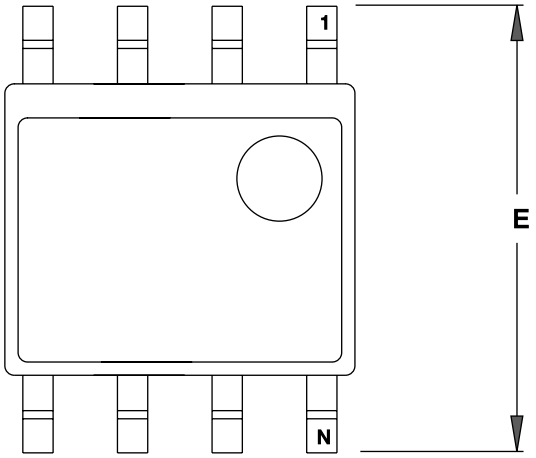
SYMBOL	MIN	NOM	MAX	NOTE
A			0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005			3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e	0.100 BSC			
eA	0.300 BSC			4
L	0.115	0.130	0.150	2

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

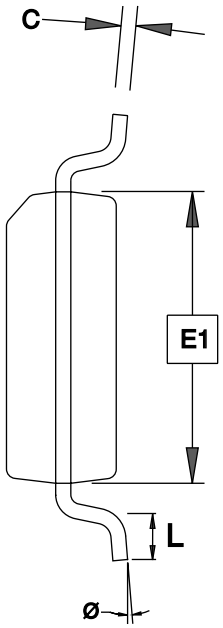
01/09/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8P3**, 8-lead, 0.300" Wide Body, Plastic Dual In-line Package (PDIP)	8P3	B

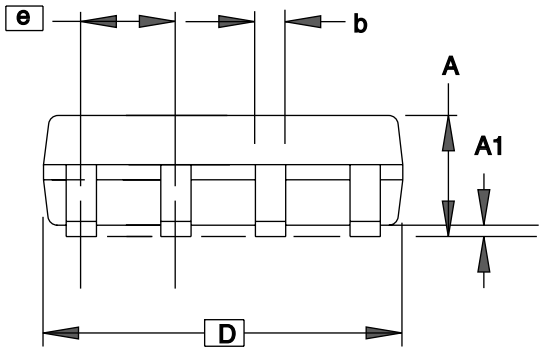
23.3 8S1 – SOIC



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

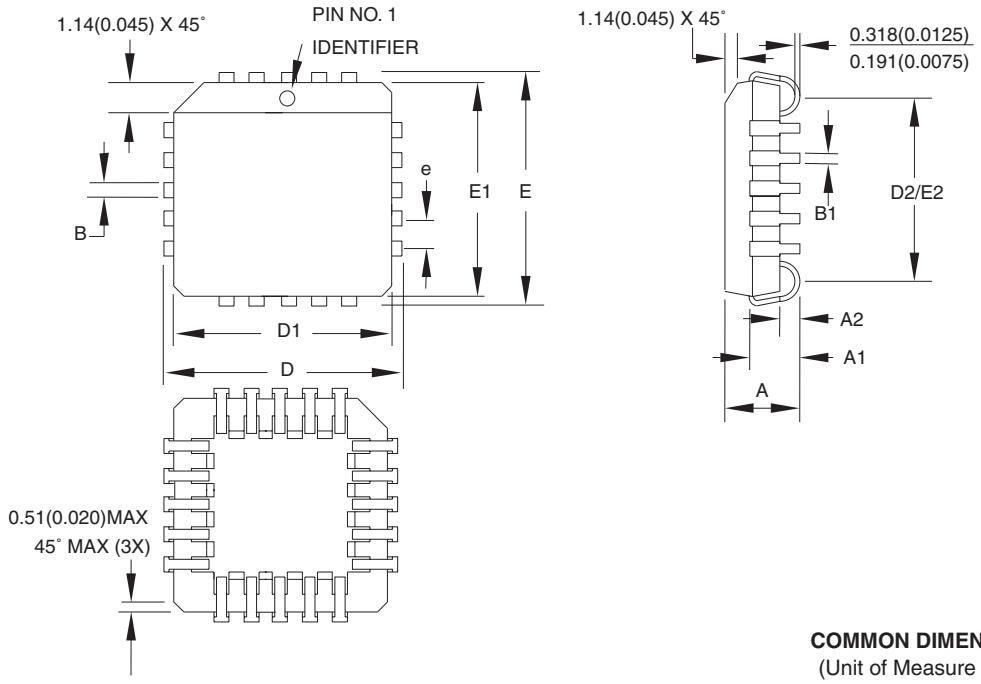
SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
θ	0°	–	8°	

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

3/17/05

	TITLE	DRAWING NO.	REV.
1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	8S1	C

23.4 20J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

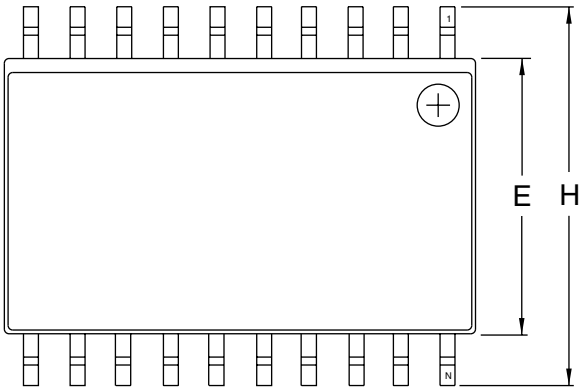
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	9.779	–	10.033	
D1	8.890	–	9.042	Note 2
E	9.779	–	10.033	
E1	8.890	–	9.042	Note 2
D2/E2	7.366	–	8.382	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

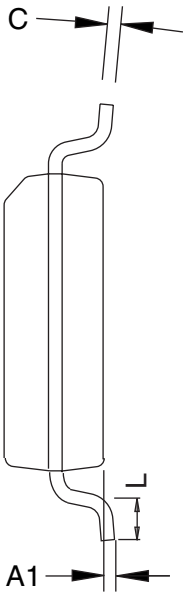
10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20J**, 20-lead, Plastic J-leaded Chip Carrier (PLCC)	20J	B

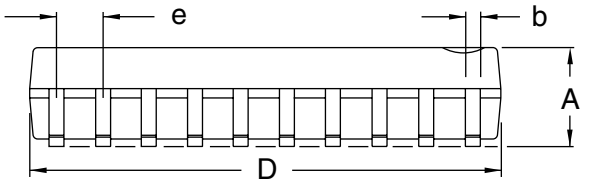
23.5 20S2 – SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

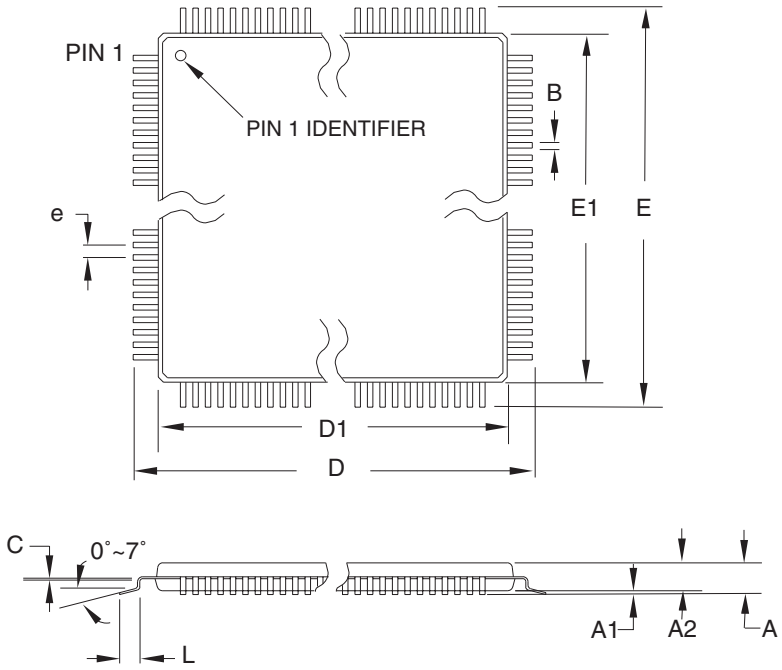
SYMBOL	MIN	NOM	MAX	NOTE
A	0.0926		0.1043	
A1	0.0040		0.0118	
b	0.0130		0.0200	4
C	0.0091		0.0125	
D	0.4961		0.5118	1
E	0.2914		0.2992	2
H	0.3940		0.4190	
L	0.0160		0.050	3
e	0.050 BSC			

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-013, Variation AC for additional information.
2. Dimension "D" does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006") per side.
3. Dimension "E" does not include inter-lead Flash or protrusion. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010") per side.
4. "L" is the length of the terminal for soldering to a substrate.
5. The lead width "b", as measured 0.36 mm (0.014") or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024") per side.

1/9/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20S2**, 20-lead, 0.300" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)	20S2	A

23.6 44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

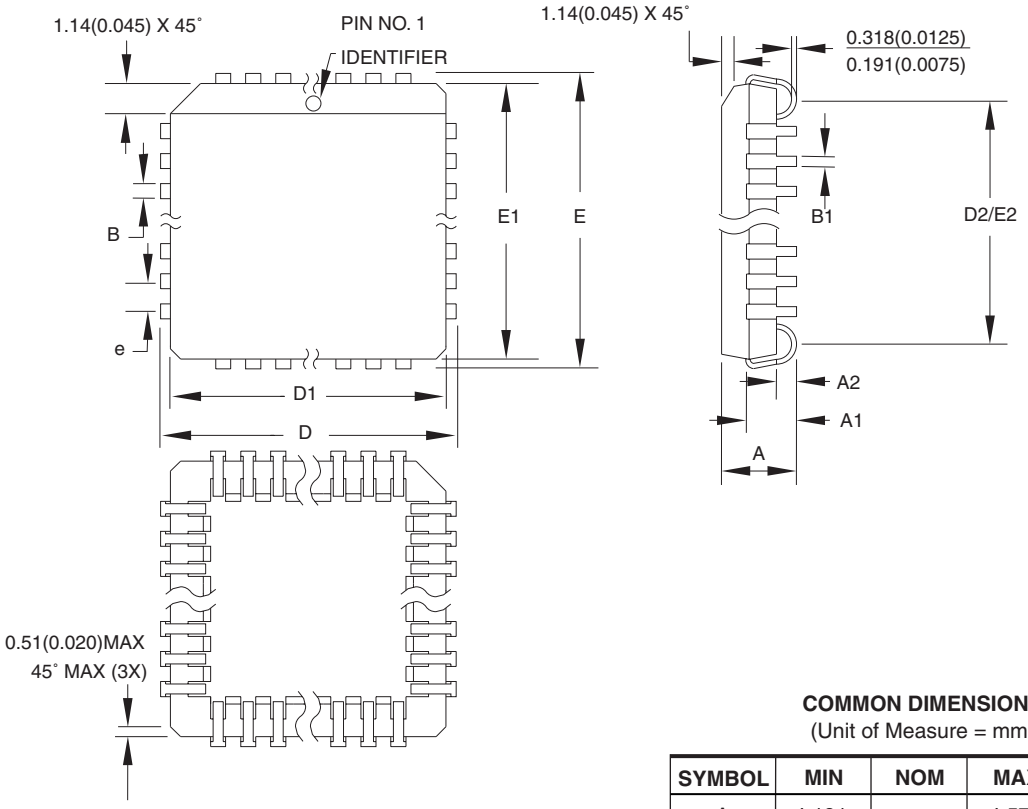
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A,** 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

23.7 44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

24. Revision History

Revision Level – Release Date	History
H – March 2006	Added last-time buy for AT17LVXXX-10CC and AT17LVXXX-10CI.

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2321H–CNFG–03/06