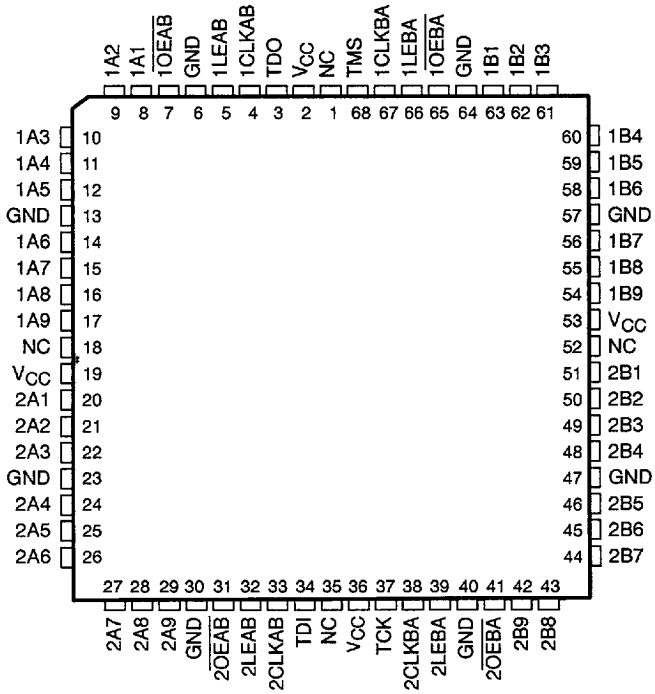
- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- B-Port Outputs of 'LVT182502 Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat (PM) Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat (HV) Packages Using 25-mil Center-to-Center Spacings

SN54LVT18502, SN54LVT182502 . . . HV PACKAGE
(TOP VIEW)



NC – No internal connection

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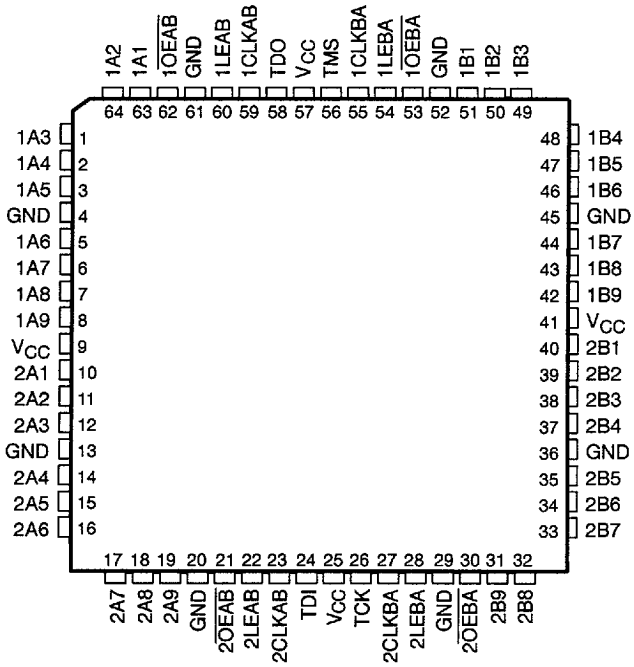
PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

SN74LVT18502, SN74LVT182502 . . . PM PACKAGE
(TOP VIEW)



description

The 'LVT18502 and 'LVT182502 scan test devices with 18-bit universal bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 18-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ universal bus transceivers.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low, A-bus data is stored on a low-to-high transition of CLKAB. When $\overline{OEAB}$ is low, the B outputs are active. When $\overline{OEAB}$ is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the $\overline{OEBA}$, LEBA, and CLKBA inputs.

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description (continued)

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The B-port outputs of 'LVT182502, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

The SN54LVT18502 and SN54LVT182502 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT18502 and SN74LVT182502 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE†
(normal mode, each register)

INPUTS				OUTPUT
$\overline{OEAB}$	LEAB	CLKAB	A	B
L	L	L	X	B_0‡
L	L	↑	L	L
L	L	↑	H	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Z

† A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established.

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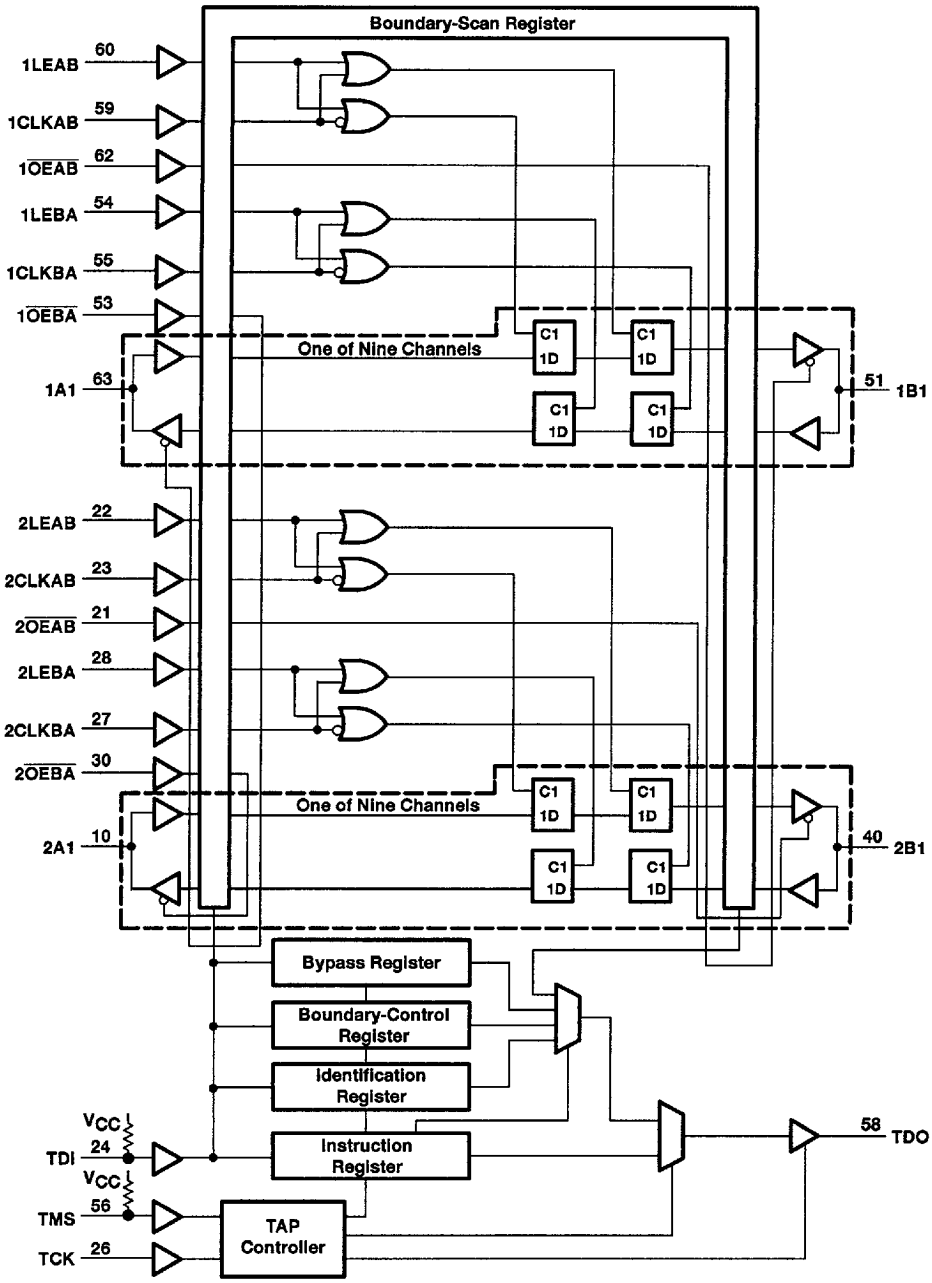
functional block diagram



Pin numbers shown are for the PM package.

Terminal Functions

TERMINAL NAME	DESCRIPTION
1A1–1A9, 2A1–2A9	Normal-function A-bus I/O ports. See function table for normal-mode logic.
1B1–1B9, 2B1–2B9	Normal-function B-bus I/O ports. See function table for normal-mode logic.
1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
GND	Ground
1LEAB, 1LEBA, 2LEAB, 2LEBA	Normal-function latch enables. See function table for normal-mode logic.
$1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, $2\overline{OEBA}$	Normal-function output enables. See function table for normal-mode logic.
TCK	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT18502 ..... 96 mA
SN54LVT182502 (A port or TDO) ..... 96 mA
SN54LVT182502 (B port) ..... 30 mA
SN74LVT18502 ..... 128 mA
SN74LVT182502 (A port or TDO) ..... 128 mA
SN74LVT182502 (B port) ..... 30 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT18502 ..... 48 mA
SN54LVT182502 (A port or TDO) ..... 48 mA
SN54LVT182502 (B port) ..... 30 mA
SN74LVT18502 ..... 64 mA
SN74LVT182502 (A port or TDO) ..... 64 mA
SN74LVT182502 (B port) ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): PM package (see Note 3) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. A 75-mil trace length was used to calculate Θ_{JA}.

recommended operating conditions

			SN54LVT18502		SN74LVT18502		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}‡	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS			SN54LVT18502			SN74LVT18502			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = − 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = − 24 mA		2						
		I_{OH} = −32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	CLK, LE, $\overline{OE}$, TCK			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	TDI, TMS			50			50	
		V_I = V_{CC}				1			1	
		V_I = 0				−100			−100	
		V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				1			1	
		V_I = 0				−5			−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−1			−1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			2			2	mA
			Outputs low			15			15	
			Outputs disabled			2			2	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				11			11		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

				SN54LVT18502				SN74LVT18502				UNIT
				V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA						0	100			MHz
t_w	Pulse duration	CLKAB or CLKBA high or low						5				ns
		LEAB or LEBA high						5				
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑						5				ns
		A before LEAB↓ or B before LEBA↓	CLK high					5				
			CLK low					5				
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑						0				ns
		A after LEAB↓ or B after LEBA↓						2				

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

			SN54LVT18502				SN74LVT18502				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK					0	25			MHz
t_w	Pulse duration	TCK high or low					20				ns
t_{su}	Setup time	A, B, CLK, LE, or $\overline{OE}$ before TCK↑					8				ns
		TDI before TCK↑					8				
		TMS before TCK↑					6				
t_h	Hold time	A, B, CLK, LE, or $\overline{OE}$ after TCK↑					1				ns
		TDI after TCK↑					1				
		TMS after TCK↑					1				
t_d	Delay time	Power up to TCK↑					50				ns
t_r	Rise time	V_{CC} power up					1				µs

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.
5. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18502				SN74LVT18502				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA						100				MHz
t_{PLH}	A or B	B or A					2	7			ns
t_{PHL}							2	7			
t_{PLH}	CLKAB or CLKBA	B or A					2.5	8.5			ns
t_{PHL}							2.5	8.5			
t_{PLH}	LEAB or LEBA	B or A					2.5	9			ns
t_{PHL}							2.5	9			
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A					2	10			ns
t_{PZL}							2	10			
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A					2.5	9			ns
t_{PLZ}							2.5	9			

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18502				SN74LVT18502				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK						25				MHz
t_{PLH}	TCK↓	A or B					3	22			ns
t_{PHL}							3	22			
t_{PLH}	TCK↓	TDO					2	12			ns
t_{PHL}							2	12			
t_{PZH}	TCK↓	A or B					3	22			ns
t_{PZL}							3	22			
t_{PZH}	TCK↓	TDO					2	12			ns
t_{PZL}							2	12			
t_{PHZ}	TCK↓	A or B					3	22			ns
t_{PLZ}							3	22			
t_{PHZ}	TCK↓	TDO					2	15			ns
t_{PLZ}							2	15			

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.
5. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

recommended operating conditions

			SN54LVT182502		SN74LVT182502		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current	A port, TDO		−24		−32	mA
		B port		−12		−12	
I_{OL}	Low-level output current	A port, TDO		24		32	mA
		B port		12		12	
I_{OL}†	Low-level output current	A port, TDO		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS			SN54LVT182502			SN74LVT182502			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA	A port, TDO	V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = −8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = −24 mA		2						
		I_{OH} = −32 mA					2			
		I_{OH} = −12 mA	B port	2			2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA	A port, TDO			0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
		I_{OL} = 12 mA	B port			0.8			0.8	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	CLK, LE, $\overline{OE}$, TCK			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	TDI, TMS			50			50	
		V_I = V_{CC}				1			1	
		V_I = 0				−100			−100	
		V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				1			1	
		V_I = 0				−5			−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−1			−1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			2			2	mA
			Outputs low			20			20	
			Outputs disabled			2			2	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				11			11		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

				SN54LVT182502			SN74LVT182502			UNIT
				V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	
				MIN	MAX	MIN MAX	MIN	MAX	MIN MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA					0	100		MHz
t_w	Pulse duration	CLKAB or CLKBA high or low					5			ns
		LEAB or LEBA high					5			
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑					5			ns
		A before LEAB↓ or B before LEBA↓	CLK high				5			
			CLK low				5			
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑					0			ns
		A after LEAB↓ or B after LEBA↓					2			

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

			SN54LVT182502			SN74LVT182502			UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	
			MIN	MAX	MIN MAX	MIN	MAX	MIN MAX	
f_{clock}	Clock frequency	TCK				0	25		MHz
t_w	Pulse duration	TCK high or low				20			ns
t_{su}	Setup time	A, B, CLK, LE, or $\overline{OE}$ before TCK↑				8			ns
		TDI before TCK↑				8			
		TMS before TCK↑				6			
t_h	Hold time	A, B, CLK, LE, or $\overline{OE}$ after TCK↑				1			ns
		TDI after TCK↑				1			
		TMS after TCK↑				1			
t_d	Delay time	Power up to TCK↑				50			ns
t_r	Rise time	V_{CC} power up				1			µs

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.
5. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT182502				SN74LVT182502				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA						100				MHz
t_{PLH}	A or B	B or A					2	8			ns
t_{PHL}							2	8			
t_{PLH}	CLKAB or CLKBA	B or A					2.5	9.5			ns
t_{PHL}							2.5	9.5			
t_{PLH}	LEAB or LEBA	B or A					2.5	10			ns
t_{PHL}							2.5	10			
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A					2	11			ns
t_{PZL}							2	11			
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A					2.5	9			ns
t_{PLZ}							2.5	9			

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT182502				SN74LVT182502				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK						25				MHz
t_{PLH}	TCK↓	A or B					3	25			ns
t_{PHL}							3	25			
t_{PLH}	TCK↓	TDO					2	12			ns
t_{PHL}							2	12			
t_{PZH}	TCK↓	A or B					3	25			ns
t_{PZL}							3	25			
t_{PZH}	TCK↓	TDO					2	12			ns
t_{PZL}							2	12			
t_{PHZ}	TCK↓	A or B					3	25			ns
t_{PLZ}							3	25			
t_{PHZ}	TCK↓	TDO					2	15			ns
t_{PLZ}							2	15			

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.
5. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW